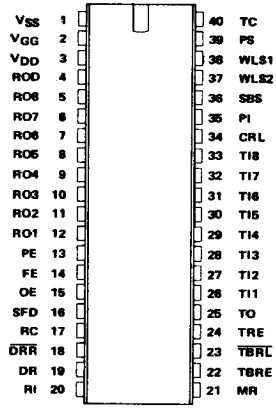
MOS
LSI

TMS 6011 JC, NC
ASYNCHRONOUS DATA INTERFACE (UART)

BULLETIN NO. DL-S 7612278, REVISED NOVEMBER 1977

- Transmits, Receives, and Formats Data
- Full-Duplex or Half-Duplex Operation
- Operation from DC to 200 kHz
- Static Logic
- Buffered Parallel Inputs and Outputs
- Programmable Word Lengths . . . 5, 6, 7, 8 Bits
- Programmable Information Rate
- Programmable Parity Generation/Verification
- Programmable Parity Inhibit
- Automatic Data Formatting
- Automatic Status Generation
- 3-State Push-Pull Buffers
- Low-Threshold Technology
- Standard Power Supplies . . . 5 V, −12 V
- Full TTL Compatibility . . . No External Components

40-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 6011 JC, NC is an MOS/LSI subsystem designed to provide the data interface between a serial communications link and data processing equipment such as a peripheral or a computer. The device is often referred to as an asynchronous data interface or as a universal asynchronous receiver/transmitter (UART).

The receiver section of the TMS 6011 will accept serial data from the transmission line and convert it to parallel data. The serial word will have start, data, and stop bits. Parity may be generated and verified. The receiver section will validate the received data transmission by checking proper start, parity, and stop bits, and will convert the data to parallel.

The transmitter section will accept parallel data, convert it to serial form, and generate the start, parity, and stop bits.

The TMS 6011 is a fully programmable circuit allowing maximum flexibility of operation, defined as follows:

- The receiver and transmitter sections are separate and can operate either in full-duplex (simultaneous transmission and reception) or in half-duplex mode (alternate transmission and reception).
- The data word may be externally selected to be 5, 6, 7, or 8 bits long.
- Baud rate is externally selected by the clock frequency. Clock frequency can vary between 0 and 200 kHz.
- Parity, which is generated in the transmit mode and verified in the receive mode, can be selected as either odd or even. It is also possible to disable the parity bit by inhibiting the parity generation and verification.
- The stop bit can be selected as either a single- or a double-bit stop.
- Static logic is used to maximize flexibility of operation and to simplify the task of the user. The data holding registers are static and will hold a data word until it is replaced by another word.
- Asynchronous operation allows the use of a single transmission line. The clock period has to be within ±4% of 1/16 of the time for one bit for the transmitter and/or receiver but no phase relationship is required.

To allow for a wide range of possible configurations, three-state push-pull buffers have been used on all outputs except **Transmitter Output (TO)** and **Transmitter Register Empty (TRE)**. They allow the wire-OR configuration.

UART

description (continued)

The TMS 6011 can be used in a wide range of data handling equipment such as modems, peripherals, printers, data displays, and minicomputers. By taking full advantage of the latest MOS/LSI design and processing techniques, it has been possible to implement the entire transmit, receive, and format function necessary for digital data communication in a single package, avoiding the cumbersome circuitry previously necessary.

P-channel enhancement-type low-threshold technology permits the use of standard power supplies (5 V, −12 V) as well as direct TTL interface. No external components are needed.

The TMS 6011 is offered in both 40-pin dual-in-line ceramic (JC suffix) and plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from −25°C to 85°C.

operation

The operation can be best understood by visualizing the TMS 6011 as three separate sections: 1) common control, 2) transmitter, and 3) receiver. The transmitter and receiver sections are independent while the control section directs both receive and transmit.

common control section

The common control section will direct both the receiver and the transmitter sections.

The initialization of the TMS 6011 is performed through the **Master Reset (MR)** terminal. The **MR** terminal is strobed to a high level after power turn-on to reset all status and transmitter registers and to reset **Transmitter Output (TO)** to a high level. The **Receiver Outputs (RO1-RO8)** are not controlled by the **MR** terminal.

Status flags **Parity Error, Framing Error, Overrun Error, Data Ready,** and **Transmitter Buffer Register Empty** are disabled when the **Status Flags Disable (SFD)** is at a high level. When disabled, the status flags float (three-state buffers are in the high-impedance state). The **Transmitter Register Empty (TRE)** status flag is not a three-state output.

The number of bits per word is controlled by the **Word Length Select 1 (WLS1)** and **Word Length Select 2 (WLS2)** inputs. The word length may be 5, 6, 7, or 8 bits. Selection is as follows:

WORD LENGTH	WLS1	WLS2
5	Low	Low
6	High	Low
7	Low	High
8	High	High

The parity to be checked by the receiver and generated by the transmitter is determined by the **Parity Select (PS)** input. A high level on the **PS** input selects even parity and a low level selects odd parity.

The parity will not be checked or generated if a high level is applied to **Parity Inhibit (PI)**; in this case the stop bit or bits will immediately follow the data bit.

When a high level is applied to **PI**, the **Parity Error (PE)** status flag is brought to a low level indicating a no-parity error because parity is disregarded in this mode.

To select either one or two stop bits, the **Stop Bit(s) Select (SBS)** terminal is used. A high level at this terminal will result in two stop bits while a low level will produce only one.

To load the control bits (**WLS1, WLS2, PS, PI,** and **SBS**) a high level is applied to the **Control Register Load (CRL)** terminal. This terminal may be strobed or hard wired to a high level.

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operation (continued)

transmitter section

The transmitter section will accept data in parallel form, then serialize, format, and transmit the data in serial form.

Parallel input data is received through the **Transmitter Inputs (TI1-TI8)**.

Serial output data is transmitted from the **Transmitter Output (TO)** terminal.

Input data is stored in the transmitter-buffer register. A low level at the **Transmitter Buffer Register Load ($\overline{\text{TBRL}}$)** command terminal will load a word in the transmitter-buffer register. The length of this word is determined by **Word Length Select 1 (WLS1)** and **Word Length Select 2 (WLS2)**. If a word of length greater than this appears at **TI8** through **TI1**, only the least significant bits are accepted. The word is justified into the least significant bit, **TI1**.

The data is transferred to the transmitter register when the $\overline{\text{TBRL}}$ terminal goes from low to high. The loading of the transmitter register is delayed if the transmitter section is presently transmitting data. In this case the loading of the transmitter register is delayed until the transmission has been performed.

Output serial data (transmitted from the **TO** terminal) is clocked out by **Transmitter Clock (TC)**. The clock rate is 16 times faster than the data rate.

The data is formatted as follows: start bit, data, parity bit, stop bits (1 or 2). Start bits, parity bits, and stop bits are generated by the TMS 6011. When no data is transmitted the output **TO** remains at a high level.

The start of transmission is defined as the transition of **TO** from a high to a low logic level.

Two flags are provided. A high level at the **Transmitter Buffer Register Empty (TBRE)** flag indicates that a word has been transferred to the transmitter/receiver and that the transmitter buffer register is now ready to accept a new word. A high level at the **Transmitter Register Empty (TRE)** flag indicates that the transmitter section has completed the transmission of a complete word including stop bits. The **TRE** flag will remain at a high level until the start of transmission of a new word.

Both the transmitter buffer register and the transmitter register are static and will perform long-term storage of data.

receiver section

The data is received in serial form at the **Receiver Input (RI)**. The data from **RI** enters the receiver register at a point determined by the character length, the parity, and the number of stop bits. **RI** must be maintained high when no data is being received. The data is clocked by the **Receiver Clock (RC)**. The clock rate is 16 times faster than the data rate.

Data is transferred from the receiver register to the receiver buffer register. The output data is then presented in parallel form at the eight **Receiver Outputs (RO1** through **RO8)**. The MOS output buffers used for the eight **RO** terminals are three-state push-pull output buffers that permit the wire-OR configuration through use of the **Receiver Output Disable (ROD)** terminal. When a high level is applied to **ROD** the **RO** outputs are floating. If the word length is less than 8 bits, the most significant bits will be at a low level. The output word is right justified. **RO1** is the least significant bit and **RO8** is the most significant bit.

A low level applied to the **Data Ready Reset ($\overline{\text{DRR}}$)** terminal resets the **Data Ready (DR)** output to a low level.

Several flags are provided in the receiver section. There are three error flags **(Parity Error, Framing Error,** and **Overrun Error)** and a **DR** flag. These status flags may be disabled by a high level at the **Status Flags Disable (SFD)** terminal.

A high level at the **Parity Error (PE)** terminal indicates an error in parity.

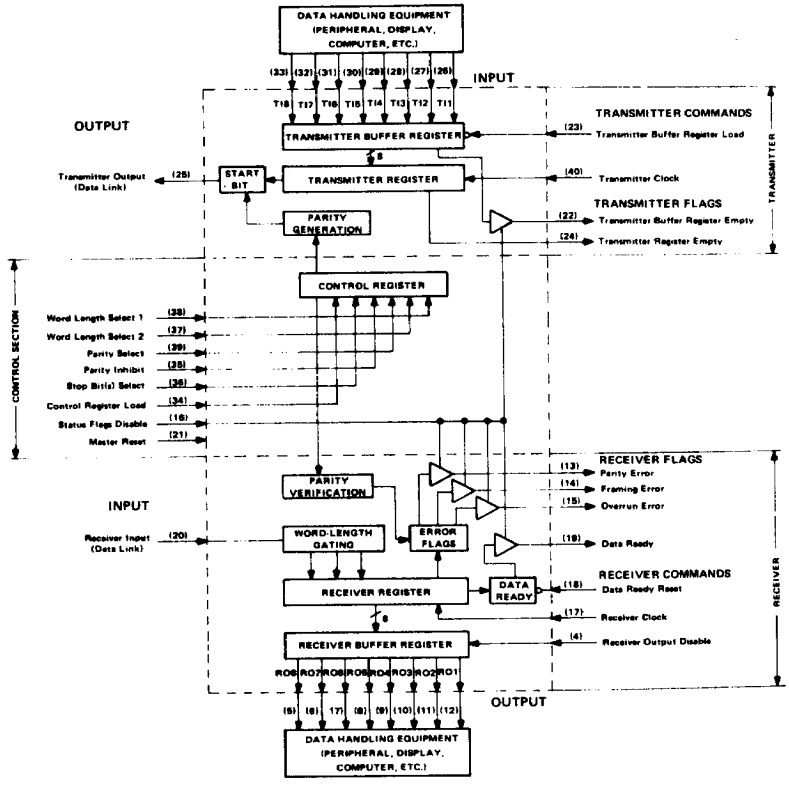
A high level at the **Framing Error (FE)** terminal indicates a framing error that is an invalid or nonexistent stop bit in the received word.

operation (continued)

A high level at the **Overrun Error (OE)** terminal indicates an overrun. An overrun occurs when the previous word has not been read, i.e., when the **DR** output has not been reset before the present data was transferred to the receiver buffer register.

A high level at the **DR** terminal indicates that a word has been received, stored in the receiver-buffer register and that the data is available at outputs **RO1** through **RO8**. The **DR** terminal can be reset through the $\overline{\text{DRR}}$ terminal.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Input voltage (any input) (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}			0		V
Supply voltage, V_{GG}		−11.5	−12	−12.5	V
Supply voltage, V_{SS}		4.75	5	5.25	V
High-level input voltage, all inputs, V_{IH} (see Notes 2 and 3)		V_{SS} −1.5		V_{SS} +0.3	V
Low-level input voltage, all inputs, V_{IL} (see Notes 2 and 3)		−12		0.8	V
Pulse width, t_w	Clock	2.5			μs
	Transmitter buffer register load	400			ns
	Control register load	250			ns
	Parity inhibit (see Notes 4 and 5)	400			ns
	Parity select (see Notes 4 and 5)	300			ns
	Word length select and stop bit select (see Notes 4 and 5)	300			ns
	Master reset	1.5			μs
	Data ready reset	250			ns
Data setup time, $t_{su(da)}$		10↓			ns
Data hold time, $t_{h(da)}$		20↑			ns
Clock frequency, f_ϕ (see Note 6)		0		200	kHz
Operating free-air temperature, T_A		−25		85	°C

NOTES: 2. All data, clock, and command inputs have internal pull-up resistors to allow direct clocking by any TTL circuit.
3. The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.
4. Inputs to PI, PS, WLS1, WLS2, and SBS are normally static signals. A minimum pulse width has been indicated for possible pulsed operation.
5. All control signal pulses should be centered with respect to CRL to ensure maximum setup and hold time.
6. Clock frequency is 16 times the baud rate.

↑↓The arrow indicates the edge of the $\overline{TBRL}$ pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.6	V
I_{IH}	High-level input current, all inputs	V_I = 5 V			10	μA
I_{IL}	Low-level input current, all inputs	V_I = 0 V			−1.6	mA
I_{GG}	Supply current from V_{GG}	All inputs at a high level		11	16	mA
I_{SS}	Supply current from V_{SS}	All inputs at a high level		20	35	mA
P_D	Power dissipation	All inputs at a high level		240	385	mW
C_i	Input capacitance, all inputs	V_I = V_{SS}, f = 1 MHz		10	20	pF

†All typical values are at T_A = 25°C and nominal voltages.

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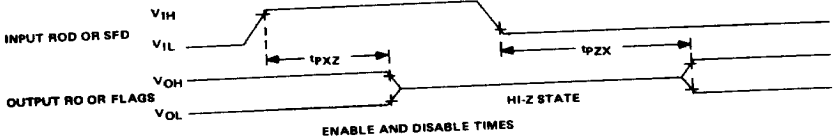
switching characteristics over full ranges of recommended operating conditions (unless otherwise noted)

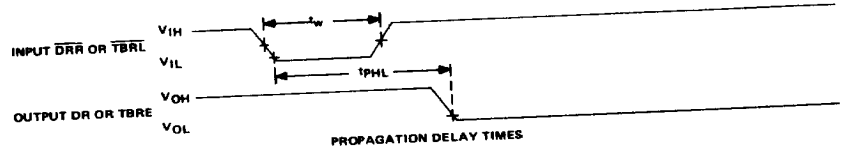
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level DR output from $\overline{DRR}$	1 Series 74 TTL load		800	1000	ns
t_{PHL}	Propagation delay time, high-to-low level TBRE output from $\overline{TBRL}$			800	1000	ns
t_{PZX}	Enable time, receiver output from ROD			300	500	ns
t_{PXZ}	Disable time, receiver output from ROD			300	500	ns
t_{PZX}	Enable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns
t_{PXZ}	Disable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns

†All typical values are at $T_A = 25°C$ and nominal voltages.

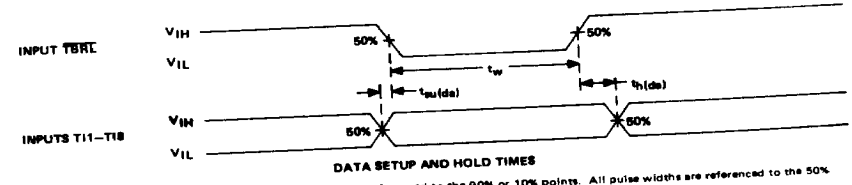
voltage waveforms



ENABLE AND DISABLE TIMES



PROPAGATION DELAY TIMES



DATA SETUP AND HOLD TIMES

NOTE: All enable, disable, and propagation delay times are referenced to the 90% or 10% points. All pulse widths are referenced to the 50% points.

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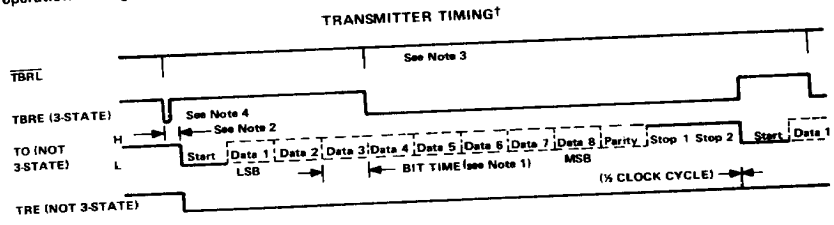
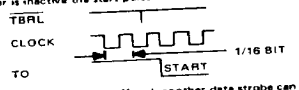
operation timing diagram



† Transmitter initially assumed inactive at start of diagram, shown for 8 level code and parity and 2 stops.

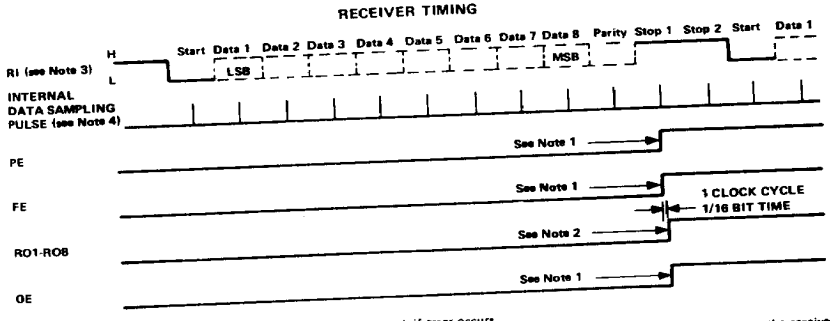
NOTES: 1. Bit time is 16 clock cycles.

2. If transmitter is inactive the start pulse will appear on line within one clock cycle of time data strobe occurs (see detail below).



3. Because transmitter is double buffered, another data strobe can occur anywhere during transmission of character 1.

4. TBRE goes to a low for a period of approximately one clock cycle following a $\overline{\text{TBRL}}$ pulse.



NOTES: 1. This is the point at which the error condition is detected, if error occurs.

2. A high-to-low transition on the DR pin indicates that the contents of the receiver register has been transferred to the receiver buffer register and that the three error-flag signals are valid. Output data remains valid until the next word is transferred into the receiver buffer register.

3. The RI waveform illustrates an eight-bit word with parity and two stop bits. If parity is inhibited, the stop bits immediately follow the last data bit. For all word lengths, the data in the buffer register must be right justified, i.e., RO1 (pin 12) is the least significant bit.

4. Data sampling occurs at the center of each data bit (8 clock cycles after the beginning of the bit).

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