# CHAPTER 6

# MICROCOMPUTER BOARD A6A2

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# CHAPTER 6

# MICROCOMPUTER BOARD A6A2

## INTRODUCTION

1. The microcomputer board contains the CPU, the static memory interface (SMI) device, the ROM and RAM devices with associated address decoders, input/output (I/O) expansion circuitry and a power up/down reset circuit. A block diagram of the CPU and SMI is given in Fig. 6.1 and circuit and layout diagrams of the board are given in figs. 6.2 and 6.3, at the end of the chapter.

## CENTRAL PROCESSING UNIT (CPU)

2. The 3850 is the Central Processing Unit for the F8 system. It is an 8-bit arithmetic device with over 70 instructions and contains a 64-byte scratchpad RAM, an instruction register, an accumulator, two parallel I/O ports, interrupt control, a status (W) register, a clock generator, a power-on reset circuit and control logic. Unlike most other 8-bit microprocessors, the 3850 does not provide an address bus and requires the use of an additional device from the F8 range to interface with external memory. In this application, a 3853 Static Memory Interface (SMI) device is used and fig. 6(1) shows the two devices in block diagram form, together with interconnections.

### Arithmetic and Logic Unit (ALU)

3. The 8-bit parallel ALU performs the required arithmetic or logic operations. These include binary add, decimal adjust, add with carry, decrement and increment, together with logical operations AND, OR, Exclusive OR and 1s complement. The ALU also produces four output signals to represent the status of a result. These signals, stored in the status register, are described in para.7.

### Accumulator

4. The accumulator is a general purpose 8-bit register used for data manipulations within the CPU, and is used by the ALU to hold the result of a completed operation.

### Instruction Register

5. The instruction register stores the instruction operation (OP) code during the instruction execution sequence. The OP code is loaded into the instruction register from the data bus at the end of the execution sequence for the previous instruction.

### Scratchpad

6. The scratchpad consists of 64 8-bit RAM registers (00 to 3F hexadecimal) which are used as general purpose working memory locations. The associated 6-bit address register is used to address any of the 64 scratchpad registers.

Status Register

7. The status register (also known as the W register) holds five bits of status information, as follows.

8. Sign(S). Bit 0 is the sign bit; when the result of an ALU operation is interpreted as a signed binary number, the most significant bit (bit 7) represents the sign of the number. At the conclusion of an instruction that may modify bit 7 of the accumulator, the sign bit is set to the complement of accumulator bit 7.

9. Carry (C). The carry bit is set to a '1' when the sum of two bytes is greater than 255.

10. Zero (Z). Bit 2 is set to a '1' when an arithmetic or logical operation produces a zero result.

11. Overflow (O). When the result of an ALU operation is interpreted as a signed binary number, bit 7 of the result is used to represent the sign of the number (para.8). Bit 6 then becomes the most significant bit of the signed binary number, and the overflow bit is thus used to indicate a carry from bit 6.

12. Interrupt (ICB bit). The interrupt control bit (bit 4 of the status register) is set to '0' when the CPU acknowledges the receipt of an interrupt request (i.e. a '0' at the /INT REQ input from either the static memory interface U4 or from a peripheral input/output device on the SCORE interface board). The /ICB output signal from the CPU (U2 pin 22) is set to a '1', and this is applied to the /PRI IN input of U4 (via R16) and to the /PRI IN input of the peripheral input/output device on the SCOPE interface board, to inhibit further interrupts. The ICB bit is subsequently set to a '1' by the system software, and this resets the /ICB output to a '0' so that further interrupt requests can be serviced by the CPU.

Interrupt Control

13. The interrupt facility allows devices external to the CPU (in this application the 3853 static memory interface device U4 and the 3861 peripheral input/output device on the SCORE interface board) to suspend execution of the main program and cause the CPU to execute a different program stored at a predetermined set of locations in memory. An interrupt sequence is initiated by the application of a '0' to the /INT REQ input of the CPU (U2 pin 23). Provided that /ICB output is at logic '0', the CPU acknowledges the interrupt request at the end of the next interruptable instruction, by forcing the /ICB output to logic '1', and by initiating a set of instructions which causes program execution to jump to an address supplied by the interrupting device. In the case of the 3861 peripheral input/output device on the SCORE interface card, this interrupt vector address is mask programmed whereas the interrupt vector address held by the 3853 static memory interface device is programmable.

14. So that the interrupted main program may be resumed at the end of the interrupting program, the address of the next main program instruction at the time the interrupt is serviced (the continuation address) is held in the stack register of the 3853 static memory interface device U4

(para. 19), whilst the CPU accumulator and status register contents are deposited in the scratchpad RAM (under software control).

Control Logic

15. The five ROMC lines (ROMC0 to ROMC4) are used to convey commands from the CPU to the other devices in the system. At the beginning of each cycle, the CPU decodes the instruction and a command is presented on these lines to indicate the operation to be performed during the current cycle by the rest of the system. The 32 possible states of the five ROMC lines, and the corresponding commands (as far as the MA 1075 is concerned) are listed in Table 1.

Table 1: ROMC States

| ROMC LINES | | FUNCTION |
|---|---|---|
| 4 3 2 1 0 | HEX | |
| 0 0 0 0 0 | 00 | Fetch instruction. The operation code in memory at the address contained in the program counter (SMI) is placed on the data bus. The program counter is then incremented. |
| 0 0 0 0 1 | 01 | The content of the memory location at the address contained in the program counter is placed on the data bus. The 8-bit value on the data bus is added, as a signed binary number, to the contents of the program counter. Used for branch instructions. |
| 0 0 0 1 0 | 02 | The content of the memory location at the address contained in data counter DC (SMI) is placed on the data bus. DC is then incremented. |
| 0 0 0 1 1 | 03 | Fetch operand immediate. The operand in the memory location at the address contained in the program counter is placed on the data bus. The program counter is then incremented. |
| 0 0 1 0 0 | 04 | Copy the contents of the stack register into the program counter. |
| 0 0 1 0 1 | 05 | Store the data bus content in the memory location whose address is contained in data counter DC, then increment DC. |
| 0 0 1 1 0 | 06 | The high order byte contained in data counter DC is placed on the data bus. |

Table 1: ROMC States (Cont'd)

| ROMC LINES | | FUNCTION |
|---|---|---|
| 4 3 2 1 0 | HEX | |
| 0 0 1 1 1 | 07 | The high order byte contained in the stack register is placed on the data bus. |
| 0 1 0 0 0 | 08 | The content of the program counter is copied into the stack register. The CPU clears the data bus to the all-zero state, and the data bus content is then loaded into the program counter, in two bytes, thus cleaning the counter. |
| 0 1 0 0 1 | 09 | The low order byte contained in data counter DC is placed on the data bus. |
| 0 1 0 1 0 | 0A | The 8-bit value on the data bus is added, as a signed binary number, to the content of data counter DC. |
| 0 1 0 1 1 | 0B | The low order byte contained in the stack register is placed on the data bus. |
| 0 1 1 0 0 | 0C | The content of the memory location at the address contained in the program counter is placed on the data bus, and is then transferred as the low order byte into the program counter. |
| 0 1 1 0 1 | 0D | The content of the program counter, incremented by one, is stored in the stack register. The program counter is unaltered. |
| 0 1 1 1 0 | 0E | The content of the memory location at the address contained in the program counter is placed on the data bus, and is then transferred as the low order byte into data counter DC. |
| 0 1 1 1 1 | 0F | The interrupting device with the highest priority places the low order byte of the interrupt vector onto the data bus. The content of the program counter is transferred to the stack register, and the data bus content is loaded into the low order byte of the program counter. |
| 1 0 0 0 0 | 10 | Inhibit any modification to the interrupt priority logic. |

Table 1: ROMC States (Cont'd)

| ROMC LINES | | FUNCTION |
|---|---|---|
| 4 3 2 1 0 | HEX | |
| 1 0 0 0 1 | 11 | The content of the memory location at the address contained in the program counter is placed on the data bus. The data bus content is then loaded as the high order byte into data counter DC. |
| 1 0 0 1 0 | 12 | The content of the program counter is loaded into the stack register. The content of the data bus is then loaded into the low order byte of the program counter. |
| 1 0 0 1 1 | 13 | The interrupting device with the highest priority places the high order byte of the interrupt vector onto the data bus, and then loads the data bus content as the high order byte into the program counter. The interrupt circuitry of the interrupting device is reset so that the CPU can respond to a further interrupt request. |
| 1 0 1 0 0 | 14 | The content of the data bus is loaded as the high order byte into the program counter. |
| 1 0 1 0 1 | 15 | The content of the data bus is loaded as the high order byte into the stack register. |
| 1 0 1 1 0 | 16 | The content of the data bus is loaded as the high order byte into data counter DC. |
| 1 0 1 1 1 | 17 | The content of the data bus is loaded as the low order byte into the program counter. |
| 1 1 0 0 0 | 18 | The content of the data bus is loaded as the low order byte into the stack register. |
| 1 1 0 0 1 | 19 | The content of the data bus is loaded as the low order byte into data counter DC. |
| 1 1 0 1 0 | 1A | During the prior cycle an I/O port or interrupt control register was addressed. The data bus content is loaded into the addressed port or register. |

Table 1: ROMC States (Cont'd)

| ROMC LINES | | FUNCTION |
|---|---|---|
| 4 3 2 1 0 | HEX | |
| 1 1 0 1 1 | 1B | During the prior cycle, the data bus specified the address of an I/O port. The content of the addressed I/O port is placed on the data bus. (Note that the timer and interrupt control registers cannot be read by the CPU.) |
| 1 1 1 0 0 | 1C | None (No-op) |
| 1 1 1 0 1 | 1D | The content of data counter DC is loaded into data counter DC1, and the content of data counter DC1 is loaded into data counter DC. |
| 1 1 1 1 0 | 1E | The low order byte of the program counter is placed on the data bus. |
| 1 1 1 1 1 | 1F | The high order byte of the program counter is placed on the data bus. |

Power-On Reset

16. When the CPU external reset line (U2 pin 37) is taken to 0 V and then returned to +5 V, power-on detection circuitry within the CPU sets the program counter (SMI device) to zero and inhibits interrupt acknowledgement by clearing the ICB bit in the status register to zero. Since the first instruction of the operating program is stored at memory location 0000, program execution is automatically started (or restarted) when the MA 1792 is switched on. If the +5 V supply subsequently falls below a pre-determined level, the CPU external reset line is held at 0 V and this holds the CPU in an idle state (the power up/down reset circuit is described in para.31).

Input/Output Ports

17. The CPU has two high-speed 8-bit I/O ports designated port 0 and port 1. In this application, these two I/O ports are used only by the SCORE interface board.

Clock Circuits

18. The clock generator within the CPU may be operated in the crystal mode (2 MHz crystal connected between pins 38 and 39 of U2) or in the RC mode (simple resistor/capacitor network). In this application the crystal mode is used and the RC connection (U2 pin 40) is taken to 0 V. The clock circuits generate all the timing signals required by the microcomputer. The two primary timing signals, Ø and WRITE, are used for instruction execution sequence timing. The falling edge of the WRITE signal denotes the beginning of a new machine cycle, while Ø is used to time the length of individual machine cycles (either 4 or 6 Ø periods long).

STATIC MEMORY INTERFACE

19. The 3853 static memory interface device provides the necessary address lines and control signals to interface with up to 64k bytes of external static memory (in this application 8k of ROM and 2k bytes of RAM). The device also contains the program counter, stack register and two data counters which are used by the CPU, and a programmable timer. The block diagram of the device is shown, together with the 3850 CPU, in fig. 6(1).

Address Bus A0 - A15

20. These lines are used to address the external ROM and RAM devices. Lines A0 to A11 are used to address the 4 k ROM devices U8, U9, lines A0 to A10 are used to address RAM (U11), whilst lines A12 and A13 are used for address decoding purposes. The remaining address lines (A14, A15) are not used in this application.

Data Bus DB0 - DB7

21. This 8-bit bus provides bi-directional communication between the static memory interface device and the CPU.

Memory Control

22. This provides three output signals, CPU READ, REGDR and /RAM WRITE. CPU READ is set to a '1' for a ROM read cycle; in this application it is inverted by U5f to enable the ROM address decoder U7A (para.36). REGDR (register drive) is not used in the RA 1792 and no connection is made to this pin (this output is not shown in fig. 6.1. /RAM WRITE is used to control the RAM read/write line, and is set to a '0' for a write cycle, to a '1' for a read cycle.

Program Counter

23. This is a 16-bit register which is used to hold the memory address from which the next object program code must be fetched.

Stack Register

24. The 16-bit stack register is used as a buffer for the program counter. The content of the stack register is never used directly to address memory.

Data Counters

25. Data counter DC is used to address memory locations which contain individual data bytes or bytes within data tables to be used as operands. Data counter DC1 is an auxiliary data counter, which can be used to save the content of DC by using the command 'exchange data counters'. This instruction puts the contents of DC into DC1 and the contents of DC1 into DC.

Control Logic

26. The five ROMC lines are used by the CPU to convey commands to the 3853 static memory interface device, as listed in table 1.

Programmable Timer

27. The 3851 static memory interface contains a programmable timer which is used in conjunction with interrupt logic to generate real-time intervals. The timer consists of a polynomial shift register which is made to count down to zero from a programmed starting number. When a count of zero is reached (every 500 micro seconds), an interrupt request signal is produced at U4 pin 4. When the interrupt is serviced by the CPU, control is passed to a clock interrupt handler routine; this counts successive interrupts and, dependent on the number of interrupts counted, calls one of a number of subroutines to, for example, service the front panel shaft encoder, service the front panel push buttons, or update the front panel displays.

Interrupt Control

28. The 3853 SMI device may originate an interrupt request signal either internally from the programmable timer (para. 27) or following the arrival of a 0 V signal at the /EXT INT pin. In this application, however, the /EXT INT pin (U4 pin 7) is permanently connected to the +5 V rail. The logic '0' interrupt request signal is only produced at U4 pin 4 when a '0' is also present at the /PRI IN pin (U4 pin 5). If a '1' is present at this pin, denoting that an interrupt is currently being serviced by the CPU, then an interrupt request is latched until such time as the level at the /PRI IN pin reverts to 0 V.

29. The interrupt vector address is programmed into the 3853 SMI device during the software initialisation routine following switch-on. When the interrupt request is serviced, this address is loaded into the program counter and program execution continues from that address.

Timing

30. All timing within the 3853 static memory interface device is controlled by the Ø and WRITE signals produced by the 3850 CPU. Each machine cycle will contain either 4 Ø clock periods (short cycle) or to 6 Ø clock periods (long cycle).

Power Up/Down Reset

31. In this circuit, U16a is connected as a comparator which, once its operating point is reached behaves as a shmitt trigger. The unregulated +5 V supply input (approximatley 10 V) at J1 pins 15 and 16 comes from the power supply module and is taken from the line which supplies the +5 V regulator. When the receiver is switched on, the unregulated +5 V supply begins to rise exponentially from 0 V. Whilst this rising voltage is below the threshold set by the voltage reference device U14, the output of U16a goes high. Once the level of the rising unregulated +5 V supply exceeds the threshold of U14, U16a output goes low. R8 provides positive feedback for the Schmitt action and Q1 inverts the output of U16a before applying it to pin 37 of the CPU. Thus the $\overline{\text{Reset}}$ line is held low for a short time at switch-on, and is released after the +5 V line has been established. After CPU reset, program execution commences at memory location 0000. The reset output signal from U16a is also applied to the RAM Chip Enable circuit (para. 33) and to the front panel memory board (chapter 10), via J1 pin 13. The reset output is also taken to pin 2 of J2 which mates with the SCORE interface board, but is not used on this board.

32. If the level of the +5 V unregulated supply subsequently falls below the threshold set by U16a, then U16a output rises rapidly, and, via Q1, the CPU is reset and held in the idle condition before the regulated +5 V is degraded.

RAM Enables $\overline{\text{CE}}$

33. To enable the RAM device U11 a '0' must be applied to the $\overline{\text{CE}}$ input. A '0' is produced at the $\overline{\text{CE}}$ input by decoder U7b and Q4 when the correct address is present on the address bus. Q4 is driven by Q3 both of which are turned on only after the +5V supply has been established and U16a output is low, the reset period being over.

34. As stated in para. 32, the 0 V reset signal is produced if the level of the +5 V unregulated supply falls below the threshold set by U16a (due to a supply failure or when the unit is switched off). When this occurs, the CPU is reset at the end of the current instruction, and the RAM $\overline{\text{CE}}$ enable signal is maintained for the duration of this last cycle due to the charge on C10 being discharged by R15 and R16 sufficiently slowly maintaining Q4 in conduction to allow this. The RAM device then enters the data-retention mode and the Vdd supply (from the battery back-up circuit) is allowed to fall to approximately 2.6 V.

Battery Back-up Circuit

35. The normal Vdd supply for the RAM devices is provided by Q2. This transistor conducts when power is applied to the unit; CR4 clamps the base of Q2 at approximately +5.6 V and C11 rapidly charges to the resulting +5 V RAM Vdd supply available on Q2 emitter. When power is connected the battery, B1, is charged via R17 and when power is disconnected, C11 slowly discharges into the RAM Vdd terminals, and the battery. When C11 is sufficiently discharged, current flows from B1 via R17 to maintain the RAM device in the data-retention mode. (Approximately 2.6 V at less than 40 microamps for the RAM device).

MEMORY ADDRESS DECODING

36. The address decoder comprises a dual 2-line to 4-line decoder U7A, U7B, and inverting buffer U5F. For a ROM read operation, the CPU READ output from U4 is set to a '1'. This is inverted by U5F to enable U7A (table 2) and the levels present on the A11 and A12 address bus lines are decoded to enable one of the ROM devices U8 or U9 (table 3). For addresses in the range 0000 to 17FF, tables 2 and 3 show that the Y2 output of U7A is set to a '1', and this is used to output-disable the two RAM devices, U11 and U12.

37. The 256 bytes of RAM respond to addresses in the range 1800 to 18FF. Thus with both the A11 and A12 address bus lines at '1' (table 3), the resulting '0' at the Y2 output from U7A removes the output-disable condition from U11 and U12, the '0' at the Y2 output of U7B enables the two RAM devices, and a RAM read or write operation is performed dependent on the state of the RAM write output at U4 pin 6 ('0' for write, '1' for read).

Table 2: 2-Line to 4-Line Decoder Truth Table

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $\overline{E}$ | B | A | $\overline{Y3}$ | $\overline{Y2}$ | $\overline{Y1}$ | $\overline{Y0}$ |
| 1 | x | x | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 |

x denotes either 0 or 1

INPUT/OUTPUT INTERFACE

38. Communication between the microcomputer and the front panel memory board is made via the I/O control bus (J1 pins 26 and 28 to 34) and the I/O data bus (J1 pins 1 to 8), together with I/O read and write strobe (WSTB) timing signals (J1 pins 27 and 25). The I/O control bus, the I/O read and the WSTB timing signals are also used on the SCORE interface board, together with the processor bus and the ROMC control bus.

ROMC Decoder

39. Table 1 shows that the ROMC states applicable to input/output operations are hexadecimal 1A and 1B. When either of these two states is present, the inputs to NAND gate U1A are all at '1' resulting in '0' at the output, and both inputs to NOR gate U3A are thus at '0', resulting in a '1' at the output.

Table 3: Memory Address Decoding

| ADDRESS BUS | | | | | U7a | | | | | | | U7b | | | | | ADDRESSED MEMORY |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HEX | A15 | A14 | A13 | A12 | $\overline{E}$ | B | A | $\overline{Y3}$ | $\overline{Y2}$ | $\overline{Y1}$ | $\overline{Y0}$ | $\overline{E}$ | B | A | $\overline{Y3}$ | $\overline{Y2}$ | |
| 0000<br>0FFF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | ROM U8 READ |
| 1000<br>1FFF | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | ROM U9 READ |
| 2000<br>2FFF | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | RAM U11 READ OR WRITE |
| 3000<br>3FFF | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | U13a READ TEST SWITCHES |

I/O Read Operation

40. For an I/O read operation, the ROMC lines are set to the 1B state. This state specifies (table 1) that during the previous cycle, the required I/O address was present on the processor data bus. Since for the duration of this previous cycle, the ROMC lines were not in the 1A or 1B state, the output from U3A was at '0', and the required I/O address was clocked into the octal D-type latch U6 by the WRITE clock signal from U2 (applied via inverter U5A and NOR gate U3B).

41. With a 1B state present on the ROMC lines, the output from U3A changes to logic '1'. This is routed to:

    (1) The output enable input of the octal latch U6 via inverter U5C, and the I/O address is latched at the Q outputs.

    (2) One input of NOR gate U3D via inverter U5C, but since the remaining input is fed from the ROMC0 line (which is set to a '1' for the 1B state), the output of U3D is forced to a '1'. This is applied to the direction (DIR) input of the octal bus transceiver U10 to set it to the direction B to A.

    (3) One input of NOR gate U3C via inverter U5C. Provided the Q7 output from U6 is not at logic '1' i.e. the I/O address is numerically less than hexadecimal 80, then the output of U3C is set to a '1'. This is inverted by U5D and the octal bus transceiver U10 is enabled.

    (4) One input of NAND gate U1B where it is combined with the '1' at the ROMC0 line to produce a 3 microsecond negative-going I/O read pulse.

42. The data content of the I/O port (on the front panel memory board) at the address present on the I/O control bus is then placed on the I/O data bus and is routed to the CPU via the octal bus transceiver U10 and the processor data bus.

43. If bit 7 of the I/O address from U6 is at a '1', signifying an I/O address of hexadecimal 80 or above, the enable signal (G) for the octal bus transceiver U10 is not produced ('1' at the Q7 output of U6), and data is taken from the SCORE interface board via the processor data bus (I/O port address 88).

I/O Write Operation

44. For an I/O write operation, the ROMC lines are set to the 1A state. This state specifies (table 1) that during the previous cycle, the required I/O address was present on the processor data bus. As for the I/O read operation, this address was clocked into U6 during the previous cycle by the CPU WRITE clock signal, applied via U5A and U3B ('0' at U3A output).

45. With a 1A state present on the ROMC lines, the output from U3A changes to a '1' and this is routed to:

    (1) The output enable input of octal latch U6 via inverter U5C, and the I/O address is latched at the Q outputs.

(2) One input of NOR gate U3D via inverter U5C, and since the ROMC0 line is at logic '0', a '1' is applied to the direction (DIR) input of the octal bus transceiver U10 to set it to the direction A to B.

(3) One input of NOR gate U3C via inverter U5C. Provided the Q7 output from U6 is not at logic '1' i.e. the I/O address is numerically less than hexadecimal 80, then the output of U3C is set to a '1'. This is inverted by U5D and the octal bus transceiver is enabled.

(4) One input of NAND gate U1C, where it is combined with the '0' at the ROMC0 line inverted by U5E and the next positive-going excursion of the WRITE clock signal to produce a 500 nanosecond negative-going write strobe (WSTB) signal.

46. The data present on the CPU data bus is then loaded into the addressed port (on the front panel memory board) via U10 and the I/O data bus. As the I/O write operation using the I/O control bus is confined to the front panel memory board, the situation where bit 7 of the I/O address bus is at a '1' does not arise, and the write strobe is not used on the SCORE interface board.

BITE

47. SA contains 4 independent switches which may select a '0' (closed) or a '1' (open and pulled-up by a resistor in U17). The resultant code is applied to U13a and is made available to the data bus when U13a pin 1, is selected by the address bus via U7a. This arrangement is used during BITE Signature Analysis Tests. U13 is read once in each Software-Background Loop, approximately every 30 ms, to check for changes in SA. U15, U13b, CR1 and CR2 provide status indication of the code set on SA. U15 is a quad latch of which two sections are used, Q0 and Q1, to drive the 2 LEDs CR1 and CR2 via buffer U13b. CR1 and CR2 may be addressed independently under control of the system software, and may be on, off or flashing. Table 4 shows the positions of SA, plus the corresponding states of LEDs CR1 and CR2, and which routine is running. Returning to Normal receiver operation from any BITE mode leaves the receiver in BITE continuous update mode. Normal receiver operation can be obtained by pressing RCL on the front panel.

Table 4: SA Operation

| SA | | | | LED STATE | | ROUTINE RUNNING |
|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | CR1 | CR2 | |
| 1 | 1 | 1 | 1 | on | on | Normal Receiver Operation |
| 0 | 1 | 1 | 1 | flashing | flashing | ROM Signature Analysis |
| 1 | 0 | 1 | 1 | on | flashing | I/O Exercise |
| 0 | 0 | 1 | 1 | flashing | off | DAC Ramptests (Not Signature Analysis) |
| Any Other | | | | flashing | on | BITE Continuous Update mode |

ROM DEVICES

48. The two ROM devices fitted to the microcomputer board are 4096by 8-bit organised (4 K) and are usually of the ultra-violet (UV) erasable type. This type of device may be identified from all other types in that a transparent window is set into the top surface. Where UV type devices are in use they must at all times be protected from direct light. Should it be necessary to remove the microcomputer board from the unit for a prolonged period of time, non-transparent covers should be fitted over the UV erasable devices (a self adhesive label is fitted to the top face of each device at the factory, for identification purposes).

ROM Replacement Instructions

49. Ensure that all ROM devices fitted to a particular board have the same program number, last suffix letter and program issue number. When ordering a replacement ROM device, quote the RA 1792 serial number and the full information printed on the label attached to the faulty device. The label information takes the following form:

Pnnnnn/2/A
Iss.1 dddd.

where: (1) Pnnnnn is the software reference number

(2) The first suffix number is the programmed device (PD) number (PD2 in this example), where

PD1 is located at U8 (0000-0FFF)
PD2 is located at U9 )1000-1FFF)

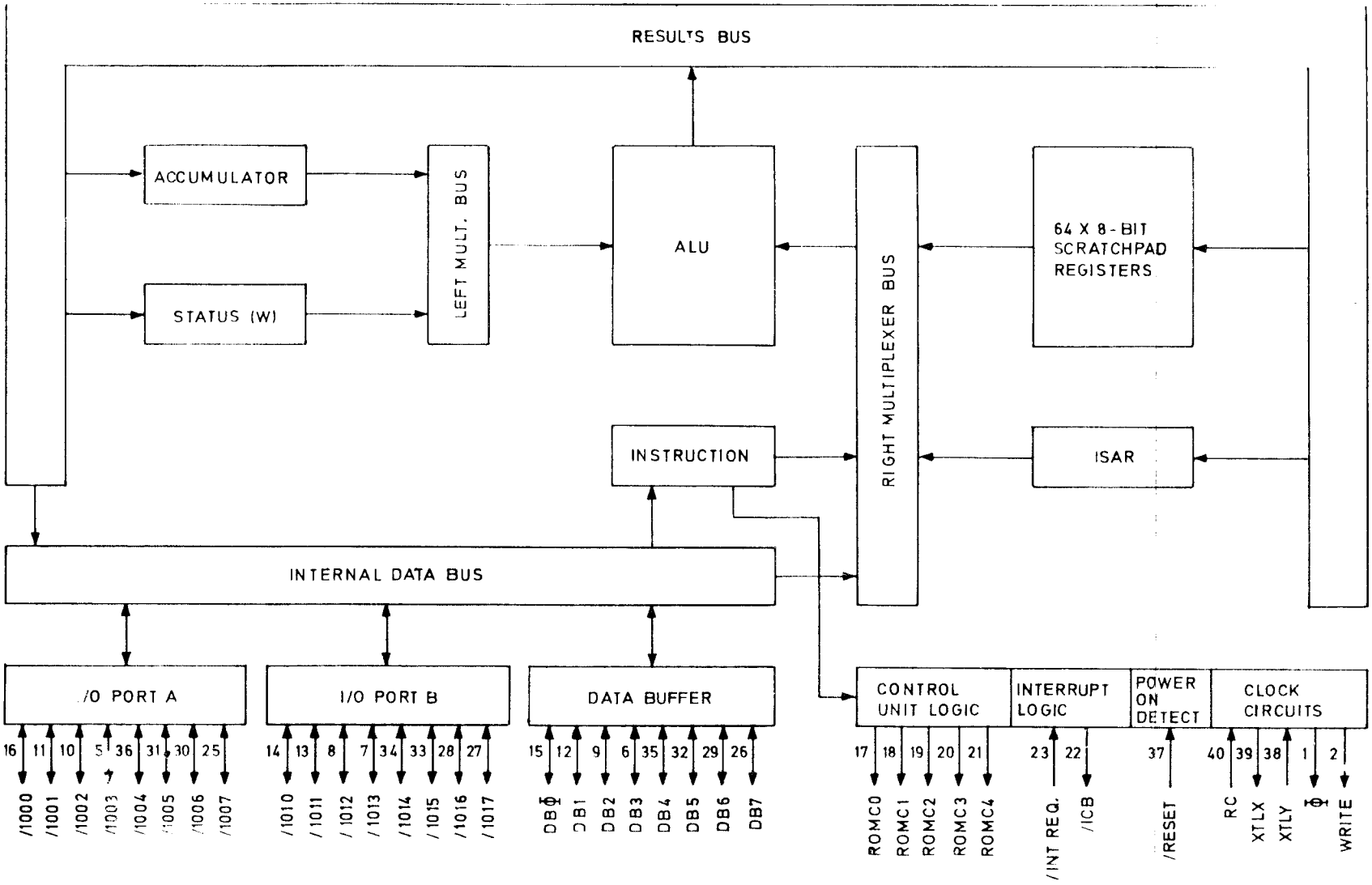
(3) The second suffix (A in this example) defines the type of ROM device.

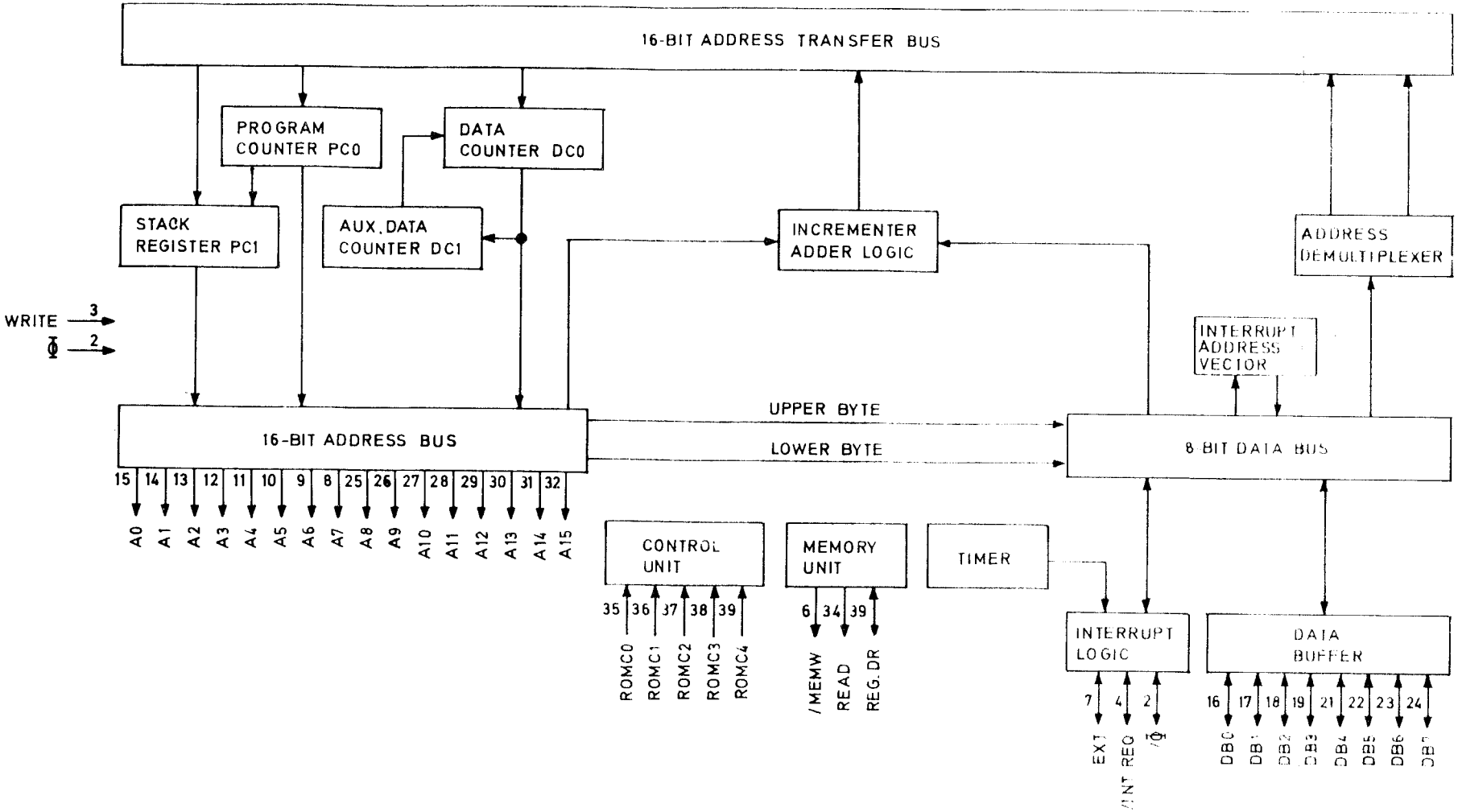
(4) Iss. denotes the program issue number (1 in this example).

(5) dddd is the date code.

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R1 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R2 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R3 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R4 | 2k2 | Metal Oxide | ¼ | 2 | 916546 |
| R5 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R6 | 1k8 | Metal Oxide | ¼ | 2 | 911148 |
| R7 | 4k7 | Metal Oxide | ¼ | 2 | 913490 |
| R8 | 82 k | Metal Oxide | ¼ | 2 | 915189 |
| R9 | 47 k | Metal Oxide | ¼ | 2 | 913496 |
| R10 | | Not Used | | | |
| R11 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R12 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R13 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R14 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R15 | 4k7 | Metal Oxide | ¼ | 2 | 913490 |
| R16 | 100 k | Metal Oxide | ¼ | 2 | 915190 |
| R17 | 1.2 k | Metal Oxide | ¼ | 2 | 911179 |
| **Capacitors** | | | | | |
| | µF | | V | | |
| C1 | 15 p | Ceramic | 500 | 5 | 938522 |
| C2 | 15 p | Ceramic | 500 | 5 | 938522 |
| C3 | 1.0 | Ceramic | 50 | 20 | 938401 |
| C4 | 100 n | Ceramic | 50 | 20 | 938406 |
| C5 | 100 n | Ceramic | 50 | 20 | 938406 |
| C6 | 100 n | Ceramic | 50 | 20 | 938406 |
| C7 | 100 n | Ceramic | 50 | 20 | 938406 |
| C8 | 100 n | Ceramic | 50 | 20 | 938406 |
| C9 | 100 n | Ceramic | 50 | 20 | 938406 |
| C10 | 1 n | Ceramic | 50 | 20 | 938408 |
| C11 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C12 | 100 n | Ceramic | 50 | 20 | 938406 |
| C13 | 10 n | Ceramic | 50 | 20 | 938053 |
| C14 | 10 n | Ceramic | 50 | 20 | 938053 |
| C15 | 10 n | Ceramic | 50 | 20 | 938053 |
| C16 | 100n | Ceramic | 50 | 20 | 938406 |
| C17 | 10 | Tantalum | 16 | 20 | 923569 |
| **Diodes** | | | | | |
| CR1 | LED | MV5074B | | | 931291 |
| CR2 | LED | MV5074B | | | 931291 |
| CR3 | | Not Used | | | |
| CR4 | | Silicon 1N 4149 | | | 914898 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Transistors** | | | | | |
| Q1 | | Silicon NPN 2N 2222A | | | 923217 |
| Q2 | | Silicon NPN BC109 | | | 914900 |
| Q3 | | Silicon PNP BFX48 | | | 915231 |
| **Connectors** | | | | | |
| J1 | | Plug, 34-way | | | 938524 |
| J2 | | Plug, 2 x 25-way | | | 943282 |
| **Integrated Circuits** | | | | | |
| U1 | | 74LS10 Triple 3-Input NAND gate | | | 938530 |
| U2 | | 3850 CPU | | | 938526 |
| U3 | | 74LS02 Quad 2-Input NOR gate | | | 938531 |
| U4 | | 3853 SMI | | | 938527 |
| U5 | | 74LS04 Hex Inverter | | | 938532 |
| U6 | | 74LS374 Octal Latch | | | 938533 |
| U7 | | 74LS139 Dual 1-of-4 decoder | | | 938528 |
| U8 | | 2532 4k x 8 ROM | | | 939343 |
| U9 | | 2532 4k x 8 ROM | | | 939343 |
| U10 | | 74LS245 Octal Transceiver | | | 938529 |
| U11 | | 445L 1024 x 4 Static RAM | | | 938038 |
| U12 | | 445L 1024 x 4 Static RAM | | | 938038 |
| U13 | | 14503 Hex Buffer | | | 931004 |
| U14 | | ZN423 Precision Voltage Refernce | | | 939905 |
| U15 | | 4076 Quad C-MOS Latch | | | 931000 |
| U16 | | LM393 Dual Comparator | | | 939906 |
| U17 | | 22k S.I.L. Resistor Pack | | | 934360 |
| **Miscellaneous** | | | | | |
| Y1 | | Crystal, 2 MHz | | | A07621 |
| BT1 | | Battery, NI-CAD 2.4 V | | | 941649 |
| | | 24 pin DIL IC socket | | | 938534 |
| | | 40 pin DIL IC socket | | | 938646 |


RESULTS BUS
ACCUMULATOR
STATUS (W)
LEFT MULT. BUS
ALU
RIGHT MULTIPLEXER BUS
64 X 8-BIT SCRATCHPAD REGISTERS
INSTRUCTION
ISAR
INTERNAL DATA BUS
I/O PORT A
I/O PORT B
DATA BUFFER
CONTROL UNIT LOGIC
INTERRUPT LOGIC
POWER ON DETECT
CLOCK CIRCUITS
16 11 10 5 36 31 30 25
/1000 /1001 /1002 /1003 /1004 /1005 /1006 /1007
14 13 8 7 34 33 28 27
/1010 /1011 /1012 /1013 /1014 /1015 /1016 /1017
15 12 9 6 35 32 29 26
DBΦ DB1 DB2 DB3 DB4 DB5 DB6 DB7
17 18 19 20 21
ROMC0 ROMC1 ROMC2 ROMC3 ROMC4
23 22
/INT REQ. /ICB
37
/RESET
40 39 38 1 2
RC XTLX XTLY Φ WRITE


16-BIT ADDRESS TRANSFER BUS
PROGRAM COUNTER PC0
DATA COUNTER DC0
STACK REGISTER PC1
AUX. DATA COUNTER DC1
INCREMENTER ADDER LOGIC
ADDRESS DEMULTIPLEXER
WRITE
3
2
INTERRUPT ADDRESS VECTOR
UPPER BYTE
LOWER BYTE
16-BIT ADDRESS BUS
8-BIT DATA BUS
15 14 13 12 11 10 9 8 25 26 27 28 29 30 31 32
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
CONTROL UNIT
MEMORY UNIT
TIMER
35 36 37 38 39
ROMC0 ROMC1 ROMC2 ROMC3 ROMC4
6 34 39
/MEMW READ REG.DR
INTERRUPT LOGIC
DATA BUFFER
7 4 2
EXT /INT REQ
16 17 18 19 21 22 23 24
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7