August 27, 1990

PROTOTYPE

TECHNICAL MANUAL

FOR

R-110 RECEIVER

DRAFT 2

THIS MANUAL IS INTENDED FOR USE WITH

THE FOLLOWING SERIAL NUMBERS:

_____ thru _____

DYNAMIC SCIENCES, INC
9655 Irondale Ave.
Chatsworth, CA 91311-5009

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FACTORY ACCEPTANCE TEST PROCEDURE FOR R-110 FTTR RECEIVER

TP493000

1. SCOPE

Outlined in this test procedure are steps necessary to ensure the prototype Model R-110 FTTR Receiver meets requirements in accordance with the referenced documents.

2. REFERENCED DOCUMENTS

2.1 Customer Documents

FTTR Specification (part of Statement-Of-Work)

2.2 DSI Documents

SRR Minutes, August 31, 1989
PDR Minutes, October 10, 1989
CDR Minutes, March 3, 1990
R-110 Receiver Specification, March 5, 1990

3. STANDARD TEST CONDITIONS

The tests shall be performed under the following standard conditions:

Temperature	75 ± 10 degrees F
Altitude	0 to 3000 feet
Humidity	10 to 90 %
Line Voltage	115 ± 3 vac

4. TEST PROCEDURES

The tests shall be conducted with the receiver assembled and its cover installed. Refer to Figures 1 and 2 for the location of front and rear panel controls and connectors.

The test equipment shall be energized and allowed to stabilize for at least 2 hours prior to initiating the tests.

Test results are to be recorded on the attached data sheets. All specifications and acceptable limits are defined on the appropriate data sheet.

4.1 EQUIPMENT REQUIRED

4.1.1 Commercial Test Equipment

NAME	MANUFACTURER	MODEL NO.
Dual Directional Coupler	Hewlett Packard	778D
Spectrum Analyzer	Tektronix	7L14
Main Frame	Tektronix	7603
Tracking Generator	Tektronix	501
Frequency Counter	Tektronix	509
Signal Generator	HP	8662
Function Generator	Tektronix	FG501
Digital Multimeter	Fluke	8600A
Volt/Ohmmeter	Triplet	630NS
Broadband Sampling VM	HP	3406A
Oscilloscope	Tektronix	4465A
Storage Oscilloscope	HP	54110D
Signal Generator	HP	3325A
MW Frequency Counter	HP	5342A
Impulse Generator	DSI	I-1700
Power Meter	HP	HP-435A
Power Amplifier	(any)	
Scale, 50 lbs max.	(any)	
Headphone	(any)	
Power Transformer	(any)	
AC Power Supply	(any)	
Termination, BNC, 50 ohm	(any)	
Tee, BNC	(any)	

Figure 1 R-110 FTTR Receiver Front Panel

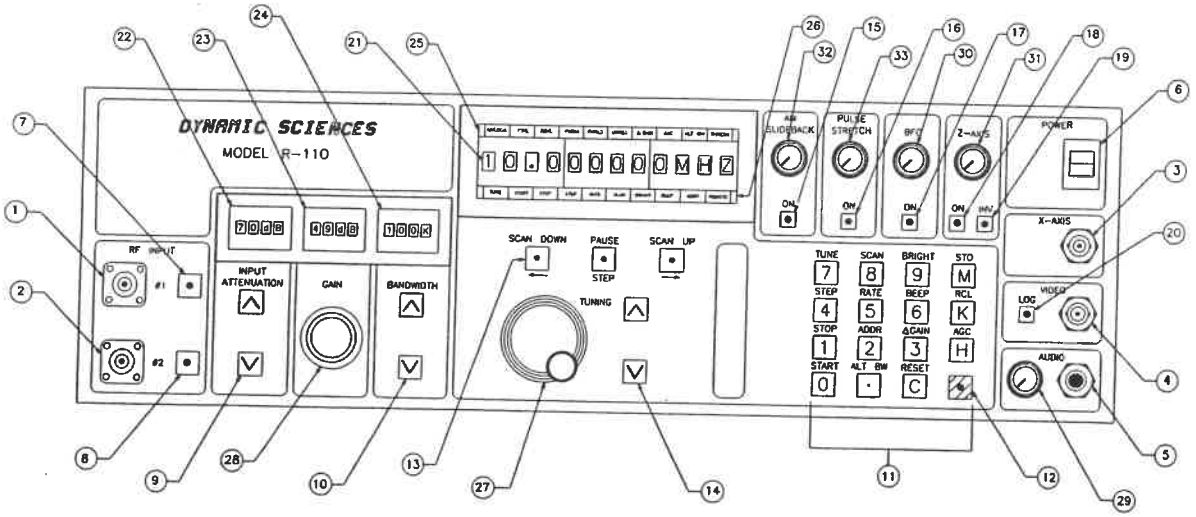
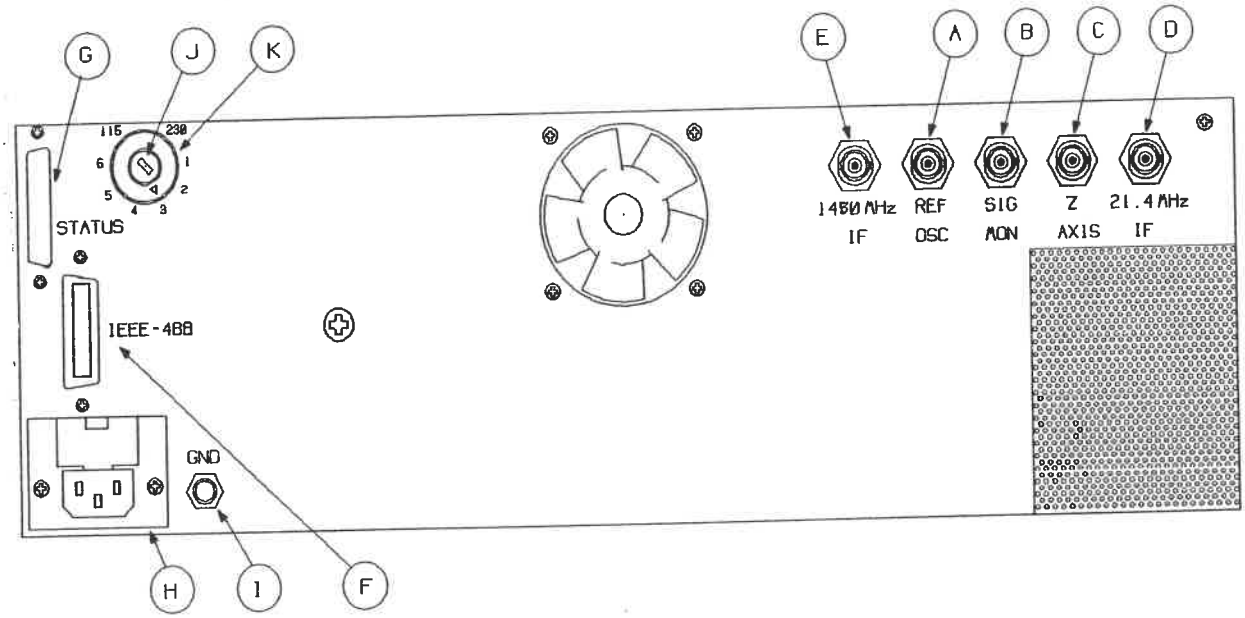


Figure 2 R-110 FTTR Receiver Rear Panel



4.1.2 DSI Test Fixtures

HF Directional Coupler	SK11001
Combiner Network	SK11002
Modulator	SK11003

4.2 TEST SETUP

4.2.1 Basic Test Set-up

The basic set-up used for a major portion of the tests is shown in Figure 3. The HP 8662 Signal Generator is connected to the receiver's RF Input #1. The Tektronix 4465A oscilloscope is connected to the video output, and the Tektronix 7L14 spectrum analyzer to the IF output. Special test set-ups are used for the balance of the tests; these are described in the procedures.

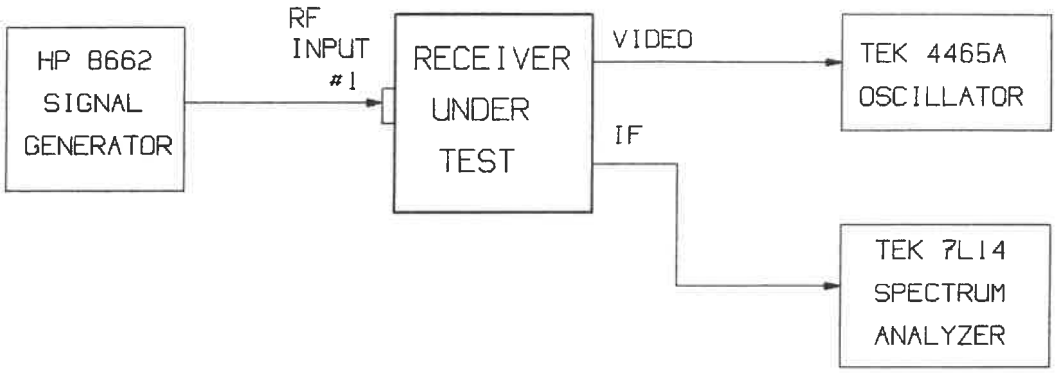


Figure 3 Basic Test Set-up

4.3 TEST PROCEDURES

4.3.1 Physical Audit

The physical audit verifies compliance with the physical and mechanical requirements of the FTTR specification, encompassing paragraphs *4.3.1 Mechanical, 4.3.2 Panel Controls and Connectors, 4.3.2.1 Front Panel, 4.3.2.2 Rear Panel, 4.3.3.8.d Shielded Power Cord, 4.3.3.8.f Line Voltage Select, and 4.5 Size and Weight.*

4.3.1.1 Visual Inspection

Visually examine the receiver and record the status on the Physical Audit Data Sheet.

4.3.1.2 Weight Measurement

Using the scale, weigh the fully assembled receiver and record the weight on the Data Sheet.

4.3.1.3 Size Measurement

Using suitable ruler(s), measure the dimensions of the fully assembled receiver. Record measurements on the Data Sheet.

4.3.2 Operational Tests

The operational test verifies the operational requirements delineated in the following paragraphs of the SOW:

4.3.3.1	*Modes of Operation*
4.3.3.2	*Detection Modes*
4.3.3.3.a	*RF Inputs, Two, Selectable*
4.3.3.3.b	*RF Inputs, tunable range*
4.3.3.3.c	*Input Selection and Termination*
4.3.3.4.a	*Tuning Range*
4.3.3.4.c	*Tuning Schemes*
4.3.3.4.d	*Tuning Resolution*
4.3.3.4.e	*Up/Down Tuning Resolution*
4.3.3.4.f	*Displayed Tuned Frequency*
4.3.3.4.h	*Synthesizer Step Noise in Outputs*
(new)	*Scan Mode*

4.3.2.1 Set-up for Operational Tests

Connect the power cable to receptacle at the rear of the receiver and to the 115 vac power source. Record the test conditions on the data sheet.

4.3.2.2 Knob Alignment

Align the following control knobs so the indicator pointers are at their maximum CCW positions. Record on data sheet.

a. AM Slideback
b. AM Pulse Stretch
c. Z axis
d. BFO Control
e. Audio

NOTE: The circuits for the AM Slideback and AM Pulse stretch functions are not installed in the prototypes, but their controls are included. Setting the controls full CCW does not effect receiver operation but is to be done to insure uniformity in the set-up.

4.3.2.3 Start-up and Initialization

(a) Turn power on; observe that the TUNE light-bar indicator (located adjacent to the frequency display) is illuminated. Record.

(b) Observe if any of the light-bar indicators listed below are illuminated. If so, terminate the test and correct the problem. Record corrective actions taken. Otherwise, proceed with the test.

UNLOCK
RFOVL
IF/DET OL
UNREG

(c) Observe if either the "PWRHI" or "PWRLO" lightbars are illuminated (or both). If so, check the line voltage. Record. If line voltage is satisfactory and either lightbar remains on, terminate the test and correct the problem. Record corrective actions taken. Otherwise, proceed with the test. If the line voltage is high or low, rotate the Power Range Selector switch on the rear panel as required.

(d) Reset Receiver to Standard Test Conditions

NOTE: The receiver's default conditions can be changed by the operator. The following steps are to be performed to return the receiver to its "standard" default settings.

Using keypad, press FNT key (12); press RESET key (key "C"). Record.

Press FNT key (12); press BEEP key (key "6"). Verify that the BEEP light-bar illuminates. Use PAUSE/STEP pushbutton (13) to activate Beeper. Record. Exit the adjustment mode by pressing the TUNE key (key "7").

(e) Observe that the front panel displays are illuminated and indicate the following default values. Record.

Frequency Display:	100 MHz
Input Attenuation Display:	20 dB
Gain Display:	0 dB
Bandwidth Display:	1 MHz

(f) Allow a 10 minute warm up before proceeding. Record.

4.3.2.4 Input Operation

(a) Connect the HP 8662 signal generator to the RF Input #1 connector. Set the generator's frequency to 100 KHz and the output to -50 dBm. Connect a 50 ohm terminator to RF Input #2. Connect the spectrum analyzer to the IF output connector on the receiver's rear panel.

(b) Verify the indicator LED in RF Input #1's pushbutton is illuminated (if not, press the pushbutton to activate). Set the input attenuation display to 0 dB, select the 10 KHz bandwidth, and tune the receiver to 100 KHz.

(c) Set the receiver's gain display to 20 dB with the gain pushbuttons (9). Adjust the analyzer controls for a mid-scale signal level with the analyzer in the 2 dB log position. Record the analyzer measurement. Move the cable from RF Input #1 to RF Input #2, connecting the terminator to RF Input #1. Measure the IF signal with the analyzer. Record. Depress RF Input #2's pushbutton and confirm that its LED illuminates. Record the analyzer's measurement.

4.3.2.5 Display Tests

4.3.2.5.1 Input Attenuation Display

(a) Briefly depress the "up" input attenuation pushbutton (9). Observe the display and record value. Continue to briefly depress, recording the value. When the maximum attenuation (70 dB) is reached, observe that the next depression of the pushbutton causes the display to indicate AUTO. Repeat the process using the "down" pushbutton. Observe that the beeper sounds when the pushbutton is depressed when the attenuation display is at 0 dB. Record.

4.3.2.5.2 Bandwidth Display

(a) Briefly depress the "up" bandwidth pushbutton (10). Observe the display and record value. Continue to briefly depress, recording the value. When the maximum bandwidth (15 MHz) observe that the next depression of the pushbutton causes the beeper to sound. Repeat the process using the "down" pushbutton. Observe that the beeper sounds if pushbutton is depressed when the bandwidth display is at 500 Hz. Record.

4.3.2.5.3 Frequency Display and Tuning

(a) Enter the data sheet's test frequencies (with decimal point) using keypad (11), followed by H, K, or M (Hz, KHz, or MHz). Record if display reads properly.

999.9 MHz
888.88 KHz
7777.7 Hz

4.3.2.6 Tuning Tests

(a) Adjust tuning resolution (indicated by flashing digit) in frequency display (21) by pressing left (13L) arrow pushbutton; select the left-most digit. Turn rotary tuning control (27) CW and ensure that each digit tunes 1 through 9 when the tuning knob is turned. Repeat using tuning pushbuttons (14). Record. Repeat for each digit.

4.3.2.7 Display Brightness

(a) Select display brightness adjust mode by pressing the FNT key (12) and then the BRIGHT key (key "9"). Verify that the BRIGHT light-bar illuminates. Use right/left arrow (13) keys to adjust brightness from maximum to minimum. Record. Exit the adjustment mode by pressing the TUNE key (key "7").

4.3.2.8 Audible Alarm

(a) Connect the headphone to the phone jack, and set the audio level control to its mid-position.

(b) Select the audible alarm adjust mode by pressing the FNT key (12) and then the BEEP key (key "6"). Verify that the BEEP light-bar illuminates. Use right/left arrow (13) keys to adjust loudness from maximum to minimum. Record. Exit the adjustment mode by pressing the TUNE key (key "7").

4.3.2.9 Synthesizer Step Noise in Outputs

(a) Set the receiver bandwidth to 10 Khz and the gain control to the minimum setting (turn CCW). Set the tuning resolution to the 10 KHz digit. Tune the receiver to the first start frequency shown in the data sheet.

(b) Using the headphones, monitor the audio output as the receiver is slowly tuned (using the tuning knob) from the start frequency to the end frequency shown on the data sheet. Observe if audible noises are heard and record the frequencies. Verify that any noise noted is repeatable.

4.3.2.10 Scan Mode

(a) Connect the receiver as shown in the basic test set-up (Figure 3) with the HP 8662 signal generator cabled to the RF Input #1 connector. Set the generator's frequency to 100 KHz and the amplitude to -30 dBm. Connect the storage oscilloscope's vertical axis to the video output, and its horizontal axis to the X-axis output. Adjust the controls to display 0 to 10 vdc on both axes.

(b) Set the receiver's controls as follows:

Tuned Frequency	1 MHz
Input Attenuator	0 dB
Bandwidth	10 KHz
Gain	Maximum (turn CW to max.value)
RF Input #1	On

(c) Select the scan mode by pressing the FNT key (12) and then the SCAN key (key "8"). Verify that the SCAN light-bar illuminates.

(c) Enter the first start frequency shown on the data sheet by pressing the START key (key "0"). Verify that the START light-bar illuminates.

(d) Enter the stop frequency and step size in the same fashion, again verifying that the STOP and STEP light-bars illuminate correctly.

(e) Press the "Scan Up" (13c) to start the scan. Observe the oscilloscope display and note that the sweep shows the presence of a strong signal at the mid-point. When scan is complete record results.

(f) Press "Scan Down" key (13a) to again start the sweep, this time from the stop frequency back to the start frequency. Press the "Pause" key and verify that the scan pauses until the key is pressed again.

4.3.3 Transfer Function Tests

The transfer function test verifies the gain-related characteristics, including those of specification paragraph *4.3.3.5.b RF Gain Adjust* and DSI-provided features. The test evaluates (1) the accuracy and frequency characteristics of the attenuator, (2) the characteristics of the variable gain over the full frequency range at various bandwidths, (3) the AGC response, and (4) the Incremental Gain mode.

4.3.3.1 Input Attenuator

(a) Connect the HP 8662 signal generator to the RF Input #1 connector. Set the generator's frequency to 100 KHz and the amplitude to -30 dBm. Connect the power meter to the IF output connector.

(b) Set the receiver's controls as follows:

Tuned Frequency	100 KHz
Input Attenuator	0 dB
Bandwidth	50 KHz
Gain	Maximum (turn CW to max.value)
RF Input #1	On

(c) Observe the power meter's reading and record on data sheet for reference. Set the input attenuator to the 10 dB position and increase the generator's output by 10 dB using its decade attenuator. Record the change in the meter's reading; it should not change by more than 0.2 dB. Repeat this sequence for the input attenuator's 20 through 70 dB positions.

(d) Reset the R-110 and generator to the next frequency listed in the data sheet. Reset the receiver's input attenuator to 0 dB. Repeat test.

(e) Reset the R-110 and generator to the third frequency listed in the data sheet. Reset the receiver's input attenuator to 0 dB. Repeat test.

4.3.3.2 Variable Gain

(a) The test is performed using the same set-up as above. Set the generator's frequency to 100 KHz and the amplitude to -50 dBm.

(b) Set the receiver's attenuator to 0 dB. Set the bandwidth and gain controls as stated in the data sheet. Turn the RF control to the minimum (0 dB) setting. Record the power meter's indication of IF output amplitude.

(c) Adjust the RF control to the 10, 20, and 50 values, recording the IF output on the data sheet.

(d) Set the generator to the next frequency on the data sheet.

(e) Set the receiver to the next frequency and bandwidth values and repeat the measurements.

4.3.3.3 AGC Mode

(a) The test is performed using the same set-up as above. Set the generator's frequency to 100 KHz and the amplitude to -30 dBm.

(b) Set the receiver's attenuator to 0 dB, the bandwidth to 10 KHz, and the gain display to 20. Record the IF output reading.

(c) Select the AGC mode. Record the IF output reading. Reduce the generator's signal level to -50 dBm. Record the amplitude reading. Determine the differency between the readings (it must be within the range shown). Return the generator's level to -30 dBm.

(d) Connect the storage oscilloscope to the video output. Store the transient when the generator's level is step-changed from -30 to -25 dBm. Estimate and record the time constant. Repeat, changing the level from -25 to -30 dBm. De-select the AGC mode by pressing the TUNE key (key "7").

4.3.3.4 Incremental Gain Mode

(a) The test is performed using the same set-up as above. Set the generator's frequency to 100 KHz and the amplitude to -30 dBm.

(b) Set the receiver's attenuator to 0 dB, the bandwidth to 10 KHz, and the gain display to 20. Record the analyzer's amplitude reading.

(c) Select the Incremental Gain mode by pressing the FNT key (12) and then the △ GAIN key (key "3"). Verify that the △ GAIN light-bar illuminates. Record the Gain display reading (it should be zero). Reduce the generator's signal level to -50 dBm using the decade switch. Increase the gain control to achieve the same amplitude reading on the analyzer. Record the Incremental Gain indication.

(d) De-select the Incremental Gain mode by pressing the TUNE key (key "7"). Set the gain display to 20. Record the analyzer's amplitude reading. Re-select the Incremental Gain mode. Increase the signal generator's level from -50 dBm to -10 dBm by decades. Adjust the receiver's attenuator to return the analyzer to as close as possible its previous indication. Record the Incremental Gain indication. De-select the Incremental Gain mode.

4.3.4 IF Tests

These tests verify the IF-related requirements for specification paragraphs *4.3.3.6.a IF Selectivity, 4.3.3.6.c IF Bandwidths, 4.3.3.6.d IF Bandwidth Selection, 4.3.3.7.d IF Output Level, and 4.3.3.7.f Signal Monitor*. The main purpose of this test is to measure the shape factor of the IF filters which determine the receiver's selectivity. Because the receiver utilizes both fixed and variable (DCIF) filters, two separate procedures are used. The test exercises both the "default" and "alternate" DCIF filter sets.

4.3.4.1 IF Selectivity (Fixed Filters)

(a) Connect the receiver as shown in the basic test set-up (Figure 3) with the HP 8662 signal generator cabled to the RF Input #1 connector. Set the generator's frequency to 100 MHz and the amplitude to -30 dBm.

(b) Set the receiver's controls as follows:

Tuned Frequency	100 MHz
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	Per data sheet

(c) Adjust the spectrum analyzer to produce a mid-screen display. Record the signal generator output level and the analyzer's amplitude reading.

(d) Increase and decrease the signal generator frequency from the preset point in order to find the frequencies at which the analyzer's power reduces by 6 dB. Record the frequency of these two points on the data sheet. Calculate the difference between these points and enter this value on the data sheet under 6 dB BW. The calculated bandwidth must be within the range shown in the MIN MAX column.

(e) Repeat the steps of (C), to find the 60 dB frequencies. Record the frequency of these two points on the data sheet. Calculate the difference between these points and enter this value on the data sheet under 60 dB BW.

(f) Repeat the steps above for all bandwidths listed on the data sheet.

4.3.4.2 IF Selectivity (DCIF Filters)

(a) Set the HP 8662 signal generator's frequency to 100 KHz and the amplitude to -30 dBm. Record. Monitor the video output with the oscilloscope.

(b) Set the receiver's controls as follows:

Tuned Frequency	100 KHz
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)

RF Input #1	On
Bandwidth	Per data sheet

(c) Adjust the signal generator's level to produce a 3 vdc video output; adjust the oscilloscope to obtain as nearly full-scale presentation as can be achieved with calibrated settings. Record the signal generator output level and the oscilloscope's amplitude reading.

(c) Increase and decrease the signal generator frequency from the preset point to find the frequencies at which the oscilloscope's display decreases to 1.5 vdc. Record the frequency of these two points on the data sheet. Calculate the difference between these points and enter this value on the data sheet under 6 dB BW.

(d) Repeat the steps of (C), to find the 60 dB frequencies. This will require increasing the signal generator's level and the oscilloscope's sensitivity as the filter attenuates the signal. Increase the generator's level to -60 dBm using the decade switch as the 60 dB frequency is approached, and increase the oscilloscope's sensitivity by 10. Record the frequency of the two points on the data sheet. Calculate the difference between these points and enter this value on the data sheet under 60 dB BW.

(e) Repeat the steps above for all of the default DCIF bandwidths listed on the data sheet.

(f) Select the Alternate Bandwidth mode by pressing the FNT key (12) and then the ALT BW key (key "."). Verify that the ALT BW light-bar illuminates. Repeat the steps above for the alternative DCIF bandwidths listed on the data sheet. De-select the Alternate Bandwidth mode by pressing the TUNE key (key "7").

4.3.4.3 IF Output Level

(a) Set the HP 8662 signal generator's frequency to 100 MHz and the amplitude to -30 dBm. Monitor the IF output with the power meter.

(b) Set the receiver's controls as follows:

Tuned Frequency	100 MHz
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	1 MHz

(c) Adjust the signal generator's level until the RF or IF/DET overload indicators illuminate. Record the level.

(d) Read and record the power meter's amplitude reading.

4.3.4.4 Signal Monitor

(a) Connect the HP 8662 signal generator to the RF Input #1 connector. Set the signal generator's frequency to 100 MHz and the amplitude to -30 dBm. Connect the spectrum analyzer to the signal monitor connector.

(b) Set the receiver's controls as follows:

Tuned Frequency	100 MHz
Input Attenuator	0 dB
Gain	Maximum (turn CW to max. value)
RF Input #1	On
Bandwidth	15 MHz

(c) Measure and record the frequency of the sinal monitor output with the specrum analyzer.

(d) Adjust the signal generator's level to equal -107 dBm. Set the spectrum analyzer's bandwidth to 3 KHZ and record the amplitude.

(e) Connect the HP 8662 signal generator to the input port of the modulator. Connect the Tektronix FG501 Function Generator to the modulation port of the modulator. Connect the modulator's output port to the RF Input #1 connector. Reset the generator's level to -30 dBm. Set the function generator's frequency to its 1 KHz and its level to -50 dBm.

(f) Record the peak amplitude of either the upper or lower sidebands displayed by the spectrum analyzer. Increase the function generator's frequency until the amplitude of the sideband decreases by 3 dB. Record the function generator's frequency.

4.3.5 Noise Figure Tests

This test verifies the noise figure characteristics in accordance with paragraph *4.3.3.5.a Noise Figure.*

(a) Connect the HP 8662 signal generator to the RF Input #1 connector, and the HP-435A Power Meter to the IF output connector. Set the generator's frequency as indicated on the data sheet and the amplitude to the minimum.

(b) Set the receiver's controls as follows:

Tuned Frequency	Per data sheet
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	Per data sheet

(c) Adjust the power meter to a range that gives an indication of the noise level present at the IF output of the receiver.

(d) Slowly increase the generator's level until the power meter's indication increases by 3 dB. Record the generator's output level on the data sheet under the 3 dB SENSITIVITY column.

Subtract the THEORETICAL NOISE FLOOR value from the 3 dB SENSITIVITY. This difference is the noise figure to be recorded on the data sheet.

(e) Repeat this procedure for each of the bandwidths and associated frequencies indicated on the data sheet.

4.3.6 Image and IF Rejection Test

This test verifies the image and IF rejection characteristics of specification paragraph *4.3.3.6.b IF and Image Rejection.*

(a) Connect the receiver as shown in the basic test set-up (Figure 3) with the HP 8662 signal generator cabled to the RF Input #1 connector. Set the generator's frequency as indicated on the data sheet and the amplitude to the -50 dBm.

(b) Set the receiver's controls as follows:

Tuned Frequency	Per data sheet
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	Per data sheet

(c) Adjust the spectrum analyzer to produce a mid-screen display. Record the signal generator output level and the analyzer's amplitude reading.

(d) Set the signal source to a frequency which equals the tuned frequency plus twice the IF frequency, as shown on the data sheet. Increase the signal source amplitude until the IF output equals the previous level. Record the signal generator's level, and calculate the image rejection (equal to the difference in the signal generator's levels). Determine if the rejection meets the requirement.

(e) Set the signal generator set to the IF frequency for each band as indicated on the second page of the data sheet. Increase the signal source amplitude until the IF output equals the previous level. Record the signal generator's level, and calculate the IF rejection.

(f) Repeat the measurements for the other conditions in the data sheet.

4.3.7 AM Dynamic Range Tests

The basic set-up is used to determine the AM Video and AM Log dynamic ranges using the procedure for paragraph *4.3.3.5.c Spur-free Dynamic Range (RF Input to AM/Video) and 4.3.3.7.b AM Log.*

(a) Connect the signal generator to the RF Input #1 connector. Connect the oscilloscope and the power meter to the video connector, using a "T". Set the generator's frequency to 100 KHz and the level as indicated on the data sheet.

(b) Set the receiver's controls as follows:

Tuned Frequency	100 KHz
Input Attenuator	0 dB
Gain	Minimum (turn CCW to min.value)
RF Input #1	On
Bandwidth	10 KHz

(c) Increase the receiver's gain control until noise is observed on the oscilloscope. Slight decrease the gain to obtain a low-noise display. Record the power meter's reading in the LIN column. Press the Log pushbutton. Readjust the gain control for a low-noise display and record the power meter reading in the LOG column.

(d) Change the signal generator level per the data sheet, and record the linear and log readings as above.

(e) Enter the logarithm of the linear readings in the "LIN (log)" column, and plot the logarithms as a function of the signal generator level on the second page of the data sheet. Determine the 1 dB linear range and calculate the linear dynamic range.

(f) Plot the data in the LOG column vs. the signal generator level on the third page of the data sheet. Again determine the 1 dB points and calculate the log dynamic range.

4.3.8 IDR Tests

This test verifies the instantaneous dynamic range (IDR) meets the requirements of paragraph *4.3.3.5.d Spur-free Dynamic Range (RF Input to IF).*

(a) Connect the HP 8662 signal generator (A) to the #1 port of the combiner network. Connect the Tektronix FG501 Function Generator (B) to the #2 port. Connect the combiner network's output port to the RF Input #1 connector. Connect the spectrum analyzer to the IF output connector. Set the generator's frequencies as indicated in the A and B columns on the data sheet.

(b) Set the receiver's controls as follows:

Tuned Frequency	Per data sheet
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	Per data sheet

(c) Adjust the spectrum analyzer controls to produce a mid-screen display. Observe the analyzer and equally adjust the levels of the signal sources until the third order intermodulation products are 3 dB above the noise floor. Record the levels in the SIG.GEN.LEVEL column on the data sheet.

(d) Calculate the IDR as shown in the data sheet and record the value.

(e) Repeat the process for the data sheet's other test conditions.

4.3.9 Input Tests

These tests verify the input characteristics in accordance with paragraphs *4.3.3.3.d Input Isolation, 4.3.3.3.f Input Impedance and VSWR, 4.3.3.3.g Maximum Tolerated RF Input, and 4.3.3.8.b LO Re-radiation.*

4.3.9.1 Input Isolation

(a) Connect the HP 8662 signal generator to the RF Input #1 connector and the spectrum analyzer to the RF Input #2 connector. Set the generator's frequency and amplitude as indicated on the data sheet.

(b) Set the receiver's controls as follows:

Tuned Frequency	Per data sheet
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	Per data sheet

(c) Increase the generator's output until an adequate reading is obtained with the spectrum analyzer. Record both the signal generator's level and the spectrum analyzer's amplitude reading.

(d) Set the generator frequency to the other values on the data sheet and repeat the test.

(e) Calculate the isolation and record on data sheet

4.3.9.2 LO Re-radiation

(a) Connect the spectrum analyzer to the RF Input #1 connector.

(b) Set the receiver's controls as follows:

Tuned Frequency	Per data sheet
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	Per data sheet

(c) Adjust the spectrum analyzer and record the analyzer's amplitude reading in the LO RE-RADIATION column on the data sheet.

(d) Tune the receiver to the other frequencies on the data sheet and repeat the measurement.

4.3.9.3 Input Impedance and VSWR

(a) Connect the HF directional coupler between the TEK 501 tracking generator and the receiver's RF Input #1. Verify that RF Input #1 is selected. Connect the spectrum analyzer to the test output of the coupler. Set the tracking generator's frequency and the analyzers frequency-span per the data sheet.

(b) Tune the receiver per the data sheet, and set the input attenuator to 0 dB.

(c) Observe and store the analyzer's display of the return loss. Disconnect the cable from the receiver. Again observe the analyzer's display. Recall the stored display and determine the difference between the new and stored displays; record results on the data sheet in the RETURN LOSS column. The return loss must be greater than 9.5 dB at the nominal input impedance of 50 ohms. Set the receiver's attenuator to 30 dB and repeat the test.

(d) Repeat the test at the other frequencies in the data sheet, substituting the dual directional coupler where indicated.

4.3.9.4 Maximum Tolerated RF Input

(a) Connect the power amplifier between the HP 8662 signal generator and the power meter (use the high power head). Set the generator to 100 KHz and adjust the generator's level while monitoring the power meter. Record the generator setting required for a 30 dBm reading on the power meter. Reduce the generator level so the power meter reads -20 dBm. Record the generator setting.

(b) Connect the output of the power amplifier to RF Input #1. Verify that RF Input #1 is selected.

(c) Verify operation of the receiver is normal by selecting different bandwidths and changing the attenuator and gain settings. Record results. Reset the input attenuator to 0 dB and the RF Gain to maximum.

(d) Increase the generator's level to the value required for a 30 dBm input. Maintain this input for 1 minute. Reduce the input to -20 dBm. Verify operation of the receiver is normal. Record results.

(e) Set the input attenuator to 30 dB and the RF Gain to maximum. Increase the generator's level to the value required for a 30 dBm input. Maintain this input for 1 minute. Reduce the input to -20 dBm. Verify operation of the receiver is normal. Record results.

4.3.10 IF Impulse Response Tests

This test verifies impulsive response characteristics of the IF in accordance with paragraph *4.3.3.6.e IF Bandwidth Impulse Response*. Two test sequences are used: the first for the fixed IF filters, and the second for the DCIF's default filter set.

4.3.10.1 Fixed Filter Impulse Response

(a) Connect the impulse generator (IG) to the RF Input #1 connector. Connect the oscilloscope to the IF output connector. Set the IG repetition rate and level per the data sheet.

(b) Set the receiver's controls as follows:

Tuned Frequency	Per data sheet
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	Per data sheet

(c) Adjust the oscilloscope controls to produce a mid-screen display of a single pulse. Measure the peak amplitude of the response and record in the "A" column of the data sheet. Measure the peak-to-peak amplitude of the secondary ringing and record in the "a" column. Calculate the ratio (a/A) and record.

(d) Repeat the test for the remaining bandwidth in the data sheet.

4.3.10.2 DCIF Impulse Response

(a) Connect the impulse generator (IG) to the RF Input #1 connector. Connect the oscilloscope to the video output connector. Set the IG repetition rate and level per the data sheet.

(b) Set the receiver's controls as follows:

Tuned Frequency	Per data sheet
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	Per data sheet

(c) Adjust the oscilloscope controls to produce a mid-screen display of a single pulse. Measure the peak amplitude of the response and record in the "A" column of the data sheet. Measure the peak-to-peak amplitude of the secondary ringing and record in the "a" column. Calculate the ratio (a/A) and record.

(d) Repeat the test for the remaining bandwidths in the data sheet.

4.3.11 Frequency Accuracy and Stability

This test verifies that the receiver's frequency accuracy and stability are in accordance with paragraph *4.3.3.4.b Frequency Accuracy and Stability*. Because this test requires an extended power-off period, it should be performed when most convenient (i.e. first thing in the morning).

(a) Turn off the receiver and allow it to stabilize at room temperature for 8 hours. Do not turn on the receiver until step (c), below.

(b) Turn on the HP 8662 signal generator for at least 3 hours before the test. Connect the generator to the RF Input #1 connector. Set the generator's frequency to exactly 100 MHz using the keypad and the amplitude to -30 dBm. Connect the frequency counter to the IF output connector. Set the counter's controls to permit frequency measurements with a resolution of 0.1 Hz.

(b) Record the time and turn on the receiver; immediately set the receiver's controls as follows:

Tuned Frequency	100 MHz (use keypad)
Input Attenuator	0 dB
Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	1 MHz

(c) Read and record the frequency counter indication and the time of the measurement. Calculate the frequency accuracy by taking the difference between the measurement and the IF center frequency (21.4000000 MHz) and dividing the result by 21.4000000.

(d) Repeat the measurement and calculation every 5 minutes for the first 30 minutes, and at 15 minute intervals until two hours has elapsed.

(e) Determine the frequency stability by calculating the difference between the readings at each interval and the reading at the end of two hours and dividing the result by 21.4000000.

4.3.12 Output Tests

These tests verify the BFO operation and the characteristics of the AM video, AM Log, audio, and Z-axis outputs in accordance with paragraphs *4.3.3.6.g BFO Operation, 4.3.3.7.a Audio, 4.3.3.7.b AM Log, 4.3.3.7.c AM, and 4.3.3.7.e Z-axis.*

4.3.12.1 BFO operation

(a) Connect the HP 8662 signal generator to the RF Input #1 connector. Set the generator's frequency to 1 MHz sheet and the amplitude to the -50 dBm. Connect headphones to the audio phone jack.

(b) Set the receiver's controls as follows:

Tuned Frequency	1 MHz
Input Attenuator	0 dB

Gain	Maximum (turn CW to max.value)
RF Input #1	On
Bandwidth	20 KHz
BFO pushbutton	On

(c) Slowly adjust the signal generator frequency by less than 1 KHz form the 1 MHz setting. Adjust the audio gain control to provide a comfortable sound level. Confirm that the audio frequency changes smoothly as the signal generator is adjusted. Reset the signal generator to the initial frequency.

(d) Connect the frequency counter to the audio phone jack with an adapter. Record the indication (should be zero or a low frequency).

(e) Increase the signal generator frequency by exactly 4 KHz using the keypad. Record the counter's reading (should be 4 KHz).

(f) Adjust the signal generator frequency using a 1 Hz resolution. Confirm that the audio signal changes with the same resolution.

(g) Set the signal generator frequency to equal exactly 4 KHz less than the initial setting using the keypad. Record the counter's reading (should be 4 KHz).

(h) Press the BFO pushbutton to turn off BFO operation

4.3.12.2 AM Video Output

(a) Connect the HP 8662 signal generator to the RF Input #1 connector. Set the signal generator's frequency to 100 MHz and the amplitude to -30 dBm. Connect the oscilloscope (with a 50 ohm load) to the video connector.

(b) Set the receiver's controls as follows:

Tuned Frequency	100 MHz
Input Attenuator	0 dB
Gain	Minimum (turn CCW to min. value)
RF Input #1	On
Bandwidth	Per data sheet
LOG pushbutton	Off

(c) Record the DC video offset voltage present at the video connector at the bandwidth settings indicated on the data sheet.

(d) Return the receiver gain to the maximum setting (turn CW). Set the bandwidth to 15 MHz.

(e) Increase the signal generator output until the video reaches its maximum. Record the maximum DC value.

(f) Introduce the modulator between the signal generator and the receiver. Connect the Tektronix FG501 Function Generator to the modulation port of the modulator. Connect the

modulator's output port to the RF Input #1 connector. Set the HP 8662's frequency to 100 MHz and the amplitude to -30 dBm. Set the function generator's frequency to 100 KHz and its level to -10 dBm.

(g) Increase the function generator's level and observe the video signal with the oscilloscope. Adjust the level to obtain a 2 volt (peak) signal on the oscilloscope.

(h) Change the function generator's frequency per the data sheet and record the peak voltage indication on the oscilloscope at each setting.

(i) Plot the video data. Determine where the signal level decreases to 1 volt. Record as cut-off frequency value.

4.3.12.3 Z-axis

(a) Connect the HP 8662 signal generator to the input port of the modulator. Connect the Tektronix FG501 Function Generator to the modulation port of the modulator. Connect the modulator's output port to the RF Input #1 connector. Set the HP 8662 frequency to 100 MHz and the amplitude to -30 dBm. Set the function generator's frequency to 100 KHz and its level to -10 dBm. Connect the oscilloscope (with a 50 ohm load) to the Z-axis connector.

(b) Set the receiver's controls as follows:

Tuned Frequency	100 MHz
Input Attenuator	0 dB
Gain	Maximum (turn CW to max. value)
RF Input #1	On
Bandwidth	15 MHz
Z-axis ON pushbutton	On
Z-axis INV pushbutton	Off

(c) Increase the signal and function generator's outputs in equal increments until the Z-axis output just starts to distort. Measure or calculate the maximum RMS voltage and record in the NORMAL column on the data sheet.

(d) Press the Z-AXIS INV pushbutton. Readjust the generator's outputs to obtain the inverted Z-axis output at the distortion point. Record the maximum RMS voltage in the INVERTED column on the data sheet. Press the pushbutton to return to normal Z-axis operation.

(e) Return the HP 8662's level to -30 dBm, and decrease the function generator's level to obtain a 2 volt peak-peak signal on the oscilloscope.

(f) Change the function generator's frequency per the data sheet and record the peak voltage indication on the oscilloscope at each setting.

(g) Plot the Z-axis data. Determine where the signal level decreases to 1 volt. Record as cut-off frequency value.

(h) Press the pushbutton to turn off Z-axis operation

4.3.12.4 AM Log Output

(a) Connect the HP 8662 signal generator to the RF Input #1 connector. Connect the oscilloscope (with a 50 ohm load) to the video connector. Set the signal generator's frequency and amplitude per the data sheet.

(b) Set the receiver's controls as follows:

Tuned Frequency	Per data sheet
Input Attenuator	0 dB
Gain	Minimum (turn CCW to min. value)
RF Input #1	On
Bandwidth	10 KHz
Log Pushbutton	On

(c) Record the DC log offset voltage present at the video connector at the bandwidth settings indicated on the data sheet.

(d) Return the receiver gain to the maximum setting (turn CW). Set the bandwidth per the data sheet.

(e) Increase the signal generator output until the maximum level is obtained. Record the maximum DC level seen on the oscilloscope.

(f) Press the pushbutton to turn off Log operation

4.3.12.5 Audio Output

(a) Connect the HP 8662 signal generator to RF Input #1. Select 1 KHz 30% AM modulation. Set the signal generator's frequency to 100 KHz and the amplitude to -30 dBm. Terminate the audio jack with an 8 ohm 15 watt resistor and connect the oscilloscope across this resistor.

(b) Set the receiver's controls as follows:

Tuned Frequency	100 KHz
Input Attenuator	0 dB
Gain	Maximum (turn CW to max. value)
RF Input #1	On
Bandwidth	Per data sheet

(c) Adjust the audio output control until the audio viewed on the oscilloscope just starts to clip. Measure or calculate the RMS voltage and record on the data sheet. Readjust the audio control for 3 vpp.

(d) Set the modulation frequency to the values shown on the data sheet and record the p-p voltages.

(e) Determine and record the end-point frequencies where the voltage is 1.5 vpp.

(f) Turn the audio control full CCW.

4.3.13 Spurious Response Test

The test checks for spurs in accordance with paragraph *4.3.3.8.c Internally Generated Spurs.*

(a) Terminate the receiver's inputs with 50 ohms. Select a bandwidth of 500 Hz. Monitor the IF output with the spectrum analyzer.

(b) Tune the receiver per the data sheet from 1 KHz to 20 KHz. Record the frequency and amplitude of all spurious responses greater than 6 dB above the noise floor.

(c) Set the bandwidth to 10 KHz and tune the receiver through its full range per the data sheet. Record the frequency and amplitude of all spurious responses greater than 6 dB above the noise floor.

(d) Remove the 50 ohm termination and connect the HP 8662 signal generator to RF Input #1. Adjust the signal generator frequency to the first spur frequency recorded in the previous steps. Adjust the generator's level until the IF response is equal to the spur. Record the generator's level in the data sheet's INPUT LEVEL column.

4.3.14 Power Tests

The power tests verify the receiver will not be damaged by connection to a 230 vac source when the line switch is in its 115 vac setting, and determines the power consumption, in accordance with paragraphs *4.3.3.8.e No Damage by High Line Voltage, and 4.4 Power Requirements.* The power consumption is also checked.

4.3.14.1 High Line Voltage

(a) Set the receiver's line switch to 115 vac.

(b) Power the receiver from the tapped transformer. Set the transformer's output voltage to 115 vac.

(c) Connect the HP 8662 signal generator to RF Input #1. Select 1 KHz 30% AM modulation. Set the signal generator's frequency to 100 KHz and the amplitude to -30 dBm. Connect the oscilloscope to the video connector.

(d) Set the receiver's controls as follows:

Tuned Frequency	100 KHz
Input Attenuator	0 dB
Gain	Maximum (turn CW to max. value)

RF Input #1	On
Bandwidth	1 KHz

(e) Adjust the generator's level until the video viewed on the oscilloscope is 1 vpp.

(f) Exercise the receiver's controls to verify that operation is normal.

(g) Switch the transformer to output 230 vac. Observe if the receiver's line fuse(s) blow. If the fuses fail to blow and the receiver continues to operate, shut off the receiver and correct problem.

(h) Shut off power and replace the fuse(s). Set the transformer power to 115 vac and turn on the receiver.

(i) Confirm that the receiver operates properly using the video indication and by exercising the controls.

4.3.14.2 Power Requirements

(a) Set the receiver's line switch to 115 vac.

(b) Connect the receiver to the variable AC power supply. Set the output voltage to 115 vac and the frequency to 60 Hz.

(c) Connect the HP 8662 signal generator to RF Input #1. Select 1 KHz 30% AM modulation. Set the signal generator's frequency to 100 KHz and the amplitude to -30 dBm. Connect the oscilloscope to the video connector.

(d) Set the receiver's controls as follows:

Tuned Frequency	100 KHz
Input Attenuator	0 dB
Gain	Maximum (turn CW to max. value)
RF Input #1	On
Bandwidth	1 KHz

(e) Adjust the generator's level until the video viewed on the oscilloscope is 1 vpp. Exercise the receiver's controls to verify that operation is normal. Record.

(f) Record the AC Power Supply's voltage and current readings. Calculate and record the power consumption.

(g) Set the AC power supply's frequency to 48 Hz.

(h) Check the video signal and exercise the receiver's controls to verify that operation is normal. Record.

(i) Increase the frequency to 62 hz in 1 Hz steps. Check for normal operation at each step. Record. Set the frequency back to 60 Hz.

(j) Adjust the AC power supply's voltage to 127 vac. Observe if the PWRHI light-bar illuminates. Record.

(k) Rotate the receiver's power range switch to the high line setting (position 1). Observe if the PWRHI light-bar extinguishes. Record.

(l) Check the video signal and exercise the receiver's controls to verify that operation is normal. Record.

(m) Set the AC power supply's frequency to 48 Hz. Verify that operation is normal. Record.

(n) Set the AC power supply's frequency to 62 Hz. Verify operation is normal. Record. Reset the frequency to 60 Hz.

(o) Adjust the AC power supply's voltage to 102 vac. Observe if the PWRLO light-bar illuminates. Record.

(p) Rotate the receiver's power range switch to the low line setting (position 6). Observe if the PWRLO light-bar extinguishes. Record.

(q) Check the video signal and exercise the receiver's controls to verify that operation is normal. Record.

(r) Set the AC power supply's frequency to 48 Hz. Verify that operation is normal. Record.

(s) Set the AC power supply's frequency to 62 Hz. Verify operation is normal. Record.

5. TECHNICAL NOTES

TP493000

Prototype R110 FTTR Receiver

ACCEPTANCE TEST PROCEDURE

DATA SHEETS

Test Tech: _____

Inspector: _____

S.N. _____

Final
Test Date: _____

PHYSICAL AUDIT DATA SHEET
TEST PARAGRAPH 4.3.1

PROTOTYPE SERIAL NO. _____
DATE OF AUDIT _____
AUDIT CONDUCTED BY _____ WITNESSED BY _____

REQUIREMENT	YES	NO	SOW Para.
FRONT PANEL			
Dual BNC RF Input Connectors	___	___	4.3.2.1.a, 4.3.3.3.e (modified)
Dual RF Input Select Pushbuttons	___	___	4.3.2.1.b
BNC AM Output Connector	___	___	4.3.2.1.c
BNC Audio Output Connector	___	___	4.3.2.1.d
Attenuator Control Pushbuttons/Display	___	___	4.3.2.1.e (modified)
Gain Control Pushbuttons/Display	___	___	4.3.2.1.e,f (modified)
Freq.Tuning Knob/Pushbuttons	___	___	4.3.2.1.g
Z Axis Gain Control Knob	___	___	4.3.2.1.h
Z Axis On/Off Pushbutton	___	___	4.3.2.1.i
Z Axis Polarity Pushbutton	___	___	4.3.2.1.j
Power On/Off Switch	___	___	4.3.2.1.k
RF Overload Indicator	___	___	4.3.2.1.l
IF/Detector Overload Indicator	___	___	4.3.2.1.m (modified)
Frequency Display	___	___	4.3.2.1.n
Front Panel Controls/Displays OK?			___Yes ___No
REAR PANEL			
Z axis Output Connector	___	___	4.3.2.2.a
IF Output Connector	___	___	4.3.2.2.b
Reference Oscillator Output Connector	___	___	4.3.2.2.c
Signal Monitor Connector	___	___	4.3.2.2.d
IEEE-488 Connector	___	___	4.3.2.2.e
AC Input Connector	___	___	4.3.2.2.f
Line voltage select	___	___	4.3.3.8.f
Rear Panel Switches/Connectors OK?			___Yes ___No
ACCESSORIES			
Shielded Power cord	___	___	4.3.3.8.d
Extender Card	___	___	(n.a.)
Accessories OK?			___Yes ___No

	Measurement	Requirement	
WEIGHT	_____lbs	Not exceed 75 lbs	4.5
Weight OK?			___Yes ___No

PHYSICAL AUDIT DATA SHEET
TEST PARAGRAPH 4.3.1
Continued

SIZE

Height	_____in.	Not exceed 7.0 in. 4.5
Length	_____in.	Not exceed 21.0 in. 4.5
Width	_____in.	Not exceed 17.5 in. 4.5

Size OK? ___Yes ___No

IDENTIFICATION LABELS

Label with Make, Model, and Serial No. is in place on rear panel? ___Yes ___No

OPERATIONAL TESTS DATA SHEET
TEST PARAGRAPH 4.3.2

4.3.2.1 Set-up for Operational Tests

	MEASUREMENT	REQUIREMENT
Temperature	_____ deg.F	75 ± 10 degrees F
Altitude	_____ Ft	0 to 3000 feet
Humidity	_____ %	10 to 90 %
Power line voltage	_____ vac	115 ± 3 vac

Test Conditions OK? Yes___ No___

Power Cable Connection OK? Yes___ No___

4.3.2.2 Knob Alignment

Knob Alignment OK? Yes___ No___

4.3.2.3 Start-up and Initialization

(a) TUNE light-bar indicator illuminated? Yes___ No___

(b) Any of following Light-bar indicators illuminated? Yes___ No___

	Illuminated?
UNLOCK	___
RFOVL	___
IF/DET OL	___
UNREG	___

If yes, terminate the test and correct the problem.
Describe Corrective Actions:

(c) "PwrHi" / "PwrLo" lightbars illuminated? Yes___ No___
If Yes, line voltage is: _____ vac

Corrective action: adjust line voltage

Corrected line voltage: _____ vac

(d) Reset Receiver to Standard Test Conditions

Audible Alarm:
BEEP light-bar illuminates? Yes___ No___

OPERATIONAL TESTS DATA SHEET
TEST PARAGRAPH 4.3.2
Continued

(e) Front panel displays illuminated and indicate the following?

Frequency Display:	100 MHz	
Input Attenuation Display:	20 dB	
Gain Display:	0 dB	
Bandwidth Display:	1 MHz	Yes__ No__

(f) 10 minute warm up completed? Yes__ No__

4.3.2.4 Input Operation Yes__ No__

(b) LED in RF Input #1's pushbutton illuminated? Yes__ No__

(c) IF Signal (cable to RF Input #1) _____ dBm

IF Signal (cable to RF Input #2) _____ dBm

RF Input #2's LED illuminated? Yes__ No__

IF Signal (RF Input #2 selected) _____ dBm

4.3.2.5 Display Tests

4.3.2.5.1 Input Attenuation Display Reading:

Reading:	Should Be:	Reading OK?
____	20 dB	Yes__ No__
____	30 dB	Yes__ No__
____	40 dB	Yes__ No__
____	50 dB	Yes__ No__
____	60 dB	Yes__ No__
____	70 dB	Yes__ No__
____	AUTO	Yes__ No__
____	60 dB	Yes__ No__
____	50 dB	Yes__ No__
____	40 dB	Yes__ No__
____	30 dB	Yes__ No__
____	20 dB	Yes__ No__
____	10 dB	Yes__ No__
____	0 dB	Yes__ No__

Beep tone? Yes__ No__

OPERATIONAL TESTS DATA SHEET
TEST PARAGRAPH 4.3.2
Continued

4.3.2.5.2 Bandwidth Display

Reading:	Should Be:	Reading OK?
____	1 MHz	Yes__ No__
____	4 MHz	Yes__ No__
____	15 MHz	Yes__ No__
Beep tone?		Yes__ No__
____	4 MHz	Yes__ No__
____	1 MHz	Yes__ No__
____	300 KHz	Yes__ No__
____	100 KHz	Yes__ No__
____	50 KHz	Yes__ No__
____	20 KHz	Yes__ No__
____	10 KHz	Yes__ No__
____	5 KHz	Yes__ No__
____	2 KHz	Yes__ No__
____	1 KHz	Yes__ No__
____	500 Hz	Yes__ No__
Beep tone?		Yes__ No__

4.3.2.5.3 Frequency Display and Tuning

Enter:	Reading:	Reading OK?
888.88 KHz	____ KHz	Yes__ No__
7777.7 Hz	____ Hz	Yes__ No__
999.9 MHz	____ MHz	Yes__ No__

4.3.2.6 Tuning Tests

Left-most digit (#1) tunes properly?	Yes__ No__
Digit #2 tunes properly?	Yes__ No__
Digit #3 tunes properly?	Yes__ No__
Digit #4 tunes properly?	Yes__ No__
Digit #5 tunes properly?	Yes__ No__
Digit #6 tunes properly?	Yes__ No__
Digit #7 tunes properly?	Yes__ No__
Digit #8 tunes properly?	Yes__ No__

OPERATIONAL TESTS DATA SHEET
TEST PARAGRAPH 4.3.2
Continued

4.3.2.7 Display Brightness

BRIGHT light-bar illuminates? Yes__ No__

Brightness fully adjustable? Yes__ No__

4.3.2.8 Audible Alarm

BEEP light-bar illuminates? Yes__ No__

Set to comfortable sound level? Yes__ No__

4.3.2.9 Synthesizer Step Noise in Outputs

Step Noise detected? Yes__ No__

List Frequencies:

4.3.2.10 Scan Mode

Start Frequency	50 KHz
Stop Frequency	150 KHz
Step Size	1 KHz

(c) SCAN light-bar illuminates? Yes__ No__

(c) START light-bar illuminates? Yes__ No__

(d) STOP and STEP light-bars illuminate? Yes__ No__

(e) Oscilloscope display shows the presence of a strong signal mid-point of sweep? Yes__ No__

(f) "Pause" key operates correctly? Yes__ No__

TRANSFER FUNCTION TESTS DATA SHEET
TEST PARAGRAPH 4.3.3

4.3.3.1 Input Attenuator

(c) IF Output amplitude:_____dBm (for reference only)

(c) Frequency = 100 KHz

Attenuation Setting (dB)	Pwr.Meter Change (dB) 0.2 dB max.	Attenuator Error Acceptable?	
		YES	NO
10			
20			
30			
40			
50			
60			
70			

(d) Frequency = 100 MHz

Attenuation Setting (dB)	Pwr.Meter Change (dB) 0.2 dB max.	Attenuator Error Acceptable?	
		YES	NO
10			
20			
30			
40			
50			
60			
70			

TRANSFER FUNCTION TESTS DATA SHEET
TEST PARAGRAPH 4.3.3
Continued

4.3.3.1 Input Attenuator, continued

(e) Frequency = 900 MHz

Attenuation Setting (dB)	Pwr.Meter Change (dB) 0.2 dB max.	Attenuator Error Acceptable?	
		YES	NO
10			
20			
30			
40			
50			
60			
70			

TRANSFER FUNCTION TESTS DATA SHEET
TEST PARAGRAPH 4.3.3
Continued

4.3.3.2 Variable Gain

Frequency and BW	Gain Setting (dB)	IF Output (dBm)	Required IF Output (dB) ± 1 dB		Output OK?	
					Yes	No
100 KHz						
10 Khz						
10 MHz						
1 MHz						
500 MHz						
1 MHz						

4.3.3.3 AGC Mode

(b) IF output amplitude (for reference) _____ dBm

(c) IF output amplitude with AGC _____ dBm
(c) IF output with -50 dBm input _____ dBm

Difference (-2 to +2 dB) _____dB AGC OK? Yes___ No___

(d) Time constant for -30 to -25 dBm _____ sec.

T.C. is 0.1 ± .02 sec? Yes___ No___

Time constant for -25 to -30 dBm _____ sec.

T.C. is 0.1 ± .02 sec? Yes___ No___

TRANSFER FUNCTION TESTS DATA SHEET
TEST PARAGRAPH 4.3.3
Continued

4.3.3.4 Incremental Gain Mode

(b) IF output amplitude _____dBm

(c) △ GAIN light-bar illuminates? Yes___ No___

Gain Reading:		Should Be:	Reading OK?
Initial	_____	0	Yes___ No___
@ -50 dBm	_____	+20	Yes___ No___

(d)

Gain Reading:		Should Be:	Reading OK?
Initial	_____	0	Yes___ No___
@ -10 dBm	_____	-40	Yes___ No___

IF TESTS DATA SHEET
TEST PARAGRAPH 4.3.4

4.3.4 IF Selectivity (Fixed Filters)

IF BW	Low 6 dB	High 6 dB	6 dB BW	Min Max	OK ?	Low 60 dB	High 60 dB	60 dB BW	Min Max	OK ?
15 MHz				14.0 17.0					20.0 25.0	
4 MHz										
1 MHz										
300 KHz										
100 KHz										

Fixed filter IF BW OK? Yes__ No__

IF TESTS DATA SHEET
TEST PARAGRAPH 4.3.4
Continued

4.3.4.2 IF Selectivity (DCIF Filters)

(d,e) DEFAULT FILTER SET:

IF BW	Low 6 dB	High 6 dB	6 dB BW	Min Max	OK ?	Low 60 dB	High 60 dB	60 dB BW	Min Max	OK ?
50 KHz										
20 KHz										
10 KHz										
5 KHz										
2 KHz										
1 KHz										
500 Hz										
200 Hz										

Default IF BW OK? Yes___ No___

IF TESTS DATA SHEET
TEST PARAGRAPH 4.3.4
Continued

(f) ADDITIONAL ALTERNATE FILTERS:

ALT BW light-bar illuminates? Yes___ No___

IF BW	Low 6 dB	High 6 dB	6 dB BW	Min Max	OK ?	Low 60 dB	High 60 dB	60 dB BW	Min Max	OK ?
40 KHz										
32 KHz										
25 KHz										
16 KHz										
12.5 KHz										
8 KHz										
6.4 KHz										
4 KHz										
3.2 KHz										

IF TESTS DATA SHEET
TEST PARAGRAPH 4.3.4
Continued

(f) ADDITIONAL ALTERNATE FILTERS (continued):

IF BW	Low 6 dB	High 6 dB	6 dB BW	Min Max	OK ?	Low 60 dB	High 60 dB	60 dB BW	Min Max	OK ?
2.5 KHz										
1.6 KHz										
1.25 KHz										
800 Hz										
640 Hz										
400 Hz										
320 Hz										
250 Hz										

Alternate IF BW OK? Yes__ No__

IF TESTS DATA SHEET
TEST PARAGRAPH 4.3.4
Continued

4.3.4.3 IF Output Level

(c) Sig.Gen. Level ____ dBm

(d) Max. IF output amplitude ____ dBm (Reqmt: at least 0 dBm)

Max.IF Output OK? Yes__ No__

4.3.4.4 Signal Monitor

		Reading	**Spec. Value**
(c)	Freq. counter reading	____ MHz	21.4000000 MHz
(d)	Sig.Monitor amplitude at -107 dBm input	____ dBm	10 uV peak (-90 dBm at 3 MHz BW)
(f)	sideband amplitude at 1 KHz modulation	____ dBm	na
	3 dB Frequency	____ MHz	na
	Bandwidth (2 X 3 dB Frequency)	____ MHz	at least 4.0 MHz

Signal Monitor OK? Yes__ No__

NOISE FIGURE TESTS DATA SHEET
TEST PARAGRAPH 4.3.5

4.3.5 Noise Figure Tests

FREQUENCY	BW	THEORETICAL NOISE FLOOR	3 dB SENSI-TIVITY	NOISE FIGURE 15 dB max	NF OK ?
50 KHz	1 KHz	-144 dBm			
100 KHz	1 KHz	-144 dBm			
200 KHz	1 KHz	-144 dBm			
200 KHz	10 KHz	-134 dBm			
500 KHz	10 KHz	-134 dBm			
5 MHz	10 KHz	-134 dBm			
10 MHz	10 KHz	-134 dBm			
14 MHz	10 KHz	-134 dBm			
16 MHz	10 KHz	-134 dBm			
100 MHz	1 MHz	-114 dBm			
500 MHz	1 MHz	-114 dBm			
900 MHz	1 MHz	-114 dBm			

Noise Figure OK? Yes__ No__

IMAGE AND IF REJECTION TESTS DATA SHEET
TEST PARAGRAPH 4.3.6

4.3.6 Image and IF Rejection Test

RECEIVER		(c) INITIAL READINGS			(d) IMAGE MEASUR-EMENTS		(d) IMAGE RE-JECTION	
Tuned Freq.	Band-width	Sig-Gen. Freq.	Sig.Gen. Level (A)	IF Out put	Sig.Gen. Freq.	Sig.Gen. Level (B)	B-A	At least 80 dB?
10 KHz	1 KHz	10 KHz			16 KHz			
100 KHz	10 KHz	100 KHz			106 KHz			
500 KHz	10 KHz	500 KHz			43.3 MHz			
5 MHz	10 KHz	5 MHz			47.8 MHz			
14 MHz	10 KHz	14 MHz			56.8 MHz			
20 MHz	1 MHz	20 MHz			1470 MHz			
500 MHz	1 MHz	500 MHz			1950 MHz			
900 MHz	1 MHz	900 MHz			2350 MHz			

Image Rejection OK? Yes___ No___

IMAGE AND IF REJECTION TESTS DATA SHEET
TEST PARAGRAPH 4.3.6
Continued

RECEIVER		(c) INITIAL READINGS			(e) IF MEASUR-EMENTS		IF REJECTION	
Tuned Freq.	Band-width	Sig-Gen. Freq.	Sig.Gen. Level (A)	IF Out put	Sig.Gen. Freq.	Sig.Gen. Level (B)	B-A	At least 80 dB?
10 KHz	1 KHz	10 KHz			3 KHz			
100 KHz	10 KHz	100 KHz			3 KHz			
500 KHz	10 KHz	500 KHz			21.4 MHz			
5 MHz	10 KHz	5 MHz			21.4 MHz			
14 MHz	10 KHz	14 MHz			21.4 MHz			
20 MHz	1 MHz	20 MHz			1450 MHz			
500 MHz	1 MHz	500 MHz			1450 MHz			
900 MHz	1 MHz	900 MHz			1450 MHz			

IF Rejection OK? Yes___ No___

AM DYNAMIC RANGE TESTS DATA SHEET
TEST PARAGRAPH 4.3.7

4.3.7 AM Dynamic Range Tests

Sig.Gen Level (dBm)	LIN (dBm)	LIN (log)	LOG (dBm)
-100			
-90			
-80			
-70			
-60			
-50			
-40			
-30			
-20			
-10			

AM DYNAMIC RANGE TESTS DATA SHEET
TEST PARAGRAPH 4.3.7
Continued

Plot LIN (log) Data for Linear Detection:

From plot:

± 1 dB Linear range:

a. Start sig.gen level: _____ dBm

b. End sig.gen level: _____ dBm

Dynamic Range (b-a) _____ dB (must be at least 35 dB)

Linear Dyn. Range OK? Yes__ No__

AM DYNAMIC RANGE TESTS DATA SHEET
TEST PARAGRAPH 4.3.7
Continued

Plot LOG Data for Log Detection:

From plot:

± 1 dB Linear range:

a. Start sig.gen level: _____ dBm

b. End sig.gen level: _____ dBm

Dynamic Range (b-a) _____ dB (must be at least 60 dB)

Log Dyn. Range OK? Yes__ No__

IDR TESTS DATA SHEET
TEST PARAGRAPH 4.3.8

4.3.8 Instantaneous Dynamic Range (IDR) Tests

Receiver Freq.	BW	Noise Figure*	A Freq.	B Freq.	Sig.-Gen Level (dBm)	IDR (dB) **	At least 60 dB?
100 KHz	1 KHz						
10 MHz	10 KHz						
100 MHz	1 MHz						

* from 4.3.5 Noise Figure Tests

** Calculate IDR:

IDR (dB) = 2/3 (IIP - NF + 174 - 10(log BW))

where:
IIP is the third order input intercept point in dBm = Sig.Gen Level
NF is the receiver noise figure = Noise figure from previous test
BW is the receiver bandwidth =

BW	10(log BW)
1 KHz	30
10 KHz	40
1 MHz	60

IDR OK? Yes__ No__

INPUT TESTS DATA SHEET
TEST PARAGRAPH 4.3.9

4.3.9 Input Tests

4.3.9.1 Input Isolation

Receiver Freq.	BW	Sig.Gen. Amplitude (dBm)	Spec.An. Amplitude (dBm)	Isolation (dB)*	At least 60 db?
100 KHz	1 KHz				
10 MHz	10 KHz				
100 MHz	1 MHz				

* Calculate isolation = Sig.Gen Amplitude - Spec.Analyzer Amplitude

Input Isolation OK? Yes__ No__

4.3.9.2 LO Re-radiation

Receiver Freq.	BW	LO Re-Radiation (dBm)	At least -90 dBm?
100 KHz	1 KHz		
10 MHz	10 KHz		
100 MHz	1 MHz		
900 MHz	1 MHz		

LO Re-radiation OK? Yes__ No__

INPUT TESTS DATA SHEET
TEST PARAGRAPH 4.3.9
Continued

4.3.9.3 Input Impedance and VSWR

Coupler	Frequency	Attenuator	Return Loss (dB)	Less than 9 dB?
HF	100 KHz	0 dB		
HF	100 KHz	30 dB		
HF	10 MHz	0 dB		
HF	10 MHz	30 dB		
HP 778D	100 MHz	0 dB		
HP 778D	100 MHz	30 dB		
HP 778D	900 MHz	0 dB		
HP 778D	900 MHz	30 dB		

Input Impedance and VSWR OK? Yes___ No___

4.3.9.4 Maximum Tolerated RF Input

(a) Signal generator level for 30 dBm output from power amplifier _____ dBm

Signal generator level for -20 dBm output from power amplifier _____ dBm

(c) Receiver operation OK? Yes___ No___
Input attenuator to 0 dB and RF Gain to maximum? Yes___ No___

(d) Receiver operation OK after 30 dBm input? Yes___ No___

(e) Input attenuator to 30 dB? Yes___ No___

(d) Receiver operation OK after 30 dBm input? Yes___ No___

Max. Tolerated RF Input OK? Yes___ No___

IF IMPULSIVE TESTS DATA SHEET
TEST PARAGRAPH 4.3.10

4.3.10 IF Impulse Response Tests

4.3.10.1 Fixed Filter Impulse Response

Impulse Gen. (IG)		Tuned Freq	Recvr BW	1st Peak (A)	P-P Ring-ing (a)	Ratio (a/A) (%)	Less than 12% ?
Rep.-Rate	dBm Level						
1 KHz	-30	100 MHz	300 KHz				
1 KHz	-30	100 MHz	1 MHz				
1 Khz	-30	100 MHz	4 MHz				
1 Khz	-30	100 MHz	15 MHz				

Impulse response of fixed filters OK? Yes___ No___

IF IMPULSIVE TESTS DATA SHEET
TEST PARAGRAPH 4.3.10
Continued

4.3.10.2 DCIF Impulse Response

Impulse Gen. (IG)		Receiver Tuned Frequency	Recvr BW	1st Peak (A)	P-P Ring-ing (a)	Ratio (a/A) (%)	Less than 8% ?
Rep.-Rate	dBm Level						
1 KHz	-30	100 KHz	100 KHz				
1 KHz	-30	100 KHz	50 KHz				
1 KHz	-30	100 KHz	20 KHz				
1 KHz	-30	100 KHz	10 KHz				
100 Hz	-30	100 KHz	5 KHz				
100 Hz	-30	100 KHz	2 KHz				
100 Hz	-30	100 KHz	1 KHz				
10 Hz	-30	100 KHz	500 Hz				
10 Hz	-30	100 KHz	100 Hz				

Impulse response of DCIF filters OK? Yes___ No___

FREQUENCY ACCURACY AND STABILITY TESTS DATA SHEET
TEST PARAGRAPH 4.3.11

4.3.11 Frequency Accuracy and Stability

(a) Receiver stabilized at room temperature for 8 hours? Yes__ No__

Time of Measurement	Approx. Elapsed Time	Frequency (MHz)	Frequency Accuracy (%)*	Frequency Stability (%)**
	0			
	5			
	10			
	15			
	20			
	25			
	30			
	45			
	60			
	1 hr 15 min			
	1 hr 30 min			
	1 hr 45 min			
	2 hr			

* Frequency Accuracy = {Frequency (MHz) - 21.4000000}/ 21.4000000.

** Frequency Stability = {Frequency @ 2 hrs - Frequency}/21.4000000.

Frequency Accuracy better than 1 ppm at 1/2 hour? Yes__ No__

Frequency Stability better than 1 ppm at 1/2 hour? Yes__ No__

OUTPUT TESTS DATA SHEET
TEST PARAGRAPH 4.3.12

4.3.12 Output Tests

4.3.12.1 BFO operation

(c) Audio frequency changes smoothly? Yes__ No__

(d) Frequency counter indication: _____

Frequency approx. equal to zero? Yes__ No__

(e) Frequency counter reading for + 4 KHz: _____

Frequency approx. equal to 4 KHz? Yes__ No__

(f) Audio signal changes with same resolution? Yes__ No__

(g) Frequency counter's reading for - 4 KHz: _____

Frequency approx. equal to 4 KHz? Yes__ No__

4.3.12.2 AM Video Output

(c) DC video offset voltage (for reference only)

Bandwidth	1 KHz	10 KHz	50 KHz	1 MHz	15 MHz
DC Offset					

(e) Max. video output level ____ Vdc

Max. video signal greater than 2 Vdc? Yes__ No__

(g) Video signal set to 2 volt (peak)? Yes__ No__

OUTPUT TESTS DATA SHEET
TEST PARAGRAPH 4.3.12
Continued

4.3.12.2 AM Video Output, continued

(h) Peak voltage readings:

Frequency	Peak Volts
100 KHz	
500 KHz	
1 MHz	
2 MHz	
4 MHz	
6 MHz	
7 MHz	
7.5 MHz	
8 MHz	
9 MHz	
10 MHz	
12 MHz	

(i) Cut-off Frequency (from plot) ____ MHz

Cut-off freq. is greater than 7.5 MHz? Yes__ No__

OUTPUT TESTS DATA SHEET
TEST PARAGRAPH 4.3.12
Continued

4.3.12.3 Z-axis

		NORMAL	INVERTED
(c,d)	Max. Z-axis RMS output:	____	____

Max. Z-axis signal greater than 2 Vrms? Yes__ No__

(f) Peak voltage readings:

Frequency	Peak Volts
100 KHz	
500 KHz	
1 MHz	
2 MHz	
4 MHz	
6 MHz	
7 MHz	
7.5 MHz	
8 MHz	
9 MHz	
10 MHz	
12 MHz	

(i) Cut-off Frequency (from plot) ____ MHz

Cut-off freq. is greater than 7.5 MHz? Yes__ No__

OUTPUT TESTS DATA SHEET
TEST PARAGRAPH 4.3.12
Continued

4.3.12.4 AM Log Output

(c) DC Log offset voltage

Bandwidth	1 KHz	10 KHz	50 KHz	1 MHz	15 MHz
DC Log Offset					

(e) Max. Log output level ____ Vdc
Max. Log output greater than +2 vdc? Yes__ No__

4.3.12.5 Audio Output

(c) Max. audio output RMS voltage _____ Vrms
Max. audio output greater 1 vrms? Yes__ No__

Frequency	Peak-Peak Volts
10 Hz	
20 Hz	
30 Hz	
40 Hz	
60 Hz	
100 Hz	
1 KHz	
4 KHz	
6 KHz	
10 KHz	
12 KHz	
13 KHz	
14 KHz	
15 KHz	

(e) Low Cut-off Frequency (from plot) ____ Hz
Low Cut-off freq. less than 30 Hz? Yes__ No__
High Cut-off Frequency (from plot) ____ KHz
High Cut-off freq. greater than 12 KHz? Yes__ No__

SPURIOUS RESPONSE TEST DATA SHEET
TEST PARAGRAPH 4.3.13

4.3.13 Spurious Response Test

(b,d) Frequency range = 1 KHz to 20 KHz

Bandwidth = 500 Hz

(b) Spurious Responses Scan		(d) Spurious Input Level (dBm)	Spurious less than -107 dBm?
Frequency	Amplitude		

Spurious responses up to 20 KHz OK? Yes___ No___

(c,d) Frequency range = 20 KHz to 1 GHz

Bandwidth = 10 KHz

(c) Spurious Responses Scan		(d) Spurious Input Level (dBm)	Spurious less than -107 dBm?
Frequency	Amplitude		

Spurious responses above 20 KHz OK? Yes___ No___

POWER TESTS DATA SHEET
TEST PARAGRAPH 4.3.14

4.3.14.1 High Line Voltage

(d) Receiver operation normal? Yes__ No__

(e) Line fuse(s) blow? Yes__ No__
If no, describe corrective action:

(g) Receiver operates properly after high voltage test? Yes__ No__

4.3.14.2 Power Requirements

(e) Receiver operation normal? Yes__ No__

(f) AC Power Supply: Voltage ____ Vrms

Current ____ Amps

Power = Voltage x Amps = _____ Watts

(h) Receiver operation normal at 48 Hz? Yes__ No__

(i) Receiver operation normal over range of 48 to 62 Hz? Yes__ No__

(j) PWRHI light-bar illuminates with high-line? Yes__ No__

(k) PWRHI light-bar extinguishes when power range switch set to high line position? Yes__ No__

(l) Receiver operation normal at 127 vac and 60 Hz? Yes__ No__

(m) Receiver operation normal at 127 vac and 48 Hz? Yes__ No__

(n) Receiver operation normal at 127 vac and 62 Hz? Yes__ No__

(o) PWRLO light-bar illuminates with low-line? Yes__ No__

(p) PWRLO light-bar extinguishes when power range switch set to low line position? Yes__ No__

(q) Receiver operation normal at 102 vac and 60 Hz? Yes__ No__

(r) Receiver operation normal at 102 vac and 48 Hz? Yes__ No__

(s) Receiver operation normal at 102 vac and 62 Hz? Yes__ No__

TECHNICAL MANUAL

FOR THE

R-110 RECEIVER

This manual is intended for use with

the following serial number:

_____

Document released

August 13, 1991

Dynamic Sciences International Inc.
6130 Variel Avenue
Woodland Hills, CA 91367
(818)226-6262 Fax:(818) 226-6247

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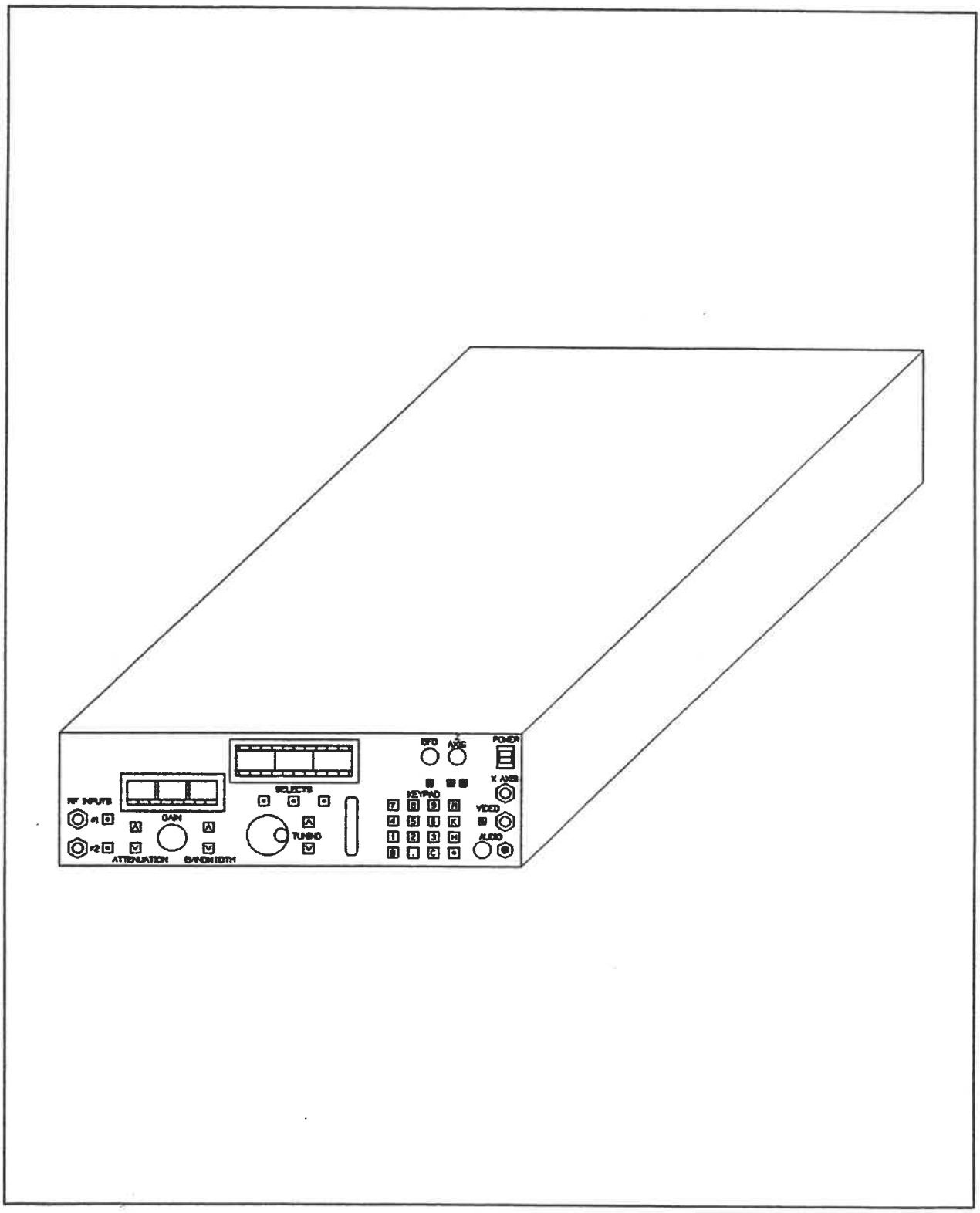


Frontispiece

INTRODUCTION

This manual provides operation, installation, and maintenance instructions for the Dynamic Sciences R-110 receiver. The purpose of the receiver is to detect and demodulate RF signals over a frequency range of 1 kHz to 1 GHz. The receiver is designed for both laboratory and field operations.

The manual is organized in sections providing the following information:

Section 1, **Description of Equipment**, provides an overview of the receiver with listings of specifications, characteristics, equipment supplied, and additional equipment needed for installation and service.

Section 2, **Installation**, supplies the information required to unpack and install the equipment, including a listing of the physical characteristics of crated equipment, cable requirements, installation procedures, and preparations required for reshipment.

Section 3, **Operating Instructions**, provides a discussion of the controls and indicators, along with detailed operating instructions. Information regarding instrument initialization and fault indications are included in this section.

Section 4, **Theory of Operation**, includes an overview discussion of system operation and in-depth detailed discussions of the functional operation of the electronic circuits and mechanical assemblies. The explanation of circuit functions are supported by signal flow diagrams for each of the major sections.

Section 5, **Maintenance**, provides information for maintaining and repairing the receiver. Beginning with a listing of recommended periodic maintenance, the section includes a detailed performance test designed to demonstrate that all of the receiver functions are operating properly, to a high degree of confidence. Following the maintenance procedures, further procedures are given for fault isolation, mechanical disassembly of the radio, and field service adjustments for newly installed modules.

Section 6, **Parts Lists and Circuit Diagrams**, includes parts lists for all sections of the receiver, with reference designations and a listing of manufacturers. This chapter also provides circuit diagrams for all sections of the receiver, including reference designaltions tied to the associated parts lists.

Appendix A, **IEEE-488 Interface Protocol**, lists the compatibility level supported for each standard IEEE-488 function, lists and describes the supported IEEE-488.2 standard protocols and commands, and lists and describes the additional interface protocols and commands unique to the R-110.

Appendix B, **Hardware Address Map**, gives the port addresses of all of the hardware which communicates with the controlling microprocessor. Usage of individual bits in these ports, and usage of read vs. write ports at the same address, are given where necessary.

SECTION 1. DESCRIPTION OF EQUIPMENT

1.1 Description and Purpose

The R-110 receiver, shown in the frontispiece, is a solid-state multiple-conversion receiver that provides a means of detecting and measuring signals associated with electromagnetic analysis, TEMPEST, spectrum analysis, and frequency surveillance, in the range of 1 kHz to 1 GHz. Three basic modes of operation are incorporated into the instrument: manual operation, automated sweeping, and remote operation controlled by a host computer. The receiver will also work with various accessories such as the R-1180 microwave downconverter, which extends the frequency range to 18 GHz.

1.2 Equipment Description

The R-110 receiver consists of modularly-constructed electronic circuits integrated with a front panel assembly containing operator controls and indicators. RF, video, and analog signals are interconnected by dedicated connectors located on the front and rear panels of the instrument. Function control signals and interface data used by separately mounted equipment are provided through multi-contact connectors that use distinctive configurations to prevent improper positioning when mated.

1.3 Physical Characteristics

The physical characteristics of the R-110 are shown in table 1-1.

1.4 Specifications

The detailed electrical and performance specifications of the R-110 receiver are shown in table 1-2. Each entry is prefaced with the applicable paragraph number from section 4.3.3 of the SOW or a "DSI", indicating that the item is in addition to the specified requirements. An "*" indicates that the specification paragraph has been revised. The "As Designed" entries show the anticipated operation/performance of the prototype and production receivers; a "Same" means "same as specified requirement". The "Specification" entries are from the SOW and approved revisions.

Table 1-1: Physical Characteristics

Line Voltage	115/230 VAC ± 10%
Power Dissipation	100 Watts
Mechanical Dimensions	
Standard Height	5.22" (133 mm)
Standard Width	17.00" (432 mm)
Standard Depth	20.50" (521 mm) (plus depth of front panel controls)
Rack Mount Height	5.22" (133 mm)
Rack Mount Width	19.00" (483 mm)
Rack Mount Depth	20.50" (521 mm) (plus depth of front panel controls)
Weight	39 lbs (18 kg)
Volume	1.0 cu ft
Cooling	Free/forced convection
Temperature Range	
Operating	+40° - +105° F (+5° to +40° C)
Storage	-40° - +167° F (-40° - +75° C)
Relative Humidity	
Operating	0 - 90% non-condensing
Storage	0 - 95% non-condensing

Table 1-2: Specifications

Feature	Specification
Modes of Operation	Manual, scan, and remote (standard); downconverter (optional)
RF Inputs	Two inputs, remotely or locally selectable, break-before-make switching
Frequency Range	Both inputs tunable from 1 kHz to 1 GHz
Noise Figure	10 dB (10)
Spurious-Free Dynamic Range	Not less than 60 dB between RF input and AM video output, and between RF input and IF output
RF Input VSWR	Less than 2:1 over full frequency range
RF Input Impedance	50 Ohms nominal
Maximum Tolerated RF Input	1 Watt average CW
Isolation Between RF Inputs	At least 80 dB
LO Leakage at RF Inputs	Less than -90 dBm
Residual Spurious Responses	Less than -107 dBm
IF Rejection	At least 80 dB
Image Rejection	At least 80 dB
RF Input Attenuator: Range Operation Switching Time	 0 - 70 dB in 10 dB steps Manual and autorange Less than 30 ms
Gain	Quasi-continuous, 50 dB range; RF, IF, predetection gains optimized

Table 1-2 Continued

Feature	Specification
Tuning Bands	Three bands, automatically selected
Band Switching Settling Time	30 ms typical
Band Frequency Ranges	1 kHz - 249.9999 kHz 250 kHz - 14.999999 MHz 15 MHz - 1 GHz (hysteresis provided across band breaks)
Tuning	Single knob tuning with selectable tuning rate; dual switches for pushbutton tuning; switches for automatic scan
Tuning Interference	No detectable tuning interference in video and audio outputs
Reference Oscillator Type	100 MHz oven-controlled quartz oscillator; trimmable
Reference Oscillator Aging	1 PPM per year
Reference Oscillator Temperature Stability	0.05 PPM, 0 - 60 °C
Reference Oscillator Output	Greater than 0 dBm
Receiver Frequency Stability	Same as reference oscillator after 30 minutes
Receiver Frequency Accuracy	Same as reference oscillator after 30 minutes
Frequency Display	12 digit alphanumeric LED, adjustable intensity
Frequency Display Readability	Visible in high or low ambient light

Table 1-2 Continued

Feature	Specification
Wideband IF Output Frequency	1450 MHz nominal
Wideband IF Output Level	At least -30 dBm into 50 Ohms
Signal Monitor Center Frequency	21.4 MHz
Signal Monitor Bandwidth	4 MHz minimum
Signal Monitor Output Level	At least -70 dBm with RF input of -107 dBm and full RF gain
IF Center Frequency	21.4 MHz
IF Bandwidths	500 Hz - 20 kHz in 1 - 2 - 5 sequence, 80 kHz, 300 kHz, 1 MHz, 4 MHz, 15 MHz (standard set); 200 Hz - 20 kHz in 1.0 - 1.25 - 1.6 - 2.0 - 2.5 - 3.2 - 4.0 - 5.0 - 6.4 - 8.0 sequence, 80 kHz, 300 kHz, 1 MHz, 4 MHz, 15 MHz (extended set)
IF Impulse Response	Overshoot less than 8% for bandwidth less than 150 kHz, less than 12% for bandwidth greater than 150 kHz
IF Selectivity	Shape factor better than 4:1 (60 to 6 dB) typical
IF Output Level	At least 10 dBm into 50 Ohms
AGC	Selectable with keypad
Detection Modes	AM, CW
Detection Type	AM peak

Table 1-2 Continued

Feature	Specification
Video Outputs	AM linear or log, Z axis
Optional Video Functions	Slideback, pulse stretch
Video Bandwidth	Not less than 1/2 selected IF bandwidth
Linear Video Dynamic Range	At least 30 dB
Log Video Dynamic Range	At least 60 dB
Video and Z Axis Output Impedance	50 Ohms nominal
Video Output Level	At least 4 Volts into 50 Ohms
Z Axis Controls	Output adjustable to 3 Volts RMS and invertible
Audio 3 dB Frequency Response	20 Hz - 20 kHz
Audio Output Level	At least 2 Volts RMS into 8 Ohms
BFO Tuning Range	At least 4 kHz
BFO Tuning Resolution	Continuous
IEEE-488 Capability Levels	SH1, AH1, T6, L4, SR1, RL1, PP0, DC1, DT0, C0
IEEE-488 Controllable Functions	Input selection, input attenuation, bandwidth, gain, tuned frequency, video selection, AGC, and others
Power Cord	Shielded cord
Protection From AC Line Voltage	No damage when improper voltage applied
Line Voltage Range Selection	Rotary switch

1.5 Equipment Supplied

The equipment and accessories supplied are shown in table 1-3.

Table 1-3: Equipment Supplied

QTY	DSI PART NUMBER	DESCRIPTION
1	493000	R-110 FTTR Receiver
1	493000OM	Operator's Manual
1	493012	Cable W1, AC Power

1.6 Equipment Required But Not Supplied

Certain equipment is required for installation or service of the receiver, but must be supplied by the user. Table 1-4 lists these items.

Table 1-4: Equipment Required But Not Supplied

QTY	DESCRIPTION
1	Ground Strap

1.7 Optional Equipment

Certain equipment is available from Dynamic Sciences, Inc., for use with the R-110 receiver which is not included in the basic package. Table 1-5 lists these items.

Table 1-5: Optional Equipment

Part No.	Description
493010	Service Kit
R-1180	Microwave Downconverter
R-1260i	Automated System Controller

SECTION 2. INSTALLATION

2.1 Introduction

This section provides installation information for the R-110 Receiver and includes interconnection data for integrating the receiver with associated equipment. Instructions for repacking the equipment for shipment are also provided.

2.2 Installation Planning

The R-110 Receiver is compact and portable, and can be used in various laboratory and field applications. All that is required is for operation is adequate power and ventilation. If the receiver is to be rack-mounted then the recommendation given for clearance within the rack for the purpose of ventilation should be followed.

2.3 Crating Data

The R-110 is packed in a specially constructed shipping container, as shown in figure 2-1, that protects the instrument during transit. Crate dimensions and weight are shown in table 2-1.

Table 2-1: Crating Data

Height	8 ⅜ in. (213 mm)
Width	22 ½ in. (572 mm)
Depth	27 ⅞ in. (708 mm)
Weight	50 lbs. (22.7 kg)

Note that the factory shipment includes an accessory package, separate from the crate containing the receiver, for the operator's manual and any other documentation.

2.4 Receiving Inspection

Each instrument is carefully tested and inspected prior to shipment. When unpacking, inspect the container and the instrument for evidence of shipping damage. If damage is indicated then notify the freight carrier immediately. Check each item against the packing list or the purchase order, to ensure that all items have been received. Determine that all instrument serial numbers are identical to the numbers shown on the packing list. If portions of the shipment are missing, and are not listed as back ordered items, then contact the freight carrier or Dynamic Sciences.

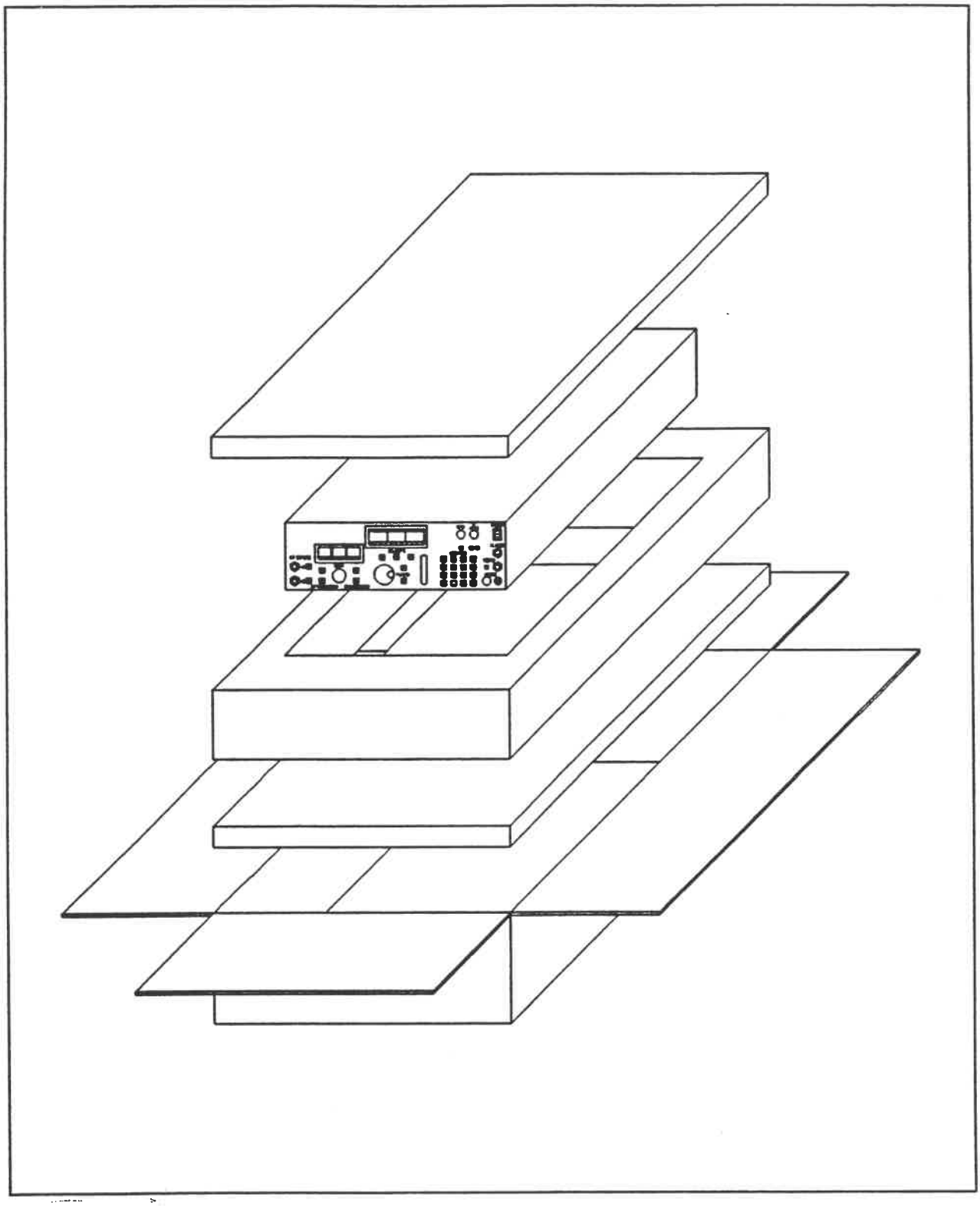


Figure 2-1: Equipment Packaging

2.5 Unpacking

Retain the shipping container and all packing material for subsequent shipments of the instrument, or when storage is required. When an instrument is returned to the factory for repair or modification, attach a tag to the instrument indicating service required, serial number, model number, and the complete return address.

Figure 2-1 shows the shipping container and contents.

Unpacking Procedure:

1. Slit the plastic tape around the top of the shipping container.
2. Open the top of the container.
3. Remove the top layer of shock absorbent material.
4. Remove the instrument from the shipping container by lifting straight up.
5. Ensure that accessory packages have been removed.

2.6 Mounting

The R-110 is designed for either bench operation or rack mounting. For bench operation insure that air-flow at the rear and sides of the instrument is not obstructed. When the instrument is rack mounted, a standard 19" RETMA rack with at least 20" depth is suitable. A minimum clearance of 1.0 inches at the rear of the instrument is required to ensure adequate free air movement. For rack mounting the optional slide rails are to be attached to the receiver's sides. When used in a system configuration, the location of the receiver and any associated components is not specified, and should be determined by the user.

2.7 Cable Requirements

Table 2-2 lists the cables required for operation of the receiver. The table indicates which cables are supplied.

Table 2-2: Connecting Cables

QTY	DSI PART NO.	DESCRIPTION	SUPPLIED
1	493012	W1, AC Power, 117 VAC	Yes
1	NA	W2, AC Power, 220 VAC	No
1	NA	W3, GPIB	No
1	NA	W4, Status	No

2.8 Equipment Connection

All signals interface with the receiver through connectors that are located on the front and rear panels of the instrument. Table 2-3 identifies the receiver's connectors.

Table 2-3: Connector Identification

Front Panel	
Function	**Type**
RF Input #1	Female BNC
RF Input #2	Female BNC
X Axis Output	Female BNC
Video Output	Female BNC
Audio Output	1/4" Phone Jack
Rear Panel	
Function	**Type**
Z Axis Output	Female BNC
Reference Oscillator Output	Female BNC
21.4 MHz IF Output	Female BNC
Signal Monitor Output	Female BNC
IEEE-488 Interface	Female 24 Pin D
Status/Control Output	Female 25 Pin D-Sub
AC Line Input	Male 3 Pin NEMA

2.9 Power Connections and Settings

The instrument is shipped from the factory preset to operate from a power source of 115 volts, 50/60 Hz, single phase. For operation using a different voltage range, select the proper fuse rating from table 2-4, and proceed as follows:

AC Range Selection Procedure:

1. Place the AC line voltage select switch located on the rear panel of the instrument in the proper position.
2. Select and install the proper line fuses for the AC line input voltage to be used.
3. Set the AC line voltage subrange switch to the required position as shown in table 2-5. When both the AC HI and AC LO indicators on the front panel are both extinguished, the range selected is acceptable.

Table 2-4: Fuse Selection

VOLTAGE	FUSE RATING
115 V Range	2 Amp, 2ASB slo-blo, Littelfuse 213002
230 V Range	1 Amp, 1ASB slo-blo, Littelfuse 213001

Table 2-5: Line Voltage Range Selection

SELECT SWITCH	SUBRANGE SWITCH	INPUT VOLTAGE RANGE
115 V	Low	95 - 105 VAC
	Norm	105 - 115 VAC
	High	115 - 126 VAC
230 V	Low	190 - 210 VAC
	Norm	210 - 231 VAC
	High	231 - 253 VAC

The instrument has a 3 conductor power cord which, when connected to an appropriate receptacle, grounds the instrument chassis for safety.

WARNING
THE AC POWER CORD SHOULD ONLY BE CONNECTED TO RECEPTACLES THAT HAVE ACTIVE PROTECTED EARTH GROUND CONTACTS. BYPASSING OR DEFEATING THE EARTH GROUND PROTECTION CAN RESULT IN INJURY TO OPERATING PERSONNEL.

2.10 External Interfaces

Pin numbers and signal identification for the IEEE-488 interface connector are listed in table 2-6.

The signal identification for the internally mounted RS-232 service connection is listed in table 2-8.

The R-110 comes factory-set to IEEE-488 interface address 16, and with the RS-232 interface set to a baud rate of 1200. To change either of them, perform the appropriate procedure, as follows:

IEEE-488 Address Setting Procedure:

1. Unplug the receiver. Remove the retaining screws from the cover and slide off of the chassis.

2. There is one dipswitch visible through the hatch on the underside of the front panel assembly. Switches 1 - 5 determine the bus address. The desired address must be set in binary, with switch 5 considered to be the MSB. "On" generates a zero, "Off" a one. Table 2-7 lists the setting for each available address.

3. When the dipswitch is set to the desired value, replace the cover and reassemble the receiver. The new setting will be read on power-up.

4. The bus address may be temporarily changed by means of the front panel controls, but this setting is lost when power is removed. See chapter 3 for details.

RS-232 Baud Rate Setting Procedure:

1. Unplug the receiver. Remove the retaining screws from the cover and slide off of the chassis.

2. There is one dipswitch visible through the hatch on the underside of the front panel assembly. Switches 6 - 8 determine the baud rate. The desired address must be set in binary, with switch 8 considered to be the MSB. "On" generates a zero, "Off" a one. Table 2-9 lists the setting for each available baud rate.

3. When the dipswitch is set to the desired value, replace the cover and reassemble the receiver. The new setting will be read on power-up.

Table 2-6: IEEE-488 Interface Connector Pinout

PIN	SIGNAL	PIN	SIGNAL
1	DIO1	13	DIO5
2	DIO2	14	DIO6
3	DIO3	15	DIO7
4	DIO4	16	DIO8
5	EOI	17	REN
6	DAV	18	DAV GND
7	NRFD	19	NRFD GND
8	NDAC	20	NDAC GND
9	IFC	21	IFC GND
10	SRQ	22	SRQ GND
11	ATN	23	ATN GND
12	SHIELD	24	LOGIC GND

Table 2-7: Dipswitch Settings for IEEE-488 Interface Address

ADDRESS	SWITCH				
	1	2	3	4	5
0	On	On	On	On	On
1	Off	On	On	On	On
2	On	Off	On	On	On
3	Off	Off	On	On	On
4	On	On	Off	On	On
5	Off	On	Off	On	On
6	On	Off	Off	On	On
7	Off	Off	Off	On	On
8	On	On	On	Off	On
9	Off	On	On	Off	On
10	On	Off	On	Off	On
11	Off	Off	On	Off	On
12	On	On	Off	Off	On
13	Off	On	Off	Off	On
14	On	Off	Off	Off	On
15	Off	Off	Off	Off	On
16	On	On	On	On	Off
17	Off	On	On	On	Off
18	On	Off	On	On	Off
19	Off	Off	On	On	Off
20	On	On	Off	On	Off
21	Off	On	Off	On	Off
22	On	Off	Off	On	Off
23	Off	Off	Off	On	Off
24	On	On	On	Off	Off
25	Off	On	On	Off	Off
26	On	Off	On	Off	Off
27	Off	Off	On	Off	Off
28	On	On	Off	Off	Off
29	Off	On	Off	Off	Off
30	On	Off	Off	Off	Off
31	Off	Off	Off	Off	Off

Table 2-8: RS-232 Interface Connector Pinout

PIN	SIGNAL	PIN	SIGNAL
1	Shield GND	14	(Spare)
2	RXD	15	(Spare)
3	TXD	16	(Spare)
4	RTS	17	(Spare)
5	CTS	18	(Spare)
6	DSR	19	(Spare)
7	Signal GND	20	DTR
8	(Spare)	21	(Spare)
9	(Spare)	22	(Spare)
10	(Spare)	23	(Spare)
11	(Spare)	24	(Spare)
12	(Spare)	25	(Spare)
13	(Spare)		(Spare)

Table 2-9: Dipswitch Settings for RS-232 Baud Rate

BAUD RATE	SWITCH		
	6	7	8
110	On	On	On
150	Off	On	On
300	On	Off	On
600	Off	Off	On
1200	On	On	Off
2400	Off	On	Off
4800	On	Off	Off
9600	Off	Off	Off

In addition to the IEEE-488 interface, there is also a connector on the rear panel of the receiver which contains discrete, dedicated status and control lines intended for interfacing to various associated hardware. The signals on the various connector pins are listed in table 2-10.

Table 2-10: Status/Control Output Connector Pinout

PIN	SIGNAL	PIN	SIGNAL
1	Signal GND	14	Unlock
2	Front Overload	15	Back Overload
3	Underload	16	AC High
4	AC Low	17	DC Unregulated
5	Spare Power Status	18	Control 0
6	Control 1	19	Control 2
7	Control 3	20	Control 4
8	Control 5	21	Control 6
9	Control 7	22	Control 8
10	Control 9	23	Control 10
11	Control 11	24	Control 12
12	Control 13	25	Control 14
13	Control 15		

2.11 Ground Stud

A very good ground connection is necessary for the receiver to perform within specification, especially at low frequencies. A ground stud is provided on the rear panel for this purpose. consisting of a 1/4 - 20 bolt and nut. It is recommended that a large, braided ground strap be connected from the stud to a cold-water-pipe or a copper stake driven at least eight feet into the ground. If the receiver is to be used in a system consisting of several pieces of hardware, then a common ground plate should be used to connect ground straps from all instruments in a star configuration, with the pipe or stake connection then being made to the plate.

2.12 Preparation for Reshipment

If at all possible, all shipments of the R-110 should be made in the original factory container. When a new instrument is unpacked, all packing material should be retained for this purpose. Packing the instrument for reshipment should be performed as follows.

Reshipping Procedure:

1. Remove all external cables from the instrument.
2. Enclose the instrument in a plastic bag. Tape the bag shut.
3. Place packing material in the bottom of a suitable shipping container.
4. Place the bagged receiver in the shipping container and cover with the remaining packing material. Make sure that there is adequate padding around the sides of the instrument as well.
5. Seal the box with plastic or paper tape.
6. Make sure that the container bears a label indicating that it contains fragile electronic equipment.
7. Commercial shipment should be insured.

SECTION 3. OPERATING INSTRUCTIONS

3.1 Introduction

This section provides instructions for the operation of the receiver. The section begins with identification of the various controls, pushbuttons, displays, indicators, and connectors. The modes of operation and the default settings are then presented, along with a list of condensed operating instructions. More detailed discussions follow, providing an in-depth understanding of the receiver's operational features.

3.2 Identification of Controls, Displays, and Connectors

Figure 3-1 is a front view of the receiver with numerical designators that are referenced to the identification list of table 3-1. Figure 3-2 provides a back view of the instrument and is referenced to the nomenclature listed in table 3-2. The tables provide a short explanation of function and purpose for each designated item; more detailed explanations are given later.

3.3 Modes of Operation

The primary modes of operation of the R-110 are "Tune", "Scan", "MDC", and "Remote":

Tune: The normal mode of operation. In this mode the receiver is tuned using the rotary tuning control (29), the pushbuttons (14), or the keypad (11). The TUNE mode indicator (23) is illuminated.

Scan: In scan mode the receiver automatically scans a preset frequency range, using preselected step size, rate, and repetition parameters. The SCAN mode indicator (23) is illuminated.

MDC: In this mode the R-110 is connected to a model R-1180 microwave downconverter via the IEEE-488 interface. The R-110 controls the interface and commands the downconverter. The downconverter is placed in remote mode and is set via the R-110's front panel controls. The R-110 remains in tune, scan or other local operating mode. R-110 operation is affected as follows:

- RF input #1 (1) is dedicated to the downconverter output.
- The RF input select pushbuttons (7, 8) are used to control the input selection of the MDC.
- The RF input attenuation of the receiver is set to a fixed value.
- The RF input attenuation pushbuttons (9) are used to control the input attenuation of the downconverter.
- The tuning range of the radio is extended to 18 GHz.
- The MDC mode indicator (24) is illuminated.

Remote: In this mode the R-110 is under control of a host computer. Control is accomplished via the IEEE-488 interface. The REMOTE mode indicator (23) is illuminated.

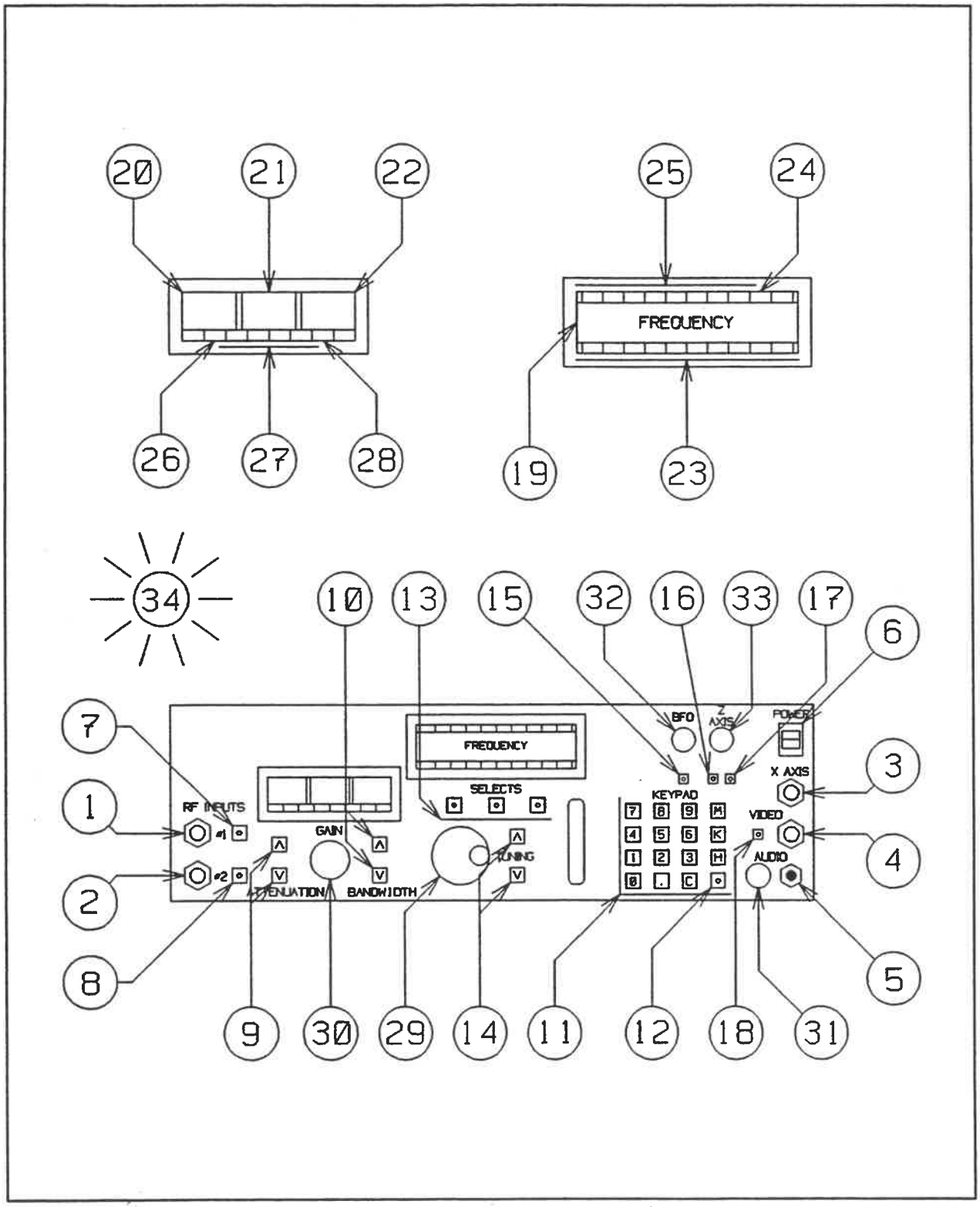


Figure 3-1: Front Panel Reference Designations

Table 3-1: Front Panel Nomenclature

Designation	Description	Designation	Description
1	RF Input #1 Connector	18	Log Pushbutton
2	RF Input #2 Connector	19	Tuning Display
3	X Axis Output Connector	20	Attenuation Display
4	Video Output Connector	21	Gain Display
5	Audio Output Connector	22	Bandwidth Display
6	Power Switch	23	Operating Mode Indicators
7	RF Input #1 Pushbutton	24	MDC Indicator
8	RF Input #2 Pushbutton	25	Status Indicators
9	RF Input Attenuation Pushbuttons	26	Autorange Indicator
10	IF Bandwidth Pushbuttons	27	Gain Mode Indicators
11	Keypad	28	External Wideband Indicator
12	Alternate Function Pushbutton	29	Frequency Tuning Control
13	Select Pushbuttons	30	IF Gain Control
14	Tuning Pushbuttons	31	Audio Volume Control
15	BFO Pushbutton	32	BFO Tuning Control
16	Z Axis Enable Pushbutton	33	Z Axis Level Control
17	Z Axis Invert Pushbutton	34	Audible Indicator

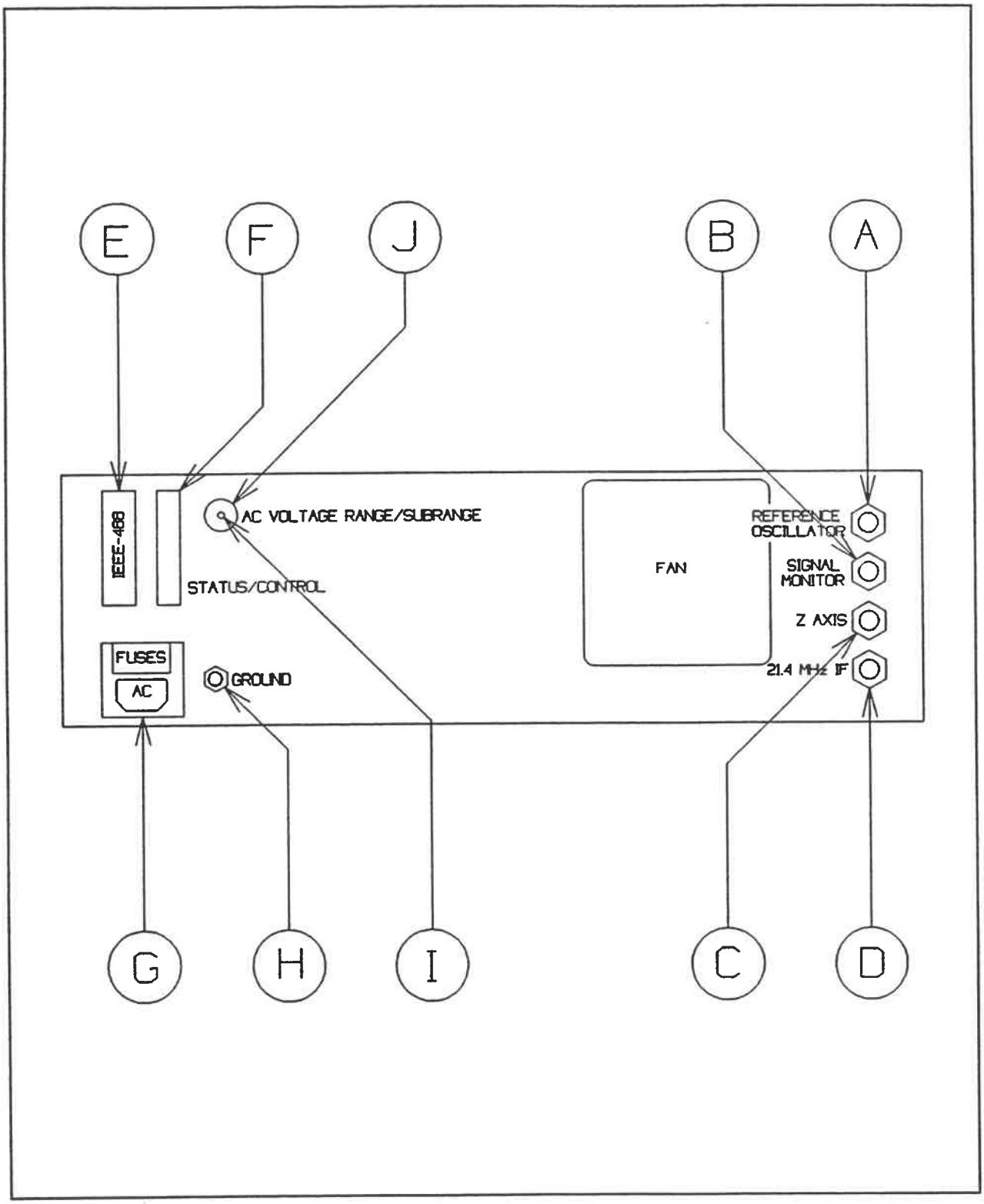


Figure 3-2: Rear Panel Reference Designations

Table 3-2: Rear Panel Nomenclature

Designation	Description
A	Reference Oscillator Output Connector
B	Signal Monitor Output Connector
C	Z Axis Output Connector
D	21.4 MHz IF Output Connector
E	IEEE-488 Interface Connector
F	Status/Control Output Connector
G	AC Line Connector / Fuse Holder
H	Ground Stud
I	AC Voltage Range Switch
J	AC Voltage Subrange Switch

In addition to these primary operating modes, additional, secondary operating modes are provided for entry of parameters and control of functions not directly provided by the front panel controls, including selection of display brightness and beep loudness, storage and recall of panel settings, AGC selection, attenuation, gain, and bandwidth modes, and IEEE-488 interface address display and temporary selection.

The modes are summarized in the condensed procedures in paragraph 3.5 and discussed in detail in paragraph 3.7.

3.4 Default Settings

When the receiver is first powered up, default operating modes and settings are automatically selected, and the front panel indicators and displays are set accordingly. These defaults are stored in reprogrammable memory and may be changed by the user using the "store settings" operating mode. The default conditions provided by the factory are listed in table 3-3.

Table 3-3: Default Settings

Parameter	Setting
Operating Mode	Tune
Tuned Frequency	100 MHz
Tuning Digit Selection	1 MHz
RF Input Selection	RF #1
RF Input Attenuation	20 dB
IF Gain	50 dB
IF Bandwidth	1 MHz
BFO	Disabled
Z Axis Output	Disabled
X Axis Output	0 Volts
Video Output	Linear
Autorange	Disabled
AGC	Disabled
Frequency Tuning	Stepped From Display Digit
Gain Mode	Impulsive Distribution, Knob Display
Bandwidth Mode	Normal, Narrowband
Scan Start Frequency	1 KHz
Scan Stop Frequency	1 GHz
Scan Step Size	100 Hz
Scan Rate	1 Step/Second
Scan Repeat Mode	Single Scan
MDC Control	Disabled
IEEE-488 Interface Address	Preset
Display Brightness	Preset
Front Panel Beep Volume	Preset
Audio Beep Volume	Preset
Audible Indicator Mode	Limit Indication Only

3.5 Condensed Operating Instructions

PRIMARY OPERATION:

Prepare for use:	Verify that the AC voltage range switch (I) is properly set. Verify that the receiver RF input connectors (1)(2) are not connected to a high voltage/energy source (e.g. a PLISN). Connect an IEEE-488 interface cable if remote or downconverter operation is intended.
Power the receiver:	Turn on power switch (6). The receiver will power up and will apply its default settings.
Select tuned frequency:	Enter a frequency (with decimal point) using keypad (11), followed by H, K, or M (Hz, kHz, or MHz).
Step tuned frequency:	Select a tuning resolution display digit with the select pushbuttons (13) and tune using the tuning knob (29) or pushbuttons (14).
Select RF input:	Press the RF Input #1 (7) or #2 (8) pushbutton.
Select RF input attenuation:	Use the RF input attenuation pushbuttons (9) and display (20).
Set IF gain:	Use the IF gain knob (28) and display (21).
Select IF bandwidth:	Use the bandwidth pushbuttons (10) and display (22).
Monitor audio output:	Connect a headphone or speaker to the audio output jack (5).
Adjust audio volume:	Use the audio volume control (31).
Monitor video output:	Connect a cable to the video output connector (4).
Select video detector:	Use the log detector pushbutton (18).
Monitor unprocessed IF:	Connect a cable to the signal monitor output connector (B).
Monitor processed IF:	Connect a cable to the 21.4 MHz IF output connector (D).
Monitor Z-axis output:	Connect a cable to the Z-axis output connector (C) on the rear panel; activate the Z-axis output by pressing the enable pushbutton (16); select polarity with the invert pushbutton (17).
Adjust Z-axis output:	Rotate the Z axis output level control (33).
Tune BFO:	Press the BFO pushbutton (15) to enable it; rotate the BFO tuning control (32) while monitoring the audio output to for tuning.

SECONDARY OPERATION:

Select Autorange: Press the alternate function pushbutton (12) followed by the keypad (11) AGC mode select key (the "3" key); use the lefthand select pushbutton (13) to select autorange. Observe the autorange mode indicator (26).

Select AGC: Press the alternate function pushbutton (12) followed by the keypad (11) AGC mode select key (the "3" key); use the righthand select pushbutton (13) to select the AGC function. Observe the AGC mode indicator (27).

Select gain display: Press the alternate function pushbutton (12) followed by the keypad (11) gain mode select key (the "2" key); use the lefthand select pushbutton (13) to select the desired gain display mode. Observe the absolute and delta gain mode indicators (27).

Select gain distribution: Press the alternate function pushbutton (12) followed by the keypad (11) gain mode select key (the "2" key); use the righthand select pushbutton (13) to select the desired gain distribution. Observe CW gain distribution indicator (27).

Select bandwidth mode: Press the alternate function pushbutton (12) followed by the keypad (11) bandwidth mode select key (the "." key); use the select pushbuttons (13) to select the desired bandwidth mode. Observe the external wideband mode indicator (28).

Select tuning step mode: Press the select step pushbutton (13) to select the stored step size as the increment/decrement value in tune mode; press the alternate function pushbutton (12) followed by keypad (11) step mode key ("4" key); then enter the desired step size; press the select step pushbutton to select ramped tuning upon return to tune mode.

Store panel settings: Press the alternate function pushbutton (12) followed by the keypad (11) store mode key (the "9" key); use the select pushbuttons (13) to select temporary, permanent, or powerup storage; enter the storage location number on the keypad; then press the H key to store the settings.

Recall panel settings: Press the alternate function pushbutton (12) followed by the keypad (11) recall mode key (the "6" key); use the select pushbuttons (13) to select temporary, permanent, or powerup storage; enter the storage location number on the keypad; then press the H key to recall the settings from storage.

Set IEEE-488 interface: Press the alternate function pushbutton (12) followed by the keypad (11) IEEE-488 mode key (the "C" key); use the left- and righthand select pushbuttons (13) to select MDC mode or remote control, and the center select pushbutton to enable/disable them; enter desired MDC or IEEE-488 address on the keypad followed by the H key to enter; use the tuning knob (29) or pushbuttons (14) to step the displayed address selection up or down.

Select Display Brightness: Press the alternate function pushbutton (12) followed by the keypad (11) brightness mode key (the "M" key); use the select pushbuttons (13) to select the desired display brightness; the selected brightness level will be stored in nonvolatile memory and will be applied at subsequent powerups as well.

Select Beeper Level: Press the alternate function pushbutton (12) followed by the keypad (11) beep mode key (the "K" key); use the select pushbuttons (13) to select beep mode and level functions; for beep level adjustments use the tuning knob (29) and pushbuttons (14) to adjust the desired beep level through the audio output connector (5) or front panel beeper (34).

Reset the receiver: Press the alternate function pushbutton (12) followed by the keypad (11) reset mode key (the "C" key) to enter reset mode; use the select pushbuttons (13) to select the desired reset function; use the keypad (11) H key to trigger the selected reset.

SCAN OPERATION:

Enter start frequency: Press the alternate function pushbutton (12) followed by the keypad (11) start mode key (the "0" key); enter the start frequency on the keypad.

Enter stop frequency: Press the alternate function pushbutton (12) followed by the keypad (11) stop mode key (the "1" key); enter the stop frequency on the keypad.

Enter step size: Press the alternate function pushbutton (12) followed by the keypad (11) step mode key (the "4" key); enter the step size on the keypad.

Enter step rate/repeat mode: Press the alternate function pushbutton (12) followed by the keypad (11) rate mode key (the "5" key); enter the step rate on the keypad (0 for maximum rate, uncalibrated); use the left- and righthand select pushbuttons (13) to select unidirectional, bidirectional, or no repetition; use the select step pushbutton to select continue or revert after pause.

Control scan: Press the alternate function pushbutton (12) followed by the keypad (11) scan mode key (the "8" key); use the select pushbuttons (13) to scan from start to stop (scan up key) or from stop to start (scan down key).

Adjust scan: During a scan, use the select pushbuttons (13): press the scan down pushbutton when scanning up to slow down the scan, or the scan up pushbutton to speed up. Press the scan up pushbutton when scanning down to slow down the scan, or the scan down pushbutton to speed up.

Pause scan and tune: During a scan, press the scan pause pushbutton (13) to temporarily halt the scan; use the tuning knob (29) or the tuning pushbuttons (14) to manually tune within the range of the scan start and stop frequencies, with steps equal to the scan step size. Press the scan up or scan down pushbutton to continue the scan in the indicated direction, or press the scan pause pushbutton again to continue the scan in the previously selected direction. Continuation will be from the last scan frequency if "revert" is selected, or from the currently tuned frequency if "continue" is selected.

Monitor X-axis output: Connect a monitoring device to the X-axis output connector (3); the output linearly tracks the progress of an ongoing scan.

Return to tune mode: Press the alternate function pushbutton (12) followed by the keypad (11) tune mode key (the "7" key) to resume tuning at the frequency at which the scan was terminated.

STATUS INDICATORS (25):

AC HI: Indicates that the AC line voltage is too high; check the AC voltage range switch (I); change the AC voltage subrange switch (J) to the next higher setting.

AC LO: Indicates that the AC line voltage is too low; check the AC voltage range switch (I); change the AC voltage subrange switch (J) to the next lower setting.

REG: Indicates that one or more of the DC supplies is out of regulation; check if the AC LO indicator is illuminated; if not then the receiver needs service.

UNLOCK: Indicates that one or more of the LO synthesizers is unlocked; flashes occasionally when tuning; if the indicator remains continuously illuminated then the radio needs service.

FR OVL: Indicates a front end overload: flashes for short overloads; for long overloads, increase the RF input attenuation.

BK OVL: Indicates a back end IF, DCIF, and/or video overload: flashes for short overloads; for long overloads decrease the IF gain setting.

BW LIM: Indicates that the tuned frequency is less than twice the selected bandwidth; decrease the bandwidth setting.

BW GAP: Indicates that the selected tuning step size is greater than the selected bandwidth, resulting in gaps in coverage when tuning; decrease the tuning step size or increase the bandwidth setting.

3.6 Detailed Operating Instructions

The following paragraphs describe the various receiver functions and their associated operational procedures. The reference numbers in the text are defined in tables 3-1 and 3-2, and are shown in figures 3-1 and 3-2.

The receiver includes audible indicators which sound when an operational limit is exceeded, or when an error condition or hardware fault is detected. A piezo transducer (34) is provided behind the front panel, and a beep tone is injected into the audio (headphone) output (5). Conditions which cause the indicators to sound are noted in the descriptions.

3.6.1 RF Input Pushbuttons, Indicators, and Connectors

The user may select one of two available RF inputs. Each input is provided with a connector (1)(2) on the front panel. Next to each connector is a pushbutton switch (7)(8), and in the middle of each button is an indicator LED. In order to select an input the operator presses the adjacent pushbutton. When this is done the pushbutton's LED will be illuminated and the LED of the other pushbutton extinguished, with the illuminated LED indicating the selected input. The input selection is also a remotely controllable function, with selection via the IEEE-488 interface; the appropriate indicator LED will be illuminated to show which input is currently selected. When in remote mode the pushbuttons will have no effect. In MDC mode the #1 input of the receiver is always selected, and the pushbuttons may be used to select the downconverter's input. When MDC mode is terminated, either by tuning the receiver below 1 GHz or by disabling the function entirely, input selection returns to that made before activating the MDC. When exiting remote mode, any selection made in that mode will be maintained until changed by the operator using the pushbuttons.

3.6.2 RF Input Attenuation Pushbuttons, Indicator, and Display

The user may select one of eight available RF input attenuation settings from 0 dB to 70 dB in 10 dB steps; the selected attenuation is shown on the four-character alphanumeric input attenuation display (20) in dB, for example "30dB". Selection is made by means of a pair of pushbuttons (9), one with an "up" arrow and the other a "down" arrow. Pressing the up arrow button increases the attenuation by 10 dB while pressing the down arrow decreases it by 10 dB. When an attempt is made to go below 0 dB of attenuation then the selection will stay at 0 dB and the audible indicator will sound. When an attempt is made to go above 70 dB of attenuation then the selection will stay at 70 dB and again the audible indicators will sound. Holding down one of the pushbuttons will cause the selection to step automatically after a short delay.

The autorange function makes use of the RF input attenuator. When this function is enabled the pushbuttons which normally control input attenuation are disabled. Instead, front end overload and underload signals are used to step the attenuator up and down to place the signal amplitude within the optimum range. When autorange is enabled the attenuation setting is shown on the display in parentheses, for example "(30)". The autorange indicator (26) is also illuminated. Autorange and its control are discussed in paragraph 3.7.10.

RF input attenuation is settable over the IEEE-488 interface. When in remote mode, autorange is disabled and the last selected value of attenuation is maintained until changed by an IEEE-488 interface command. In remote mode the up and down arrow pushbuttons are disabled, but the display will indicate all new selections made over the bus. When remote is terminated the last attenuation setting will be maintained until the operator changes it with the arrow pushbuttons. The autorange function is unavailable in remote.

In MDC mode the receiver's input attenuation is set to a fixed value and the control pushbuttons are used to set the input attenuation of the downconverter. The attenuation display will still indicate the setting of the R-110, however. If autorange is enabled in MDC mode then the downconverter's input attenuation is allowed to vary in response to its overload status signal, but the R-110's input attenuation remains fixed.

3.6.3 IF Gain Control, Indicators, and Display

User-controlled IF gain is settable over a 50 dB range, using the IF gain control (30) and the its display (21). Use of the IF gain control causes adjustments to be made in several places in the radio's signal path. The IF gain control is a high-resolution shaft encoder, while the IF gain display provides four alphanumeric characters. The display indicates the set gain value only to the nearest dB, but the adjustment granularity is about ten times smaller.

Rotating the control clockwise increases the gain in the 21.4 MHz IF, while rotating it counterclockwise reduces it. When the end of the adjustable range is reached the final value will be maintained and the audible indicators will sound.

The four characters of the IF gain display normally show the knob setting in dB, for example "12dB".

IF gain is affected by AGC, when enabled. A slowly varying voltage representative of signal level in the video output is routed back to some of the gain control stages in the 21.4 MHz IF, producing a feedback loop which tends to normalize the video output. When AGC is enabled, the setting of the front panel gain control is partly superceded, and so the displayed gain value is the knob setting shown in parentheses, for example "(30)". AGC and its selection are discussed in paragraph 3.7.10. When AGC is in use the front panel gain control should be set to maximum for the AGC to have full effect.

There are two kinds of options available for gain, one for distribution and one for display. Gain distribution may be optimized for either impulsive or CW signals. While either may be selected using a keypad function, the defaults are impulsive gain distribution for normal operation and CW distribution when the BFO is enabled. A gain mode indicator (27) illuminates when CW gain distribution is selected.

The IF gain display normally indicates the setting of the IF gain control knob. The other available gain display modes are "absolute" and "delta". In absolute mode the total gain through the receiver is shown, including the effects of the RF input attenuator, the IF gain control, and bandwidth compensating gain. The gain is displayed in dB as a signed integer. The value may be negative for high attenuation, low IF gain control setting, and wide bandwidth. Delta mode is similar except that the displayed value is calculated relative to the gain at the time that delta display mode was enabled. In other words, the display is initialized to zero when the mode is entered and incremented or decremented by changes in RF input attenuation, IF gain control setting, or IF bandwidth setting. The display is similar to that used for absolute display mode. When one of these modes is selected the associated gain mode indicator (27) will illuminate. When AGC is enabled its display supercedes those of the delta and absolute modes, since gain can no longer be indicated precisely.

Selection of gain options is discussed in paragraph 3.7.8.

Gain is a remotely controllable function. The same resolution that is available to the control is available over the IEEE-488 interface, but again the display only indicates it to the nearest 1 dB. When in remote mode the IF gain control knob is disabled, while the display updates on any settings made over the interface. The IF gain is displayed in the same format as knob gain, and if AGC is enabled the display will be similar to the display in local. When remote operation is terminated the last setting made is maintained until the operator changes it with the front panel gain control. In MDC mode the IF gain control operates as usual.

3.6.4 Bandwidth Pushbuttons, Indicator, and Display

Receiver IF bandwidth is selected using a pair of pushbuttons (10), one with an up arrow and the other a down arrow. The display (22) consists of four alphanumeric characters. The indication is given in digits and a multiplier, for example "300k". Pressing the up arrow key selects the next broader available bandwidth while pressing the down arrow key selects the next narrower available bandwidth. When an attempt is made to exceed the broadest or narrowest available bandwidth then the selection will be maintained and the audible indicators will sound. Holding down one of the arrow keys will cause selection to step repeatedly after a short delay.

The default set of bandwidths are those most commonly used, following a 1-2-5 sequence in the range covered by the DCIF. Since the DCIF is capable of providing many more bandwidths than this an expanded set may be selected using the keypad. Selection is discussed in paragraph 3.7.9. Once selected, operation of the bandwidth pushbuttons and the format of the display remain the same. The expanded set is selected so as to provide to make the noise normalization for each successive bandwidth increase by 1 dB per step.

Another available option, selected by the same means as the extended bandwidth selection mode, is external wideband mode. When selected, this mode routes the output of the 1450 MHz IF to a connector on the top of the microwave RF module in the cardcage, bypassing the 21.4 MHz IF, the video, and the audio. In this mode the bandwidth pushbuttons are disabled, the display indication is "EXT!" and the external wideband mode indicator (28) is illuminated. Tuning resolution is only to 5 MHz, and frequencies below 15 MHz are unavailable. The IF gain display (21) is also disabled. Bandwidth in this mode is about 200 MHz.

In MDC mode there is no change in the operation of the IF bandwidth controls or display.

IF Bandwidth is a remotely controllable function. When in remote mode the arrow pushbuttons are disabled. The display, however, is updated when bandwidth commands are received, so the display remains current. When remote mode is terminated the current bandwidth is maintained until the operator changes it with the pushbuttons.

3.6.5 Tuning Control, Pushbuttons, and Display

Tuning controls include the keypad (11), the tuning knob (29), the tuning pushbuttons (14), and the select pushbuttons (13). The tuning display (19) consists of twelve alphanumeric characters. The normal frequency display consists of digits and a decimal point, with a multiplier on the right-hand end, for example "100.00000MHz". Displayed resolution changes with the frequency to be displayed and can range from 0.1 Hz to 10 Hz.

Absolute tuning is accomplished by means of the keypad. The operator may enter digits and optionally a decimal point, followed by a terminator consisting of "M" for MHz, "K" for kHz, or "H" for Hz, depending on the way the digits and decimal point were entered. For example, a frequency of 1 MHz could be entered as "1M" or "1.000M" or "1000K" or "1000000H". If an error is made during the entry the "C" key may be pressed to clear it. Digits and the decimal point are presented on the frequency display as they are entered. Pressing a terminator key causes the entry to be evaluated and the nearest legal value accepted, set into hardware, and displayed in the standard format.

Stepped tuning is accomplished by means of the tuning knob and pushbuttons, and by the select pushbuttons. One digit of the tuning display may be selected for stepping by means of the left and right select pushbuttons. Pressing the left button advances the digit selection to the left, while the right pushbutton advances it to the right. In either case the selection will wrap around to the other end of the display if one button or the other is pressed enough times in succession, with one null selection intervening. Holding down either button will cause selection to step automatically after a short delay. The decimal point and multiplier characters, and also leading blanks, may not be selected.

A selected display digit will blink. This will be the digit referenced by the tuning knob anad pushbuttons. If a situation occurs in which a new frequency is set (e.g., via the keypad) for which the previously selected tuning digit is unavailable, then the decimal point will blink to indicate the condition. Stepping resolution remains that which was previously selected. An example of this is tuning the radio to 100 MHz, selecting the MHz digit for tuning, and then setting the radio to 10 kHz via the keypad. Since the MHz digit is unavailable for blinking, the decimal point is caused to blink instead.

Rotating the tuning knob clockwise will step the frequency upward, using the selected frequency display digit as the reference for step size. Similarly, rotating the knob counterclockwise will step the frequency downward. For example, if the display character representing the MHz digit of the frequency is selected, then the step size will be 1 MHz. Pressing the tuning pushbutton marked with an up-arrow will cause the frequency to increase by one step. Similarly, pressing the button marked with a down arrow will cause the frequency to decrease by one step. Holding either button down will cause the frequency to step repeatedly in the indicated direction after a short delay.

Pressing the center select pushbutton (marked "STEP") will cause the selection of a display digit to be cancelled. Instead, the stored step size specified as one of the scan parameters is used. When this mode is enabled the indicator LED inside the STEP pushbutton is illuminated. Tuning is otherwise the same as when a display digit is selected. Pressing the STEP button again will return to normal operation, as will pressing either of the arrow select buttons.

Entry of a stored step size is described in paragraph 3.7.5.

If the tuned frequency is less than twice the selected bandwidth then the BW LIM status indicator indicator (25) will illuminate and the audible indicator will sound. If the selected tuning step size is greater than the selected bandwidth then the BW GAP status indicator will illuminate.

One additional tuning option pertains to the manner in which frequency tuning is stepped up or down. In the default operating mode the step is made in a single jump, from the old frequency to the new one, subject to the speed at which the receiver's microprocessor can make all of the necessary hardware settings. At certain combinations of tuned frequency, step size, and selected bandwidth, operation in this mode can cause clicking in the audio, due to the sudden change in output level. The option, called "ramped tuning", causes tuning which under some circumstances might produce the clicking to be performed more gradually, with up to 16 microsteps per tune step. While this effectively changes the click to a buzz, the audible level of the buzz is theoretically lower since the change of output level between microsteps is smaller.

Ramp tuning may be selected as part of stored step size entry mode, as described in paragraph 3.7.5. Operation with the option enabled is considerably slower than normal when the tuned frequency, step size, and bandwidth selections make it most useful, but has no perceptible effect on operating speed otherwise.

In MDC mode both the downconverter and the receiver are tuned simultaneously. The necessary coarse resolution frequency is sent to the downconverter and the frequency appropriate to tune the desired frequency within the output of the downconverter is set into the receiver. In this mode both the receiver and the downconverter will display the tuned frequency rather than the frequencies actually set into them. When downconverter mode is exited the true tuned receiver frequency will be displayed.

In remote mode the tuned frequency may be set over the IEEE-488 interface. In addition, a step size may be entered and commands issued to step frequency up and down. When remote mode is exited the last frequency setting made will be maintained until changed manually by the operator.

3.6.6 Video Selection and Output

The video output (4) can be taken from either a log or a linear detector, with linear being the default selection. The LOG pushbutton (18) toggles selection between them. An indicator LED in the pushbutton illuminates when the log detector is selected.

Both the linear and the log detector may be selected in remote mode, but not the BFO. The linear detector is generally used. In remote mode the LOG pushbutton is disabled, but if the selection is changed by a bus command then the LED will be updated to indicate the current selection. When remote is exited any changes made while in remote will be maintained until the operator changes the selection again with the pushbutton.

3.6.7 Audio Output and Volume Control

The audio output (5) will drive headphones or a speaker, or any reasonable load down to a few Ohms. The audio volume control (31) sets the gain. At the counterclockwise end of the control's rotation there is zero output, while at the other end the output will be about 50 times the amplitude provided by the video circuit. The audio output signal includes an audible warning "beep" when an operational limit is exceeded; adjustment of this level is discussed in paragraph 3.7.14.

The input of the audio circuit is provided by an output of the video circuit. Since the gain for a given bandwidth is set to normalize the noise at the video output, in cases where the video bandwidth is greater than the audio range the noise in the audio output will not be normalized for different bandwidths. In effect this makes for quieter audio output at wider bandwidths. In addition, for CW or voice-type signals, there is greater apparent loudness at narrower bandwidths for any given setting of receiver and audio gain. This is the case regardless of whether impulsive or CW gain distribution is selected.

When BFO operation is selected the audio circuit monitors the BFO output rather than that of the video circuit. The video output remains normal, however. BFO operation is described in paragraph 3.6.8 below.

There is no control of the audio circuit available in remote mode, except that since BFO is likewise not controllable in remote, audio input selection reverts to the output of the AM detector in remote. In MDC mode the circuit functions normally.

3.6.8 BFO Control, Pushbutton, and Indicator

The BFO ("beat frequency oscillator") is used to detect unmodulated (or nearly so) CW signals. If the BFO is set to a slight deviation from the IF frequency then a "beat frequency" occurs at a frequency equal to the difference between the two. This beat frequency may be heard through the audio output connector (5). The BFO is settable over a +/- 4 kHz range by the BFO control (32). The associated pushbutton (15) is used to enable/disable the function. BFO takes the place of the normal AM detection link to the audio output, so that pressing the button to enable BFO takes the AM detector output off of the audio circuit. Pressing the pushbutton again restores the AM detector and turns off the BFO. A LED indicator located in the pushbutton illuminates when BFO is selected and is extinguished otherwise. Selection of BFO has no effect on the video output.

BFO is not a remotely settable or selectable function, and is disabled in the remote mode. It stays off when remote mode is exited, so the operator must then press the button to reselect it if it is desirable to do so. The button is disabled during remote mode. In MDC mode the circuit functions normally.

3.6.9 Z Axis Output Control, Pushbuttons, and Indicators

The Z axis output (C) is similar to the video output, but is located on the rear panel and has different controls. The output is provided to drive the Z axis (intensity) input of an oscilloscope. The Z axis control (33) adjusts the level, the polarity pushbutton (17) inverts the signal, and the select pushbutton (16) turns the output on and off. LEDs in the pushbuttons illuminate to indicate the state, with "on" and "inverted" cases producing illumination. When the transition from "off" to "on" is made, the last polarity set since powerup is selected. The powerup default polarity is normal.

The Z axis function is not remotely controllable. It is automatically disabled when entering remote. Operation in MDC mode is normal.

3.6.10 Signal Monitor and 21.4 MHz IF Outputs

There are two other signal outputs on the rear panel of the receiver, taken from two different points in the signal path. The first (B) is the signal monitor output, which is picked off of the 21.4 MHz IF before the gain control and bandwidth filtering stages. Full tuning resolution and range are available, and bandwidth is fixed at about 20 MHz, subject to the constraints of the input stages for the various tuning bands.

The second (D) is the 21.4 MHz IF output, taken this time from the same point which drives the DCIF and video sections, following the first gain control stage and the bandwidth filters. Again full tuning range and resolution are available, but now bandwidths down to 80 KHz are available, along with partial gain control.

3.6.11 Reference Oscillator Output

This rear-panel output (A) provides external monitoring and use of the receiver's internal reference clock. The frequency is 20 MHz, divided from the oscillator's 100 MHz, and the amplitude is -10 dBm.

3.6.12 X Axis Output

The X axis output (3) produces a 0 to +10 Volt ramp signal during programmed scans. It is provided to drive the horizontal input of an oscilloscope or X axis input of a plotter, to implement spectral presentations. It has no associated controls or indicators. The output is nonzero only during scan operations. At the start of a scan the output is set to 0 Volts and progresses in linear steps to +10 Volts at the stop frequency. Further discussion of scans is provided in paragraph 3.7.7.

The X axis output is unused in remote mode. Operation in MDC mode is normal.

3.6.13 Status Indicators

The status indicators (25) are alphanumeric indicators located in the upper portion of the tuning display window. Indicators are provided for synthesizer, overload, and power supply status, as well as for bandwidth and tuning step size selection errors. Lock status, overload, and power supply status is also available at the rear panel status connector and over the IEEE-488 interface.

The "AC HI" indicator illuminates when AC line voltage is too high for the current power supply input voltage selection. Change the line voltage range to the next higher setting using the subrange switch (J) on the rear panel. An AC high condition should not normally damage the radio unless it has inadvertently been switched to 117 VAC operation and used with a 220 VAC line. This condition is beyond the ability of the subrange switch to cope with and will almost certainly damage the radio.

The "AC LO" indicator illuminates when AC line voltage is too low for the current power supply input voltage selection. Change the line voltage range to the next lower setting using the subrange switch (J) on the rear panel. If the "REG" indicator is also illuminated in conjunction with the AC LO indicator then the line voltage is too low to be usable, given that the subrange switch is already in the LOW position.

The "REG" indicator illuminates when one or more of the power supply regulators is out of tolerance. It can be caused by the power line being out of tolerance (indicated by the "AC LO" indicator), or a problem in the receiver.

The "LOCK" indicator illuminates when one or more of the synthesizer's phase locked loops (PLLs) is out of lock. When all PLLs are in lock the indicator is extinguished. If one PLL is out of lock for just an instant the lightbar will give a quick flash. If the lightbar stays on the radio must be serviced.

The "FR OVL" indicator illuminates when an RF overload is detected. Detection is placed at the start of the 21.4 MHz IF, before the settable gain stages. For a short overload it gives a flash. For a long overload the input attenuation must be increased.

The "BK OVL" indicator illuminates when a 21.4 MHz IF, DCIF, or video overload is detected. For a short overload it gives a flash. For a long overload the IF gain setting must be decreased.

The "BW LIM" indicator illuminates when the selected IF bandwidth is greater than half of the tuned frequency. This is beyond what the hardware can cope with and will produce an erroneous output from the receiver. See paragraph 3.6.4.

The "BW GAP" indicator illuminates when the selected tuning step size is greater than the selected IF bandwidth, which will allow gaps in tuning coverage. For either continuous manual tuning or scanning the step size should always be less than the bandwidth.

3.7 Alternate Keypad Functions

Some receiver functions are selected and/or controlled using the keypad (11). Since the primary function of the keypad is to enter tuned frequencies, these other functions are called "alternate". They are accessed by pressing the alternate function pushbutton (12) which is placed in the lower righthand corner of the keypad layout. Pressing the alternate function pushbuttons will cause its internal indicator LED to illuminate to indicate that an alternate selection is pending. Pressing it again will cancel the pending condition and extinguish the indicator.

Once accessed, alternate keypad functions may be thought of as small-scale operating modes, in which the functions of the tuning display (19), the select pushbuttons and indicators (13), the keypad, and the tuning knob (29) and pushbuttons (14), are re-assigned to different uses. A chart of the use of these controls in each keypad-selected operating mode is given in table 3-5. The remaining front panel controls, indicators, and displays remain unaffected, save as a result of selection in one of these modes (e.g., absolute gain display mode, once selected, will change the IF gain display).

The keypad keys have their alternate functions printed above them. When an an alternate function is made pending using the alternate function pushbutton, any other keypad key may subsequently be pressed to access its designated alternate function.

A list of alternate functions is given in table 3-4.

Table 3-4: Alternate Keypad Functions

Keypad Key	Function
7	Tune Mode
8	Scan Mode
9	Store Settings Mode
M	Display Brightness Adjustment Mode
4	Scan Step Size Entry Mode
5	Scan Rate Entry Mode
6	Recall Settings Mode
K	Audible Indicator Control Mode
1	Scan Stop Frequency Entry Mode
2	Gain Options Select Mode
3	AGC Select Mode
H	IEEE-488 Interface Control Mode
0	Scan Start Frequency Entry Mode
.	Bandwidth Options Select Mode
C	Reset Select Mode

All of the alternate functions will be discussed in the following paragraphs.

3.7.1 Mode Indicators

There are ten mode indicators (23) located along the bottom of the tuning display (19) window. Indicators are provided for tune mode, start frequency entry mode, stop frequency entry mode, step size entry mode, scan rate entry mode, scan mode, store settings mode, recall settings mode, IEEE-488 interface control mode, and remote operating mode. All of these modes are mutually exclusive, so that only one of these indicators may be illuminated at any time. When one of the remaining alternate function modes is selected (display brightness selection mode, audible indicator amplitude setting mode, gain option selection mode, bandwidth option select mode, or AGC selection mode) all ten of the indicators are extinguished. In these cases the operating mode can be determined from the message on the tuning display.

3.7.2 Tune Mode

Tune mode is the default primary mode of operation of the receiver. Tune mode is entered from the other keypad-selectable modes by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated, and then pressing the keypad (11) key with "TUNE" marked above it (the "7" key). The TUNE mode indicator (23) will illuminate while the indicator LED in the alternate function pushbutton will be extinguished.

In this mode the tuned frequency is shown on the tuning display. Tuned frequencies may be entered via the keypad, or stepped by means of the tuning knob (29) and pushbuttons (14), with step resolution selected by the select pushbuttons (13). The procedure for entering parameters via the keypad is described in paragraph 3.6.5.

Two different methods of selecting tuning step size are available. Firstly, the STEP select pushbutton (13) may be pressed to select the stored step size (entered in step size entry mode, described in paragraph 3.7.5) as the size of each frequency step. Secondly, either the left or right select pushbutton may be pressed to select a digit of the tuning display (19) to designate the step size. See paragraph 3.6.5.

If an attempt is made to set the frequency beyond the limits of the receiver then the nearest legal setting will be substituted and the audible indicators will sound. When a step is generated using the tuning knob or pushbuttons which is beyond the limits of the receiver, the step is rejected and the existing value retained.

3.7.3 Start Frequency Entry Mode

Start frequency is one of the scan mode parameters, the nominal starting point of the scan. To enter this mode, first press the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "START" marked above it (the "0" key). The indicator LED in the alternate function pushbutton will extinguish and the START mode indicator (23) will illuminate. The tuning display (19) will show the last stored start frequency. The keypad digit and terminator keys may now be used to enter any start frequency from 1 kHz to 1 GHz. Entry of parameters via the keypad is discussed in paragraph 3.6.5.

The entered frequency will be stored for use by scan mode. Storage is in volatile memory, so the value will revert to the powerup default when power is cycled or when the receiver is reset.

3.7.4 Stop Frequency Entry Mode

Stop frequency is one of the scan mode parameters, the nominal end point of the scan. To enter this mode first press the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "STOP" marked above it (the "1" key). The indicator LED in the alternate function pushbutton will extinguish and the STOP mode indicator (23) will illuminate. The tuning display (19) will show the last stored stop frequency. The keypad digit and terminator keys may now be used to enter any stop frequency from 1 kHz to 1 GHz. Entry of parameters via the keypad is discussed in paragraph 3.6.5.

The entered frequency will be stored for use by scan mode. Storage is in volatile memory, so the value will revert to the powerup default when power is cycled or when the receiver is reset.

3.7.5 Step Size Entry Mode

Step size is one of the scan mode parameters, but it may also be used as the step size for normal tuning in tune mode. To enter this mode first press the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "STEP" marked above it (the "4" key). The indicator LED in the alternate function pushbutton will extinguish and the STEP mode indicator (23) will illuminate. The tuning display (19) will show the last stored step size. The keypad digit and terminator keys may now be used to enter any step size from 0.1 Hz to 1 GHz. Entry of parameters via the keypad is discussed in paragraph 3.6.5.

The entered value will be stored for use by tune mode or scan mode. Storage is in volatile memory, so the value will revert to the powerup default when power is cycled or the receiver reset.

Selection of stepped vs. ramped tuning is also made in this mode. The STEP select pushbutton (13) is used to toggle the selection. After pressing the pushbutton the new selection will be indicated on the tuning display. Ramped tuning is slower than stepped, since it breaks up the tuning step into a number of microsteps when the overall step is large in comparison to selected bandwidth. The purpose of ramped tuning is to reduce clicking in the audio due to sudden changes in output level resulting from relatively large shifts in tuned frequency. In practice the click is replaced by a chirp, but at a lower amplitude.

3.7.6 Scan Rate Entry Mode

This mode is used to set the scan rate, the scan repeat mode, and the action on resumption of a scan after a pause. To enter it first press the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "RATE" marked above it (the 5 key). The indicator LED in the alternate function pushbutton will extinguish and the RATE mode indicator (23) will illuminate. The tuning display (19) will show the last stored scan rate. The keypad digit and terminator keys may now be used to enter any scan rate from 0.01 to 10.00 steps per second. Alternatively a rate of zero may be entered to scan at the maximum possible (but uncalibrated) scan rate (about 25 steps per second). An illegal rate will be replaced by the nearest legal one. Entry of parameters via the keypad is discussed in paragraph 3.6.5.

The entered value will be stored for use by scan mode. Storage is in volatile memory, so the value will revert to the powerup default when power is cycled or the receiver reset.

Scan repetition mode is set using the left- and righthand select pushbuttons (13). Pressing either button selects, in sequence, either no repetition (single scan), unidirectional repetition, or bidirectional repetition. Unidirectional repetition repeats a scan beginning again at the initial frequency, whereas bidirectional repetition scans back and forth between the endpoints.

The center select pushbutton selects the scan resumption after pause option. Since manual tuning is possible during a scan pause, the tuned frequency when a scan is continued may not be the same as when the pause was initiated. Pressing the center select button to select the "CONTINUE" option will cause the scan to resume from the current frequency, whereas selecting the "REVERT" option will cause the scan to continue from where it left off. After pressing the select button the currently selected option will be shown on the tuning display.

3.7.7 Scan Mode

Scan mode is used to automatically step through a sequence of frequencies, using preselected values for start frequency, stop frequency, step size, step rate, and repetition. All of these are initialized to default values at powerup, but it is usually necessary to set each of them to desired values before commencing a scan. Each entry is made in a secondary operating mode, as described in the preceding paragraphs.

Scan mode is entered by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "SCAN" marked above it (the 8 key). The indicator LED in the alternate function pushbutton will extinguish while the SCAN mode indicator (23) will illuminate. The tuning display (19) will indicate the currently tuned frequency.

In scan mode the three select pushbuttons (13) are used to control the scan. The pushbuttons are given an alternate set of designations (printed below them) for this purpose. In this mode the pushbuttons are labeled "SCAN DOWN" (the left pushbutton), "SCAN PAUSE" (the center pushbutton), and "SCAN UP" (the right pushbutton). If a scan is not currently in progress, then pressing the SCAN UP pushbbutton will initiate a scan from the start frequency to the stop frequency. Pressing the SCAN DOWN pushbutton will initiate a scan from the stop frequency to the start frequency. Upon reaching the end of its range, the scan will either halt, reverse itself, or start over, depending upon the setting of the scan repeat mode. The indicator LED inside whichever pushbbutton is pressed will illuminate while the scan is running.

If a scan is running, then pressing the same pushbutton used to initiate the scan will cause it to speed up, up to the maximum executable rate of about 25 steps per second. Pressing the opposite pushbutton will cause the scan to slow down. Each press will cause the rate to approximately double or halve, respectively.

Pressing the SCAN PAUSE pushbutton while a scan is running will cause the scan to be suspended but not cancelled. Pressing the pushbutton again will cause it to resume. Alternatively, pressing either the SCAN UP or SCAN DOWN pushbuttons during a pause will cause the scan to resume in the desired direction.

During a pause the indicator LED in the SCAN PAUSE pushbutton will illuminate. At this time the tuning knob (29) and pushbuttons (14) may be used to step the frequency manually, using the scan step size as the increment or decrement. The tuning range is limited to the range of the scan. Ramped tuning is unavailable in this mode.

Resumption of the scan after a pause may be made from either the currently tuned frequency or from the frequency at which the pause was initiated. Selection of either option is made in the same submode in which scan rate and repetion mode is selected.

When not scanning or paused the radio may be tuned normally using the keypad, tuning knob, and tuning pushbuttons, using the stored step size as the tuning resolution.

3.7.8 Gain Options Select Mode

There are two kinds of gain option selections available, one for gain distribution and one for gain display. Distribution can be optimized for either impulsive or CW signals, impulsive being the factory-set default for normal operation and CW being the default when the BFO is enabled. The IF gain display can indicate either the gain control knob setting, or the total gain of the radio, or gain relative to a reference level, in which changes in input attenuation and bandwidth-compensating gain are also tracked. For a discussion of these options see paragraph 3.6.3.

The mode is entered by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "GAIN" marked above it (the "2" key). The indicator LED in the alternate function pushbutton will extinguish while the tuning display (19) will indicate the currently selected gain options. No mode indicator (23) will be illuminated.

Selections are made using the select pushbuttons (13). The lefthand pushbutton selects the display mode while the righthand pushbutton selects the distribution mode. The center pushbutton selects the default combination of both. Both modes are indicated on the tuning display simultaneously, the display mode on the left and the distribution mode on the right. In addition, when CW gain distribution, or absolute or delta gain display mode is selected, the appropriate gain mode indicator (27) will illuminate.

Gain display selection depends on whether or not AGC is enabled. If enabled, the AGC mode gain display will supercede the selection made with the select pushbuttons.

Gain distribution selection depends on whether or not BFO is enabled. The selections with BFO enabled and disabled are independent, as are the defaults. Changing the BFO selection may change the gain distribution selection as well.

All options are available in MDC mode. Only gain distribution selection is available in remote mode, though not from the front panel.

3.7.9 Bandwidth Options Select Mode

More bandwidths are available than those provided in the default selection. To make all of them selectable an extended bandwidth selection option is provided. All of these extra bandwidths are at the narrow end of the range, provided by the DCIF. At the wide end, a wideband selection is available for future expansion. If selected, the tuning range of the radio will be limited to 15 MHz at the low end, the tuning resolution will be limited to 5 MHz steps, and the signal path will be truncated after conversion to the 1450 MHz IF. See paragraph 3.6.4 for more discussion.

The mode is entered by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "BW" marked above it (the "." key). The indicator LED in the alternate function pushbutton will extinguish while the tuning display (19) will indicate the currently selected bandwidth option. No mode indicator (23) will be illuminated.

Selections are made using the select pushbuttons (13). Only one option may be selected at any given time. The left and right pushbuttons step through the selections, while the center pushbutton causes selection to revert to the default condition. When external wideband mode is selected the WIDE indicator (28) will illuminate.

All options are available in MDC mode. Extended narrowband selection is the normal case in remote mode, and external wideband mode is available as well, though it is not selectable from the front panel in remote.

3.7.10 AGC Select Mode

There are two sorts of automatic gain control (AGC) available. The first sort, called autorange, reacts to the signal amplitude at the front of the 21.4 MHz IF by stepping the RF input attenuator up or down. Since the RF input attenuator steps in 10 dB increments, this is a coarse adjustment. The second sort of AGC, back end AGC, reacts to the signal amplitude in the video section by adjusting the gain in the 21.4 MHz IF. This is an analog feedback and gain control with continuous and fairly rapid response, though over a slightly narrower dynamic range. Throughout this manual, the term "AGC" refers to back end AGC only. See paragraph 3.6.3 for more discussion.

When autorange is enabled the attenuation pushbuttons (9) are disabled.

When AGC is enabled the IF gain display automatically shifts to AGC display mode. This overrides any other gain display mode which may be selected, except that if external wideband mode is selected then there is no gain display at all, since the controlled gain stages are no longer in the signal path.

AGC select mode is entered by pressing the alternate function pushbutton (12) so that the indicator LED in the pushbutton is illuminated. Then press the keypad (11) key with "AGC" marked above it (the "3" key). The indicator LED in the alternate function pushbutton will extinguish while the tuning display (19) will indicate the currently selection of AGC and autorange. No mode indicator (23) will be illuminated.

Selections are made using the select pushbuttons (13). The lefthand pushbutton toggles autorange on/off while the righthand pushbutton does the same for AGC. The center pushbutton selects the default condition, which in the factory-provided selection is with neither selected. The AUTO indicator (26) illuminates when the function is enabled. Likewise, the AGC indicator (27) illuminates when AGC is enabled.

Both sorts of gain control are available in MDC mode, noting that autorange will affect the input attenuation of the MDC rather than that of the R-110 when tuning is in the downconverter range. Only AGC is available in remote mode.

3.7.11 Store Settings Mode

To store the current front panel settings, first press the alternate function pushbutton (12) so that the indicator LED inside is illuminated. Then press the keypad (11) key with "STORE" marked above it (the "9" key). The indicator LED in the alternate function pushbutton will extinguish and the STORE mode indicator (23) will illuminate. A prompt will be shown on the tuning display (19). Using the select pushbuttons (13), select the type of storage to be used: temporary, permanent, or powerup (which is also permanent). Using the keypad (11), enter the location number in which to store the settings (0 - 99) if temporary or permanent storage is selcted (this is unnecessary if powerup storage is selected). Finally, press the "H" key to store the settings. The following settings will be stored:

- Current tuned frequency
- Current scan start frequency
- Current scan stop frequency
- Current step size
- Current scan rate
- Current input selection
- Current input attenuation
- Current gain
- Current bandwidth
- Current AGC selections
- Current gain options
- Current bandwidth options
- Current tuning options
- Current scan options
- Current slideback on/off state (not the adjustment)
- Current pulse stretch on/off state (not the adjustment)
- Current BFO on/off state (not the adjustment)
- Current Z axis on/off and invert states (not the adjustment)
- Current log/lin detector selection
- Current audible indicator on/off states (not the amplitudes)
- Current MDC enable or GPIB enable

The following are NOT stored:

- Slideback threshold adjustment
- Pulse stretch adjustment
- BFO frequency adjustment
- Z axis output amplitude adjustment
- Audio output amplitude adjustment
- Audible indicator amplitudes
- Display brightness
- Current GPIB address (read from dipswitch at powerup)
- Current MDC address (not expected to change often)

Once the operation has been completed a message will be provided on the tuning display indicating whether the settings were stored in temporary or permanent memory.

3.7.12 Recall Settings Mode

Most of the front panel control settings may be recalled from previous storage and set into hardware. This is the companion function to the store settings mode described in the previous paragraph, and operation is similar.

To recall stored control settings, first press the alternate function pushbutton (12) so that the indicator LED inside is illuminated. Then press the keypad (11) key with "RECALL" marked above it (the "6" key). The indicator LED in the alternate function pushbutton will extinguish and the RECALL mode indicator (23) will illuminate. A prompt will be shown on the tuning display (19). Using the select pushbuttons (13), select the type of storage to be accessed: temporary, permanent, or powerup. Using the keypad (11), enter the location number from which to recall the settings (0 - 99). Finally, press the "H" key to perform the recall. For powerup storage only the terminator is needed. The following settings will be recovered and set into hardware:

- Current tuned frequency
- Current scan start frequency
- Current scan stop frequency
- Current step size
- Current scan rate
- Current input selection
- Current input attenuation
- Current gain
- Current bandwidth
- Current AGC selections
- Current gain options
- Current bandwidth options
- Current tuning options
- Current scan options
- Current slideback on/off state (not the adjustment)
- Current pulse stretch on/off state (not the adjustment)
- Current BFO on/off state (not the adjustment)
- Current Z axis on/off and invert states (not the adjustment)
- Current log/lin detector selection
- Current audible indicator on/off states (not the amplitudes)
- Current MDC enable or GPIB enable

The following are NOT recovered:

- Slideback threshold adjustment
- Pulse stretch adjustment
- BFO frequency adjustment
- Z axis output amplitude adjustment
- Audio output amplitude adjustment
- Audible indicator amplitudes
- Display brightness
- Current GPIB address (read from a dipswitch at powerup)
- Current MDC address (not expected to change often)

Once the operation has been completed the tuned frequency will be shown on the tuning display. About one second later a message will be provided on the tuning display indicating whether the settings were read from temporary or permanent memory.

If a location is read in which no data was previously stored then the default powerup settings will be read and set into hardware.

3.7.13 Display Brightness Selection Mode

The alphanumeric displays (19)(20)(21) are capable of four brightness levels, one of which is "off". To change the current brightness setting, press the alternate function pushbutton (12) so that the indicator LED located inside is illuminated. Then press the keypad (11) key with "BRIGHT" marked above it (the "M" key). The indicator LED in the alternate function pushbutton will extinguish and a mode message will appear on the tuning display (19), assuming that "off" is not already selected. No mode indicator (23) will be illuminated. The select pushbuttons (13) may now be used to step the selected brightness level. Note that only the brightness of the alphanumeric displays is affected, not that of the status indicators (25) or mode indicators (23)(26)(27)(28), and not that of the indicator LEDs located inside some of the pushbuttons. The selected brightness level is stored in nonvolatile memory so that it will be read and restored even after power is cycled.

3.7.14 Audio Indicator Selection and Adjustment Mode

There are two audible indicators. One is a piezo transducer (34) located behind the front panel, while the other is a feed into the audio output circuit. The amplitude of each may be adjusted independently. In addition, various triggers for the indication may be switched on and off.

To enter the adjustment mode press the alternate function pushbutton (12) so that the indicator LED located inside is illuminated. Then press the keypad (11) key with "BEEP" marked above it (the "K" key). The indicator LED in the alternate function pushbutton will extinguish and the tuning display (19) will show a mode status message. No mode indicator (23) will be illuminated. The left and right select pushbuttons (13) may now be used to select the desired beep function. Beep triggers consist of the following:

- Limit beep. Indicates the end of a control range. For example, rotating the gain control past the 50 dB position. This produces a short beep.

- Error beep. Indicates an unacceptable keypad entry. For example, entering a tuned frequency below 1 KHz. This produces a long beep.

- Fault beep. Indicates a lock status, overload, or DC regulation fault. This produces a repeating beep which persists for the duration of the fault.

Each of the preceding may be individually switched on or off as a trigger source to the indicator, using the center select button.

The amplitude of the beep at the transducer or the audio output may be adjusted by first selecting the level adjustment mode for the desired beep type using the select keys, and then using the tuning knob (29) and pushbuttons (14) to select the desired level. The final value will be stored in permanent memory and will be re-established each time the radio is powered up. One indicator or the other may be effectively turned off by decreasing its level to inaudibility.

3.7.15 MDC Mode

MDC mode allows automatic control of a model R-1180 microwave downconverter using the IEEE-488 interface. In this mode the R-110 becomes the interface controller, commanding the downconverter and reading back status. The R-110 allows control of the downconverter's RF input selection, RF input attenuation, and tuned frequency using the R-110's front panel controls. The tuned frequency and RF input attenuation of the R-110 is automatically adjusted to the output range of the downconverter. RF input #1 (1) of the R-110 is dedicated to the downconverter output, with the other input still available for frequencies below the downconverter's range.

Two connections are required between the downconverter and the R-110. A signal cable with response to 1 GHz is used to connect the downconverter output to RF input #1 (1) on the R-110. An IEEE-488 interface cable must also be connected between the units.

Once the MDC is connected, the R-110 must also be made aware of it. This is done in IEEE-488 interface control mode. To enter this mode press the alternate function pushbutton (12) so that the indicator LED located inside is illuminated. Then press the keypad (11) key with "GPIB" marked above it (the "H" key). ("GPIB" stands for "General Purpose Interface Bus", another name for the IEEE-488 Interface.) The indicator LED in the alternate function pushbutton will extinguish and GPIB mode indicator (23) will illuminate. The tuning display (19) will show a mode status message. The left or right select pushbuttons (13) may now be used to select the MDC mode status message. Then press the center select pushbutton so that MDC operation is enabled and the presumed MDC address is displayed.

The interface address of the MDC may now be entered using the keypad or the tuning knob (29) and pushbuttons (14). If the keypad is used then the desired address should be keyed in, followed by the "H" key as a terminator. The address will be stored in nonvolatile memory and will be recalled on powerup.

Tune mode may now be reselected. No communication with the MDC will occur until the R-110 is tuned above 1 GHz. Upon exceeding 1 GHz the MDC will be placed in remote and left in remote until either it or the R-110 is switched off, or MDC mode is disabled in GPIB select mode, using the center select key. In other words, when the MDC address is displayed, MDC operation is enabled at that address. When the mode is toggled to indicate "no MDC" the mode is disabled.

Operation of the R-110 with the MDC enabled is similar to normal operations, with the following exceptions:

- RF input selection operates normally when the radio is tuned below 1 GHz. Above 1 GHz RF input #1 will be automatically selected and the RF input select pushbuttons (7,8) remotely control input selection for the downconverter. When the radio is tuned back below 1 GHz the radio's previous input selection is recalled.

- RF input attenuation operates normally when the radio is tuned below 1 GHz. Above 1 GHz a fixed attenuation is selected and shown on the attenuation display (20), while the attenuation pushbuttons (9) remotely control RF input attenuation selection for the MDC. When the radio is tuned back below 1 GHz the radio's previous input attenuation is recalled. The autorange function operates normally below 1 GHz, while above 1 GHz it remotely controls the MDC's RF input attenuator. It does this by polling the status return byte of the MDC and stepping the attenuator based on the state of the overload status bit. Since there is no matching underload status bit as is provided in the R-110, this is a fairly rudimentary form of control.

- Tuning operates normally below 1 GHz. Above 1 GHz, tuning still presents the normal interface to the operator, but will automatically determine the proper frequencies to which to tune both the radio and the MDC. The output of the MDC is in the 800 - 900 MHz range, so if an interface error occurs then the tuned frequency of the radio will revert to this range. The range of scan frequencies is extended to 18 GHz when the MDC is enabled.

- IF bandwidth selection operates normally both below and above 1 GHz. The bandwidth of the MDC is about 400 MHz, so it presents no limitation when the radio has wideband selected (the front end of the radio has about 200 MHz bandwidth).

Remote operation of the R-110 is not feasible in MDC mode. Enabling MDC mode will disable GPIB mode.

Downconverter command formats are not covered by this document, but are listed in documentation supplied with the downconverter.

3.7.16 Remote Mode

In remote mode an external host computer is in control of the receiver, using the IEEE-488 interface. In remote most of the front panel controls are disabled. Those that are still functional include:

- The power switch (6)
- The audio volume control (31)
- The BFO tuning control (32) (BFO is disabled)
- The Z axis output level control (33) (Z axis is disabled)
- The ALT pushbutton (12)
- The keypad (11) C key (when an alternate function is pending)

All displays and indicators remain functional. The only available keypad function is ALT-RESET, which returns the receiver to local if local has not been locked out.

The receiver is accessed over the IEEE-488 interface via an address which is read from a dipswitch at powerup. This dipswitch is located on the processor PCB and the procedure for setting it is given in chapter 2. While in local mode the address may be changed temporarily in IEEE-488 interface mode. See paragraph 3.7.17.

Commands are provided in remote which control:

- RF input selection
- RF input attenuation
- IF gain
- IF gain distribution
- AGC (not autorange)
- IF bandwidth, and external wideband selection
- Tuned frequency
- Tuning step size, and step up and down
- Video detector selection
- Store and recall of settings
- Status reporting

Functions which are always disabled in remote include:

- BFO
- Z axis
- X axis
- Audible indicators
- Display brightness selection
- MDC operation under control of the R-110

MDC operation is nevertheless supported, with the IEEE-488 interface host computer controlling both instruments independently.

Additional commands are provided which allow reporting of various radio settings over the bus, and for low-level control of IF gain. In addition, commands are provided which load and read back data to and from the calibration tables in the radio's nonvolatile read/write store, so that the IEEE-488 interface may be used for automated calibration.

Note that for a more efficient remotely controlled system the radio's rear panel status outputs should be connected to a separate interface in the remote system's host computer. This permits the IEEE-488 interface to remain permanently in sending mode while still monitoring status for overloads. Turning the bus around from sending to receiving is a major slowing factor for most IEEE-488-based systems.

Remote mode command formats, protocols, and supported functions are described in detail in appendix A.

3.7.17 IEEE-488 Selection Mode

The IEEE-488 interface may be used to control an external R-1180 microwave downconverter or be used to allow an external host computer to control the R-110. These two options are not available simultaneously. If a downconverter is to be employed in remote mode then it is the responsibility of the computer controlling the interface to command it. If the R-110 has control of the interface in order to command the downconverter then an external host computer will not be able to take control.

An interface address for the R-110 is read from a dipswitch on the processor PCB at powerup. This address may be changed temporarily, but the change will be lost when power is removed. It is recommended that once an address is selected it be permanently set using the dipswitches. See section 2 for the procedure.

An interface address for the external downconverter is read from nonvolatile memory on powerup. This address may be changed as well, and the new selection will be saved in nonvolatile memory.

Address and downconverter selection are performed in a keypad submode dedicated to IEEE-488 interface-related options, called GPIB mode. The mode is selected by pressing the alternate function pushbutton (12) so that the indicator LED inside is illuminated. Then press the keypad (11) key with "GPIB" marked above it (the "H" key). The indicator LED in the alternate function pushbutton will extinguish and the GPIB mode indicator (23) will illuminate. The tuning display (19) will show a status message. The left and right select pushbuttons (13) may now be used to select MDC or GPIB control. In each case the center select pushbutton (13) may be used to toggle the selection on and off, while the keypad, tuning knob (29) and pushbuttons (14) may be used to change the displayed address when the selection is enabled. Legal addresses range from 0 to 30. When using the keypad, enter the desired address followed by the "H" key to terminate the entry, or the "C" key to revert to the old one. A new MDC address will be stored in permanent memory, whereas a new GPIB address will be held only until powerdown.

The MDC address should always be different from the R-110's own GPIB address. The R-1180 MDC comes factory-set to address 12, but this may be changed by the user. See the downconverter's documentation for details. The R-110 comes factory-set with address 16 set on the dipswitch.

This mode may be used to return an MDC to local, by setting the mode to "No MDC". When in remote this mode is unavailable, but the R-110 may be returned to local by pressing the alternate function pushbutton followed by the key with RESET marked above it ("C" key).

3.7.18 Reset Mode

Reset mode handles four sorts of resets: the IEEE-488 interface, temporary storage, permanent storage, and the entire radio.

The IEEE-488 interface reset function gets the radio off of the bus without forbidding later access. Whereas disabling both remote and MDC operation in GPIB mode (described in the preceding paragraph) will result in holding the IEEE-488 interface controller circuit in reset, using the function presented here will reset the controller and leave it in idle mode, ready to be used again. This is done by releasing control of the MDC (when MDC mode is enabled) or by returning the radio to local if it is in remote (provided local lockout has not been commanded). Note that when the radio is in remote, selecting reset mode will automatically return the radio to local without presenting the operator with the normal interface, storage, and general reset options.

Memory resets reload the selected storage with powerup data, removing any settings stored since powerup.

Resetting the entire radio reboots the control system and returns the radio to its powerup state. Note that a reset switch located on the processor PCB may also perform this function, but the pushbutton is not accessible when the radio's cover is in place.

To enter reset mode, first press the alternate function pushbutton (12) so that the indicator LED inside is illuminated. Then press the keypad (11) key with "RESET" marked above it (the "C" key). The tuning display (19) will indicate the currently selected reset function. No mode indicator (23) will be illuminated. Use the select pushbuttons (13) to select the desired function. Then press the keypad "H" key to trigger the reset.

Table 3-5: Sub-Mode Control Functions

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Tune	Tune from selected frequency display digit	Move digit selection left with wraparound	Enter "tune stored step size" sub-mode	Move digit selection right with wraparound	Enter tuned frequency	Step tuned frequency up or down by amount of selected digit
	Tune stored step size	Enter "tune selected digit" sub-mode with selected digit one left of last	Enter "tune selected digit" sub-mode with last selected digit	Enter "tune selected digit" sub-mode with selected digit one right of last	Enter tuned frequency	Step tuned frequency up or down by amount entered in step size mode
Start					Enter scan start frequency	
Stop					Enter scan stop frequency	
Step			Toggle ramp tune option on/off		Enter scan/tune step size	
Rate		Select scan repeat option: no repeat, unidirectional, bidirectional	Toggle continue/ revert after scan pause option	Select scan repeat option: no repeat, unidirectional, bidirectional	Enter scan rate	

Table 3-5 Continued

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Scan	Idle	Start scan stop → start		Start scan start → stop		Step tuned frequency up or down by stored step size, no start/stop limits
	Scanning towards stop	Slow down scan rate	Enter pause sub-mode	Speed up scan rate		
	Scanning towards start	Speed up scan rate	Enter pause sub-mode	Slow down scan rate		
	Pause	Restart scan towards start	Restart scan in last active direction	Restart scan towards stop		Step tuned frequency up or down by stored step size, limited to range between start & stop frequencies
Store		Select store: temp, permanent, powerup	Select default (temporary) storage	Select store: temp, permanent, powerup	Enter storage location number for temp and permanent, just "H" for powerup	

Table 3-5 Continued

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Recall		Select store: temp, permanent, powerup	Select default (temporary) storage	Select store: temp, permanent, powerup	Enter storage location number for temp and permanent, just "H" for powerup	
Bandwidth		Select normal, extended, or wideband	Select default (normal) bandwidth	Select normal, extended or wideband		
Gain	BFO Off	Select knob, absolute, or delta display	Select defaults: knob display, impulsive distribution for no BFO only	Select impulsive or CW distribution for no BFO only		
	BFO On	Select knob, absolute, or delta display	Select defaults: knob display, CW distribution for BFO only	Select impulsive or CW distribution for BFO only		
AGC		Toggle autorange on/off	Select defaults: autorange off, AGC off	Toggle AGC on/off		
Brightness		Select display brightness down, with wraparound	Select default display brightness: full	Select display brightness up, with wraparound		

Table 3-5 Continued

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Beep	Fault Beep	Select "panel beep level" sub-mode	Toggle fault beeps on/off	Select "error beep" sub-mode		
	Error Beep	Select "fault beep" sub-mode	Toggle error beeps on/off	Select "limit beep" sub-mode		
	Limit Beep	Select "error beep" sub-mode	Toggle limit beeps on/off	Select "beep level" sub-mode		
	Audio Beep Level	Select "limit beep" sub-mode		Select "panel beep level sub-mode		Step beep level in audio output up/down
	Front Panel Beep Level	Select "audio beep level" sub-mode		Select "fault beep" sub-mode		Step beep level in panel beep up/down
GPIB	Remote operation	Select MDC sub-mode	Toggle remote enable on/off	Select MDC sub-mode	Enter bus address if remote enabled	Step bus address up/down if remote enabled
	MDC operation	Select remote sub-mode	Toggle MDC enable on/off	Select remote sub-mode	Enter MDC address if MDC enabled	Step MDC address up/down if MDC enabled

Table 3-5 Continued

Mode	Sub-Mode	◂ Select	Step	Select▸	Keypad	Tuning Knob, Pushbuttons
Reset	Reset Radio	Select "reset GPIB" sub-mode		Select "reset perm" sub-mode	"H" key triggers radio reset	
	Reset Perm	Select "reset radio" sub-mode	Select default (radio) sub-mode	Select "reset temp" sub-mode	"H" key clears permanent store	
	Reset Temp	Select "reset perm" sub-mode	Select default (radio) sub-mode	Select "reset GPIB" sub-mode	"H" key clears temp store	
	Reset GPIB	Select "reset temp" sub-mode	Select default (radio) sub-mode	Select "reset radio" sub-mode	"H" key resets GPIB controller	
Remote					Alt followed by "C" forces return to local if no lockout	

SECTION 4. THEORY OF OPERATION

4.1 Introduction

The model R-110 is a wide range superheterodyne receiver that is continuously tunable, covering the frequency range from 1 kHz to 1 GHz in three bands. See table 4-1. The receiver detects RF signals in the form of continuous wave (CW) or amplitude modulated carriers.

Table 4-1: Receiver Tuning Bands

Band	Tuning Down	Tuning Direct	Tuning Up
1	1 kHz - 224.9999 kHz	1 kHz - 249.9999 kHz	1 kHz - 264.9999 kHz
2	225 kHz - 13.4999999 MHz	250 kHz - 14.9999999 MHz	265 kHz - 16.4999999 MHz
3	13.5 MHz - 1 GHz	15 MHz - 1 GHz	16.5 MHz - 1 GHz

The breakpoints between bands for "direct tuning" are the nominal values, those which will be obtained by direct frequency entry using the keypad or IEEE-488 interface, or during scans. Hysteresis is introduced when using the tuning knob or pushbuttons, or the IEEE-488 step commands, or when tuning manually during a scan pause. This hysteresis provides the offset breakpoints shown for "tuning up" and "tuning down".

Note that when external wideband mode is selected, band 1 and band 2 are eliminated and the nominal band 3 break is the lower tuning limit of the radio whether tuning is up, down, or direct. Also, when operating in MDC mode with the external R-1180 microwave downconverter in the signal path, the tuning range inside the radio is 800 - 900 MHz. Although this falls within band 3, it is given its own designation, band 4, due to a number of special conditions that are necessary in this mode. Finally, limitations of synthesizer usage cause band 3 to be broken up into two pieces, called band 3A and band 3B. Band 3A is the first 5 MHz of band 3, regardless of where the band break occurs. This is discussed further in the description of the programmable microwave synthesizer.

The major functional parts of the receiver are:

- RF: processes RF inputs; converts to 21.4 MHz IF; implemented with three modules (A1A1, A1A2, A1A5) plus front-panel components.
- IF: performs wider bandpass filtering, AGC and programmable gain; consists of two modules (A1A6 and A1A8).
- DCIF: performs narrow-band filtering, programmable gain, and linear AM detection; implemented in a single module (A1A11).
- video: provides AM detection of wider bandwidths; provides log response; provides BFO detection; provides buffered video, Z axis, and audio outputs; implemented in a single module (A1A9).

- synthesizer: provides LO signals for frequency conversion; consists of three modules (A1A15, A1A16, A1A17) plus components in RF section.
- control: controls operation of all modules; includes front panel; contained in front panel assembly (A2A1, A2A2, A2A3).
- power supply: provides regulated power to receiver circuits using linear design to minimize EMI; contained in rear panel assembly (A3).

The simplified block diagram of figures 4-1 - 4-5 shows how the sections are interconnected (a detailed block diagram is included in section 6). The RF section uses three parallel signal paths that divide the input range into specific frequency bands, as listed in table 4-1. The signal paths contain mixer circuits used to heterodyne the tuned input signal to the 21.4 MHz intermediate frequency. The 21.4 MHz IF section provides amplification and selectable bandpass filtering. For the wider bandwidths, the 21.4 MHz IF section's output is routed to the video section which provides the audio and video output signals. For narrow bandwidths, the IF signal goes to the DCIF section where it is processed and detected.

The synthesizer section utilizes a precision direct digital synthesizer (DDS) and phase locked loop (PLL) circuits to create the required local oscillator signals, thus providing accurate frequency control and high resolution.

The power supply section of the receiver provides individually regulated DC voltages from a selection of six ranges of AC input power.

Physically, the radio consists of a front panel assembly (A2), a cardcage assembly (A1), and a rear panel assembly (A3). The front panel assembly contains the controlling microprocessor and also the RF input selection and distribution relays, and the RF input attenuator. The cardcage assembly is provided with a backplane which routes control and status signals from the front panel assembly to the various plug-in modules, and provides power to them as well. Analog and RF signal lines are routed across the tops of the modules using discrete coax cables, both flexible and semi-rigid. The rear panel assembly contains the power supply and cooling fan. The front panel assembly, cardcage assembly, and rear panel assembly bolt together to form a chassis, which may then slide into a one-piece cover, with the result being the assembled radio. Discussions following in this section will deal more or less individually with the front and rear panel assemblies, the cardcage assembly, and the various plug-in modules.

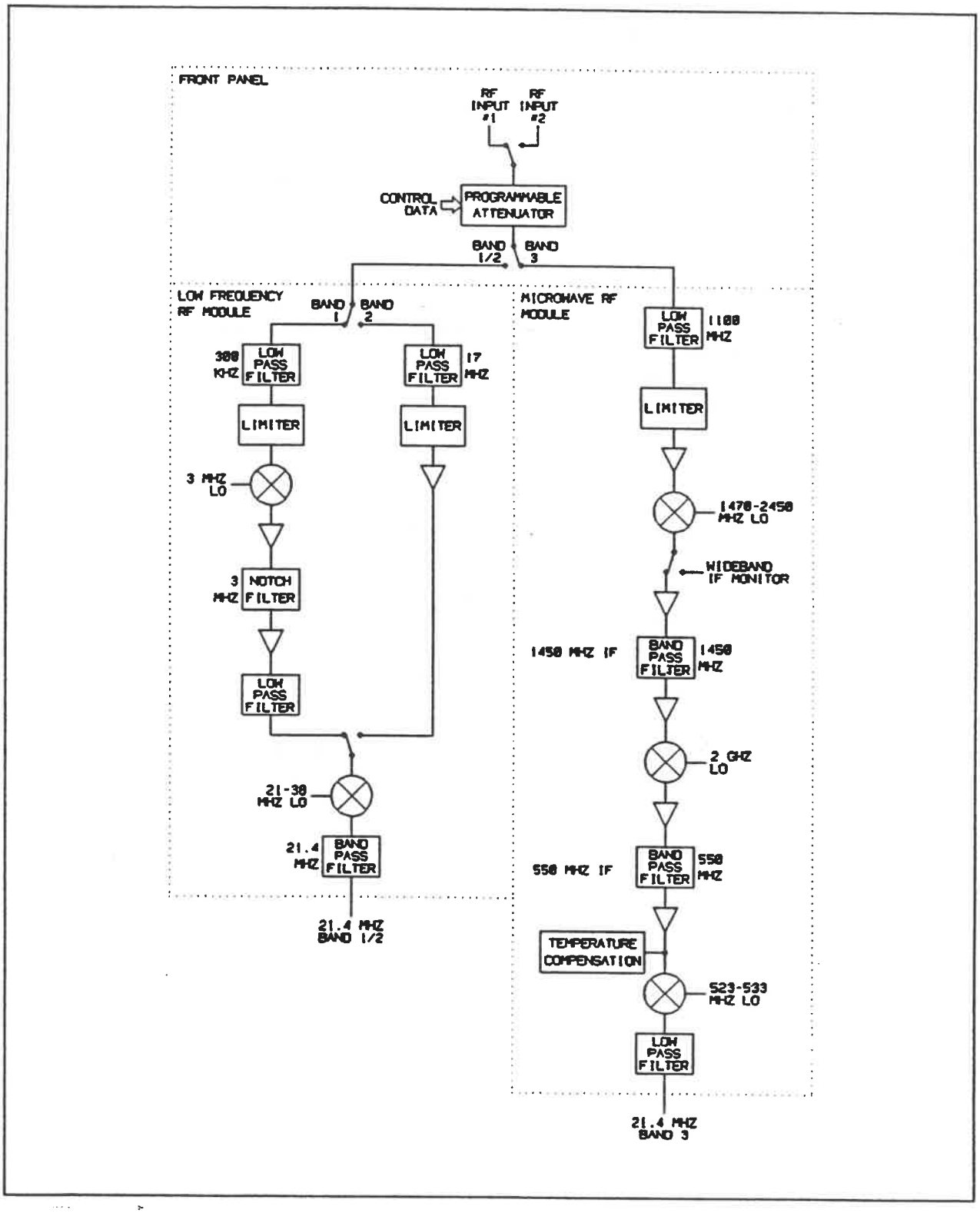


Figure 4-1: R-110 Receiver Simplified Block Diagram - Part 1

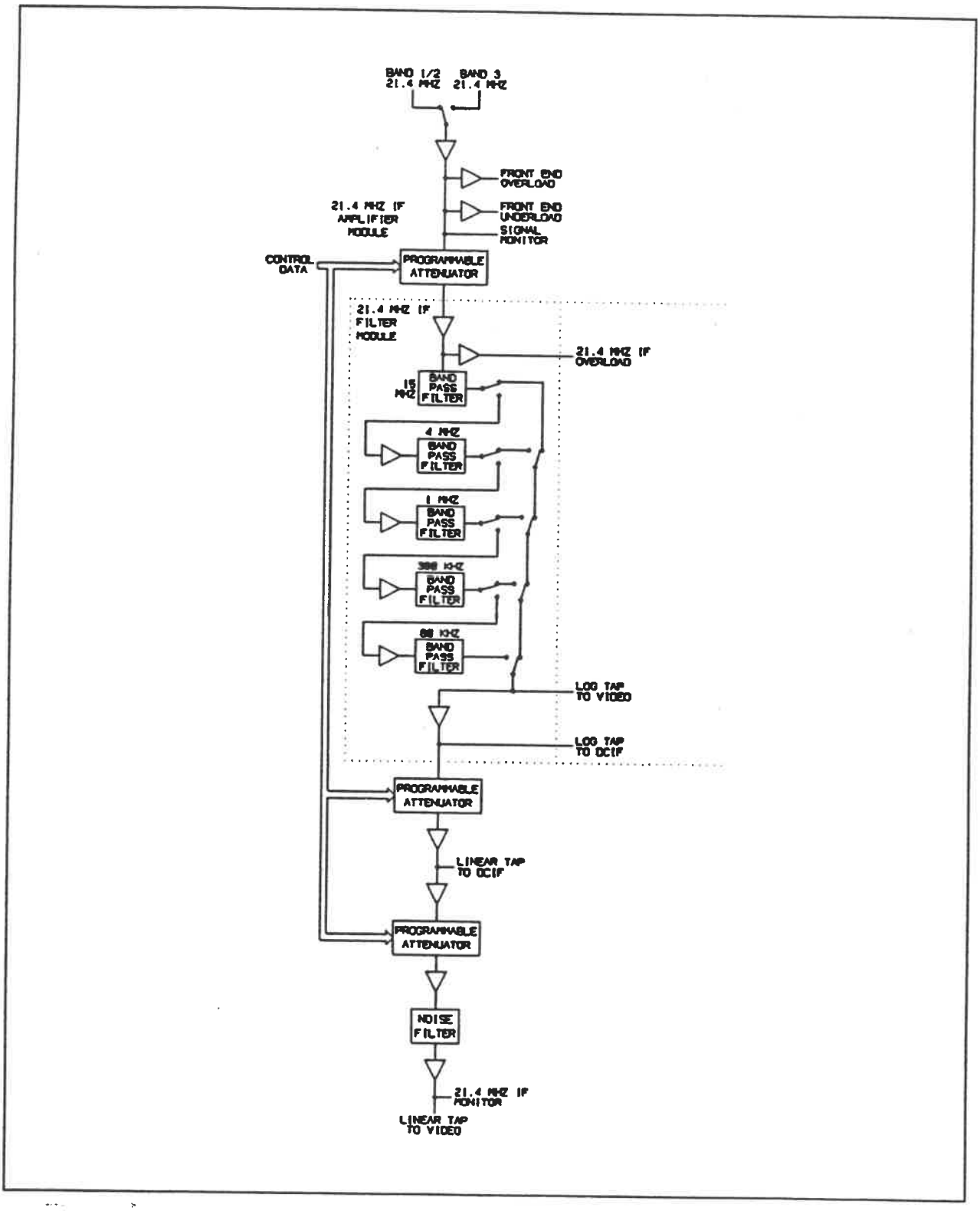


Figure 4-2: R-110 Receiver Simplified Block Diagram - Part 2

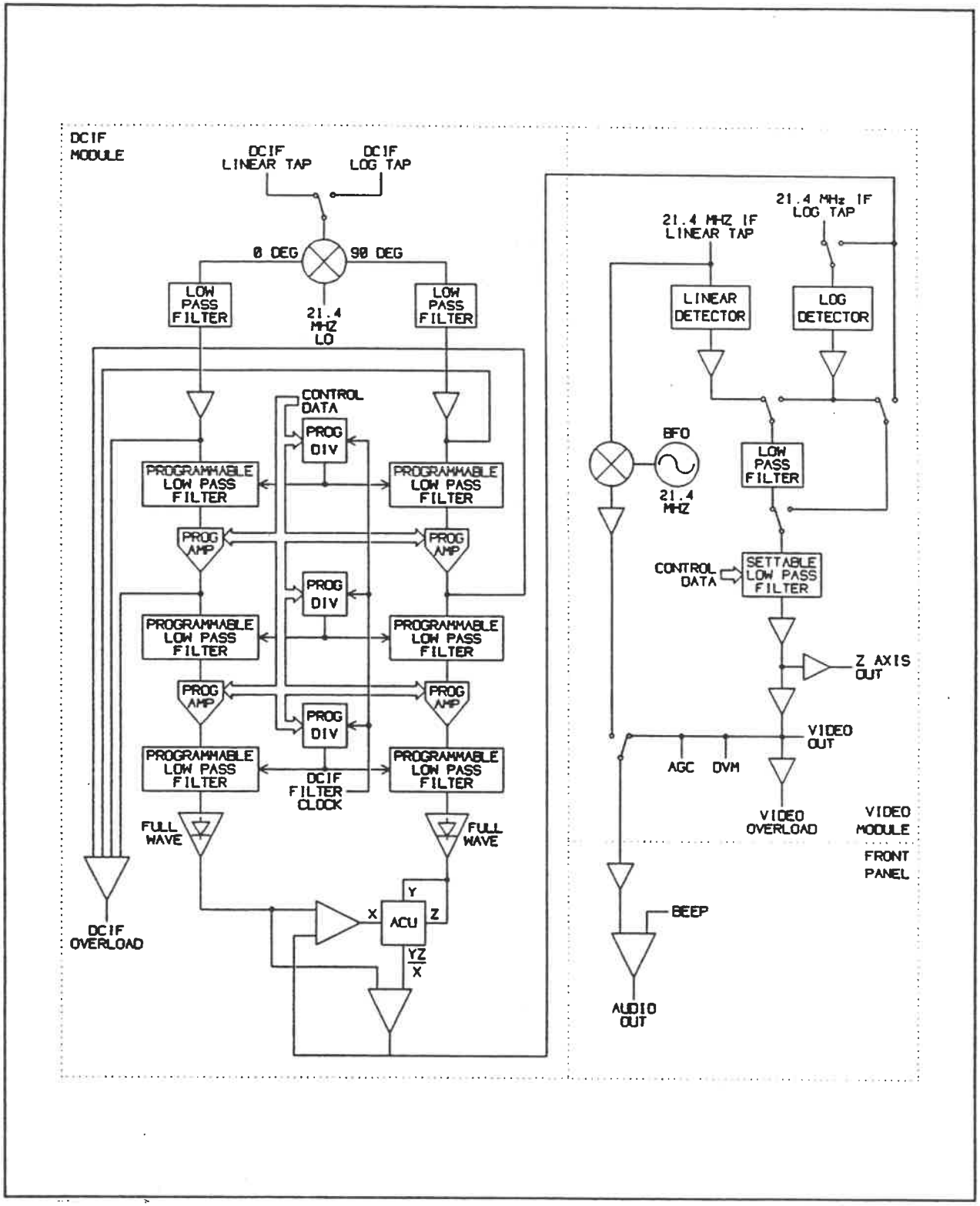


Figure 4-3: R-110 Receiver Simplified Block Diagram - Part 3

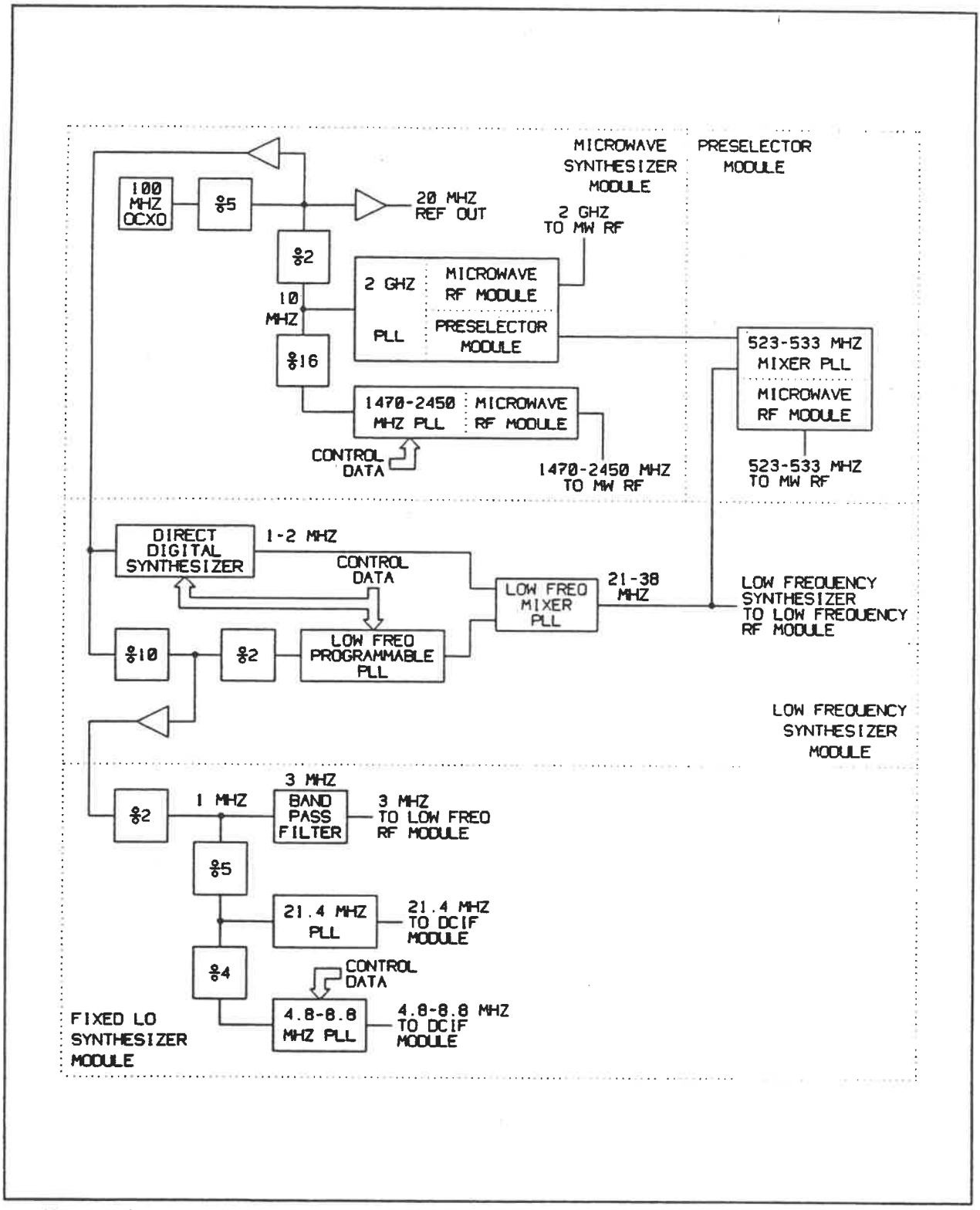


Figure 4-4: R-110 Receiver Simplified Block Diagram - Part 4

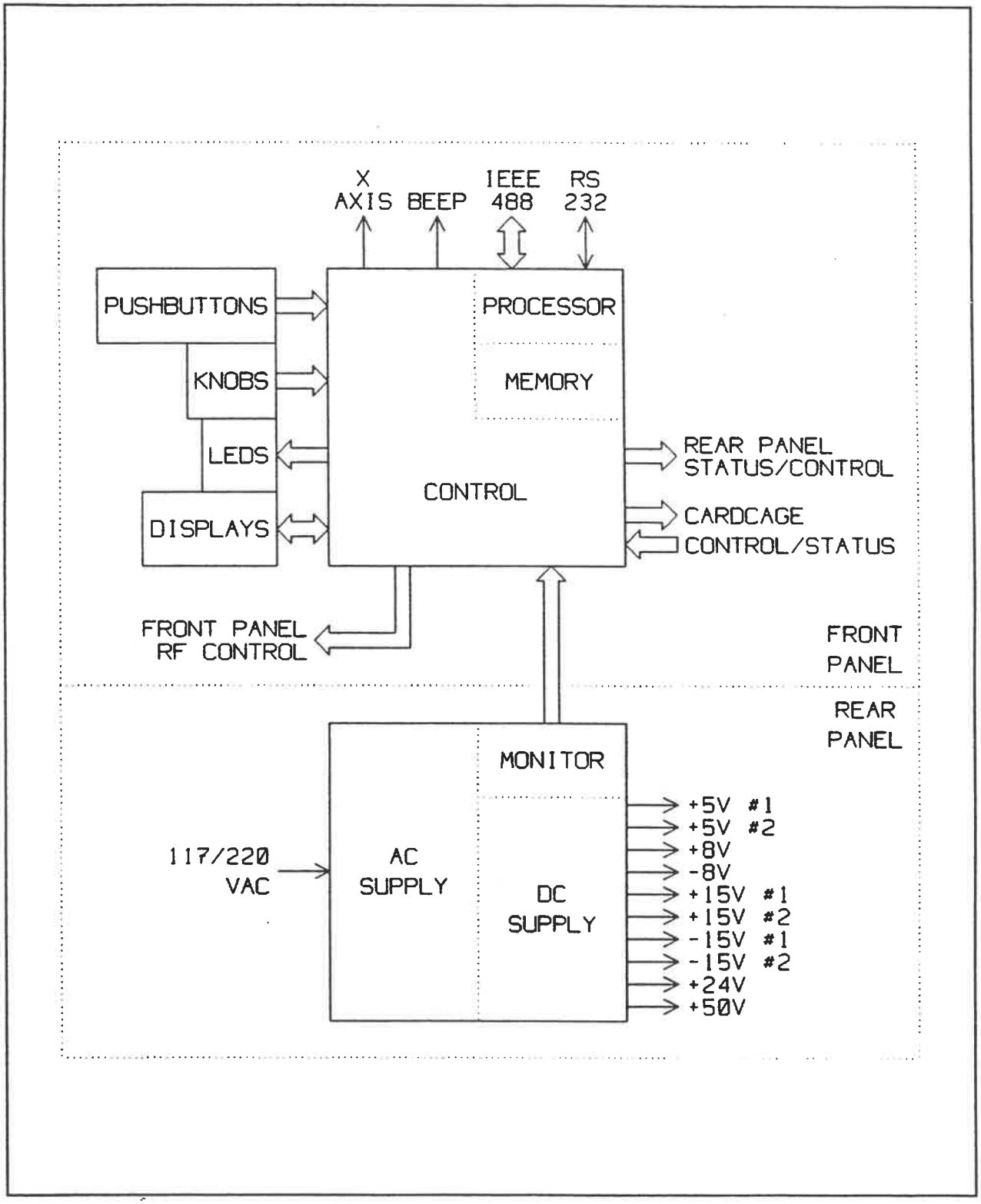


Figure 4-5: R-110 Receiver Simplified Block Diagram - Part 5

4.2 RF Section

The RF section is made up of the RF front-end components (contained in the front panel assembly), the preselector module, the microwave (MW) RF module, and the low frequency (LF) RF module.

4.2.1 Front Panel RF Components

There are two RF signal inputs to the receiver: RF input #1 and RF input #2. The two inputs are furnished with BNC connectors, which are in turn connected to a latching RF relay, which selects between them. The relay is actuated by a pulse command from the control section. The output of the relay is connected to a programmable attenuator, which ranges from 0 - 70 dB in 10 dB steps. The attenuator's controls are non-latching and are driven continuously from the control section. The attenuator's output is routed to the appropriate conversion stage by another RF relay relay which is set by the control section according to the selected tuning band. When tuning in bands 1 and 2, the signal is directed to the low frequency RF module (A1A5), while when tuning in band 3 the signal is directed to the input filter in the preselector module (A1A2). Space has been reserved for a "ground loop isolator", a device which serves to connect or disconnect input signal returns to/from chassis ground. It is currently not used in the radio, but will be necessary in the future if the tuning range of the radio is extended much below 1 kHz. While the signal input returns are currently isolated from the chassis, a hard ground is necessary when tuning low frequencies in order to reduce pickup of 60 Hz line power and its harmonics.

4.2.2 Low Frequency RF Module (A1A5)

When tuning in band 1 and band 2, the signal from the front panel RF section is passed to the low frequency RF module (A1A5) for processing and conversion. Figure 4-6 is a block diagram of the module showing the circuit functions and the LO frequencies utilized. Band 1 signals are converted to the 21.4 MHz intermediate frequency using two mixer stages. The first mixer is an up-converter that generates the sum of the band 1 received frequency and a 3 MHz fixed LO signal. The first mixer stage output is routed to a second converter where it is mixed with the output of the programmable low frequency synthesizer to produce the fixed 21.4 MHz intermediate frequency. This second converter is shared by both band 1 and band 2. Band 2 signals use only the second mixer, requiring only a single up-conversion along with the expected amplification and filtering.

At the signal input of the module (J1) is an RF relay (K1) which distributes the incoming signal from the front panel RF section to the band 1 or band 2 signal path depending on the selected tuning band (see the discussion on hysteresis at the band breaks in paragraph 4.1). The path which is not selected is terminated with 50 Ohms. The band 1 selection from the relay passes through a DC blocking capacitor (C2) and then feeds a 300 kHz lowpass filter (C6 - C11, L7, L8) which removes out-of-band signals, LO re-radiation, and image frequencies. The signal then passes through a limiter (CR3, CR4) for protection against transient spikes. The limited signal from the output of the lowpass filter drives a double-balanced mixer (U2). The other input of the mixer is fed by a 3 MHz fixed frequency LO, which arrives at -3 dBm from the synthesizer section via a coax connector (J2), and is stepped up to +7 dBm by an amplifier (U4). Since the mixer is used for up-conversion, the mixer RF and IF connections are reversed from the usual practice in order to allow the low frequency portions of the band 1 tuning range to pass through.

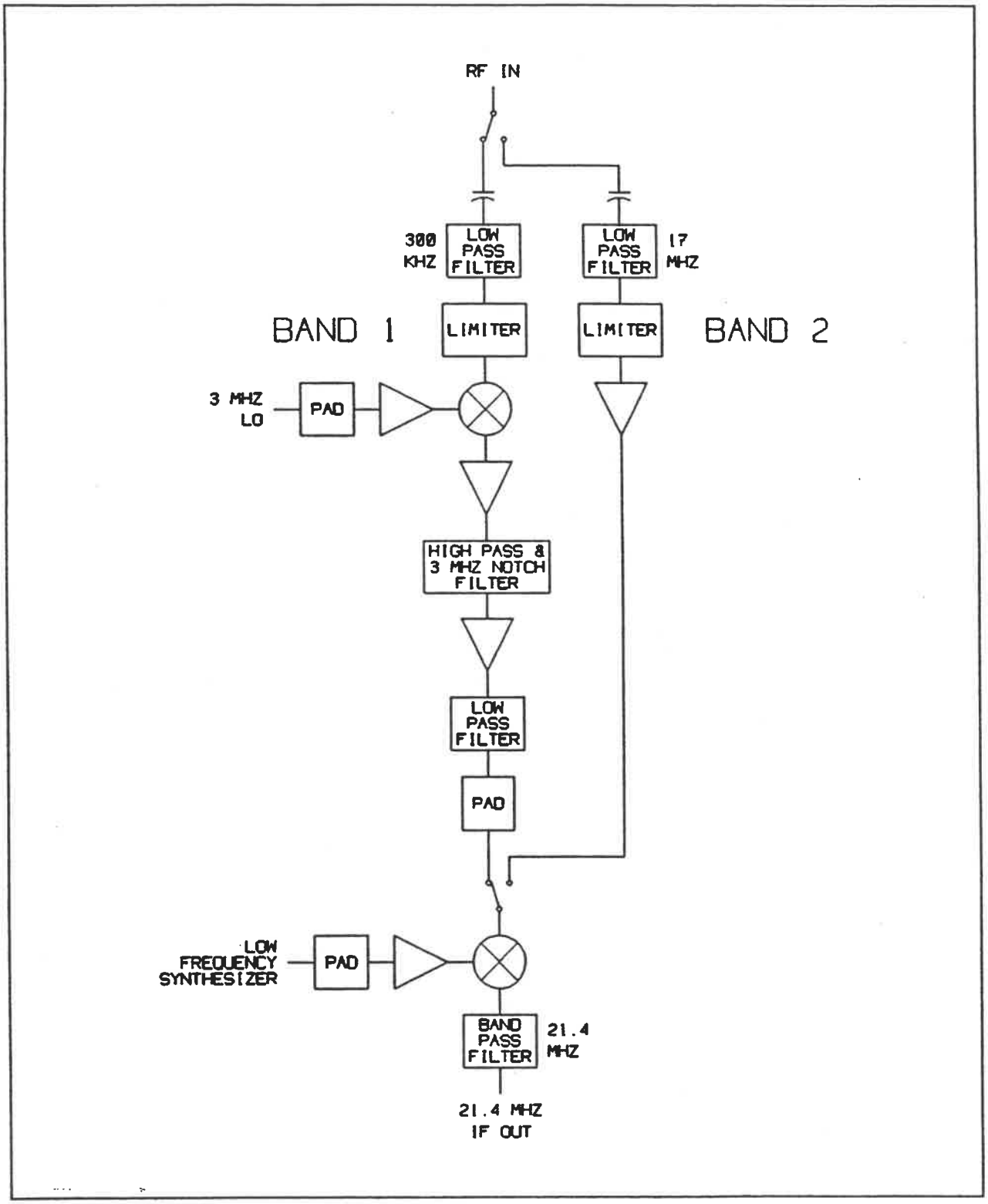


Figure 4-6: Low Frequency RF Module Block Diagram

The output of the mixer feeds a grounded-gate FET amplifer (Q2) which features 6 dB of gain and a low noise figure. The output of this amplifier is transformer-coupled (T1) to a bipolar amplifier (U3) which in turn drives a 3 MHz crystal notch filter circuit which is used to suppress the local oscillator frequency component coming from the mixer. The amplifier's 80 Ohm output impedance is transformed to 3 kOhms at the crystal and back to 35 Ohms at the input to the following amplifier (U6). The higher impedance at the crystal permits a deeper notch at the 3 MHz LO frequency. The amplifier following the crystal drives a lowpass filter (C54 - C59, L21, L22) which passes 3.001 MHz to 3.25 MHz, but attenuates higher frequency components from the mixer. The output signal at this point is not IF yet; it is merely the band 1 input range, up-converted.

The signal then goes through a 10 dB pad (R18 - R20) to a GaAs FET switch (U9) which performs selection between the band 1 and band 2 processing channels. The two signal paths are merged at this point. The GaAs FET switch feeds one input of another double-balanced mixer (U8). The second input of this mixer is driven by a tuneable local oscillator signal which arrives on the module at +2 dBm via a coax connector (J3), and is then stepped up to +7 dBm by an amplifier (U7). In band 1 this LO, provided by the low frequency synthesizer, can range from 24.401 to 24.65 MHz. The output of the mixer feeds a 21.4 MHz bandpass filter (C65 - C69, L24 - L26) which suppresses everything but the difference signal, thus producing a 21.4 MHz IF signal. This signal exits the module via a coax connector (J4). From there the signal goes to the 21.4 MHz IF amplifier module.

Band 2 receives its 250 kHz - 15 MHz signals from the same relay as band 1 (K1), and passes the signal through a DC-blocking capacitor (C4) and 17 MHz lowpass filter (C15 - C22, C25 - C28, C31, C32, L1 - L6) which attenuates out of band signals , LO re-radiation, and image frequencies. The signal then passes through a limiter (CR5, CR6) for protection against transient spikes. The limited output from the lowpass filter then feeds another input of the same GaAs FET switch (U9) that selects the band 1 signal. From this point on the circuitry is shared, the only difference being that in band 2 the tuneable LO can range from 21.65 MHz to 36.4 MHz to provide the fixed 21.4 MHz IF.

Remaining circuitry on the module consists of a transistor switch (Q1) to drive the relay (K1), and a logic-level converter (U1) to drive the GaAs FET switch (U9). Both of these circuits are driven by the same logic signal, sourced at the 21.4 MHz IF amplifier module (A1A6) and carried on a trace across the cardcage backplane.

4.2.3 Microwave RF Module (A1A1)

When tuning in band 3, the signal from the front panel RF section is passed to the preselector module (A1A2), where it is passed through a lumped-element, 1100 MHz low-pass filter (A1A2 FL1). The filtered signal is then passed to the microwave RF module. (This one filter is why A1A2 is called the "preselector module". All of the other circuitry in the module is part of the synthesizer section.) The rest of the circuitry for band 3 processing is contained in the microwave RF module. Figure 4-7 is a block diagram of the processing.

The circuitry begins with the input limiter subassembly (A1A1A1). This consists of a set of diodes (A1A1A1 CR1 - CR4) and a tuned length of 50 Ohm line (A1A1A1 W1). In normal operation the tuned line is inductive, forming a low-pass filter with the capacitance of the diodes. The corner of this filter is at about 1200 MHz. When the input signal exceeds about 300 mV, either positive or negative, the diodes begin to conduct, thus limiting the output from the subassembly by shunting the excess to ground. The capacitance of the diodes changes as they begin to conduct, so that the filter properties of the circuit are corrupted when in limit. Trimming capacitors (A1A1A1 C3, C4) are provided to optimize the VSWR.

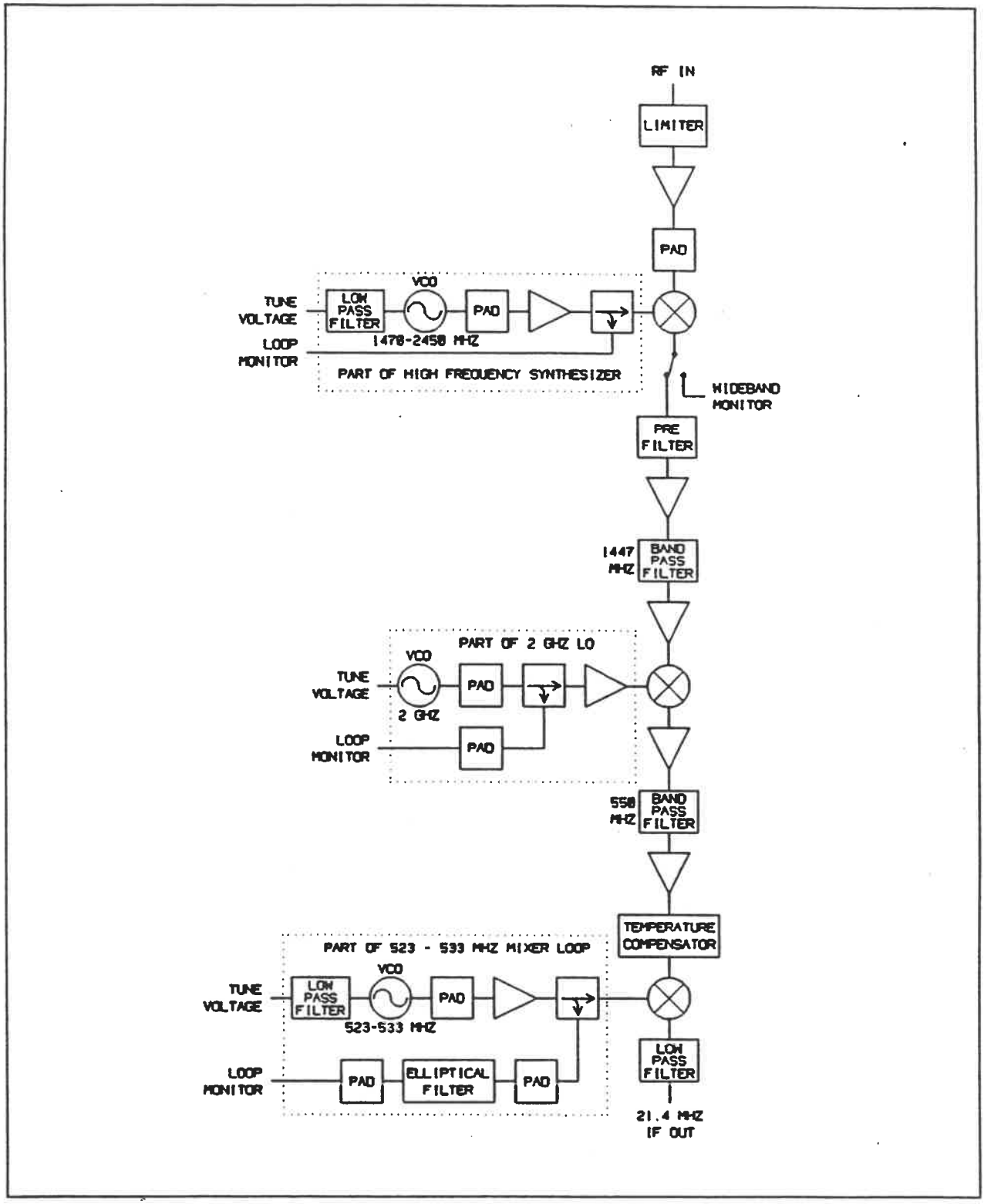


Figure 4-7: Microwave RF Module Block Diagram

The output of the limiter subassembly feeds the first conversion subassembly (A1A1A2). This begins with the RF amplifier (A1A1A2 U1), which provides 14.5 dB of gain and is the major contributor to the noise figure of the radio. The amplifier is followed by a 1 dB pad (A1A1A2 R1 - R3) which is provided to clean up the VSWR of the input of the amplifier, because this component partially reflects its output conditions at its input. The padded signal feeds the first conversion mixer (A1A1A2 U2), the other input of which is the 1470 - 2450 MHz programmable synthesizer output, arriving at approximately +9 dBm. See paragraph 4.6.2 for a description of this LO.

The mixer converts the input to about 1450 MHz. The output of the mixer feeds a GaAs FET switch (A1A1A2 K1) which diverts the signal to wideband output connector (J4) on top of the module when external wideband mode is enabled. The switch requires logic levels of 0 and -8 Volts, in complementary phases, delivered by a translator (U1) from a select signal supplied across the cardcage backplane (A1A20) from the 21.4 MHz IF amplifier module (A1A6).

If not diverted to the wideband monitor jack, the signal is passed to the prefilter/amplifier subassembly (A1A1A3). Here it feeds a 1450 MHz bandpass filter consisting of a pair of adjustable capacitors (A1A1A3 C1, C3) and a length of 50 Ohm line tuned to act as an inductor (A1A1A3 W1), all connected in series. This attenuates the undesired mixing components, and also pads the desired signal by about 1 dB. The filter is followed by an amplifier (A1A1A3 U1) which provides about 9 dB of gain. All of this between the input amplifier and the first conversion amplifier introduce losses of about 10 dB. So while the input amplifier adds 14.5 dB of margin, most of it is used up in the first conversion and filtering, and so components later in the signal path can still have a small effect on the noise figure.

The first conversion amplifier output feeds the second conversion subassembly (A1A1A4). Here it passes through a helical filter (A1A1A4 FL1) which features a center frequency of 1447.5 MHz and a 3 dB bandwidth of 24 MHz. This rejects everything but the desired IF. The filter is followed by an amplifier (A1A1A4 U1) which provides about 9 dB of gain. The amplifier drives the second conversion mixer (A1A1A4 U2), the other input of which is the 2 GHz fixed LO at approximately +9 dBm. See paragraph 4.6.2 for a description of this LO. The result of the conversion is the second IF, ranging around 550 MHz. The output of the mixer feeds the second conversion amplifier (A1A1A4 U3) which provided 12 dB of gain.

The second conversion amplifier output feeds a 550 MHz, lumped-element bandpass filter (A1A1A5 FL1) which rejects everything but the 550 MHz IF. The output of the filter feeds the third conversion subassembly (A1A1A6), beginning with an amplifier (A1A1A6 U5) which provides 12 dB of gain. Following the amplifier is the temperature compensator. Two current sources are connected in series, one temperature-varying (A1A1A6 U8), the other stable (A1A1A6 Q2). At room temperature they pass exactly the same current (about 100 uA), with a trimmer (A1A1A6 R15) provided to balance them. The difference between them therefore varies with temperature. This difference is amplified (A1A1A6 U7) and converted to a voltage. This voltage is then used to control a current source (A1A1A6 Q4) with temperature compensation (A1A1A6 CR5). The current source drives a variable attenuator circuit consisting of PIN diodes (A1A1A6 CR1, CR2) and a tuned length of 50 Ohm line (A1A1A6 W1). The diodes form the legs of a pi-network, and the tuned line forms the bridge. Varying the current source with temperature causes the impedance of the diodes to change, which causes the padding effect of the pi-network to change. The range of adjustment is about 6 dB, with 3 dB applied at room temperature. A trimmer (A1A1A6 R29) is provided to adjust the gain factor of the current source. The temperature compensating circuit uses -8 VDC from the cardcage backplane and +9 VDC developed locally from +15 VDC by means of a regulator (A1A1A6 U6). An enabling switch for the -8 VDC to the circuit (A1A1A6 Q1, Q3) is used to remove the -8 VDC supply from the temperature control circuit should the +15 Volt supply fail.

Once the signal has passed through the temperature compensator it feeds the third conversion mixer (A1A1A6 U4), the other input of which is the 523.6 - 533.6 MHz LO at approximately +9 dBm. See paragraph 4.6.3 for a description of this LO. The result of this conversion is the 21.4 MHz IF, now tuned to the exact center frequency desired. The output of the mixer passes through a 39 MHz low-pass filter (A1A1A6 L5, C18, C19) and is then delivered to the 21.4 MHz IF amplifier module (A1A6).

4.3 21.4 MHz IF Section

The 21.4 MHz IF section consists of two modules: the 21.4 MHz IF amplifier module (A1A6) and the 21.4 MHz IF filter module (A1A8). Signals pass from the outputs of the microwave RF module (A1A1) and the low frequency RF module (A1A5) to the signal inputs of the 21.4 MHz IF amplifier module. After initial selection switching, fixed and variable gain, and overload detection, the signal passes to the 21.4 MHz IF filter module. There the signal passes through one or more bandpass filters, also with switch selection, and more overload detection. The output goes to three destinations: to the video module (A1A9) log detector; to the DCIF module (A1A11) for for narrower bandwidths in log mode; and back to the 21.4 MHz IF amplifier module for further fixed and variable gain, for use with linear mode video. The outputs from this part of the 21.4 MHz IF amplifier module drive the DCIF module, the linear detector in the video module, and the 21.4 MHz IF monitor jack on the rear panel of the receiver.

Note that since the linear mode DCIF pickoff is placed before the end-to-end gain setting circuit, this function must also be supplied in the DCIF. Also, since the log mode pickoffs for both DCIF and wider-bandwidth modes are placed before the last gain-setting circuit, the controllable gain range in log mode is only 2/3 of what it is in linear mode, 33.3 dB vs. 50 dB.

The two 21.4 MHz IF modules will be discussed separately in the following paragraphs. A block diagram of the 21.4 MHz IF section is shown in figure 4-8.

4.3.1 21.4 MHz IF Amplifier Module (A1A6)

The signal path begins with a GaAs FET switch (U10) which selects the module signal input from the outputs of either the microwave RF module (A1A1) or the low frequency RF module (A1A5). The output of the switch is transformer-coupled (T2) to an amplifier (U11) to provide impedance matching. Both signals arrive at 21.4 MHz center frequency and with unwanted mixing products removed. The output of the first amplifier goes in three directions: to the front end overload/underload detector circuit, and then through a splitter (U8) out of the module to the signal monitor jack on the rear panel of the radio; and also to the first of the variable attenuator circuits.

The detector circuit provides a transistor (Q1) amplifier to bring up the signal level without worrying too much about cleanness, followed by a diode detector (CR18), followed by comparators for overload (U20) and underload (U21). The detector output is biased DC positive, and increasing signal levels cause the output to be pulled more negative. For the overload detector a positive threshold is set by a trimmer (R64), lower than the DC bias of the detector output. When the incoming signal level pulls the detector output below the threshold comparison level set by the trimmer, an overload is detected. The trimmer is set so that this happens at -19 dBm signal level entering the module. Similarly, the underload detector has a second positive threshold set by a trimmer (R69). The underload comparator is connected oppositely, so that when the incoming signal level *doesn't* pull the output of the detector below the comparison value set by the trimmer, an underload is detected. The threshold here is set at -32 dBm at the module inputs. Overload and underload status is passed to the cardcage backplane interface circuit for further processing.

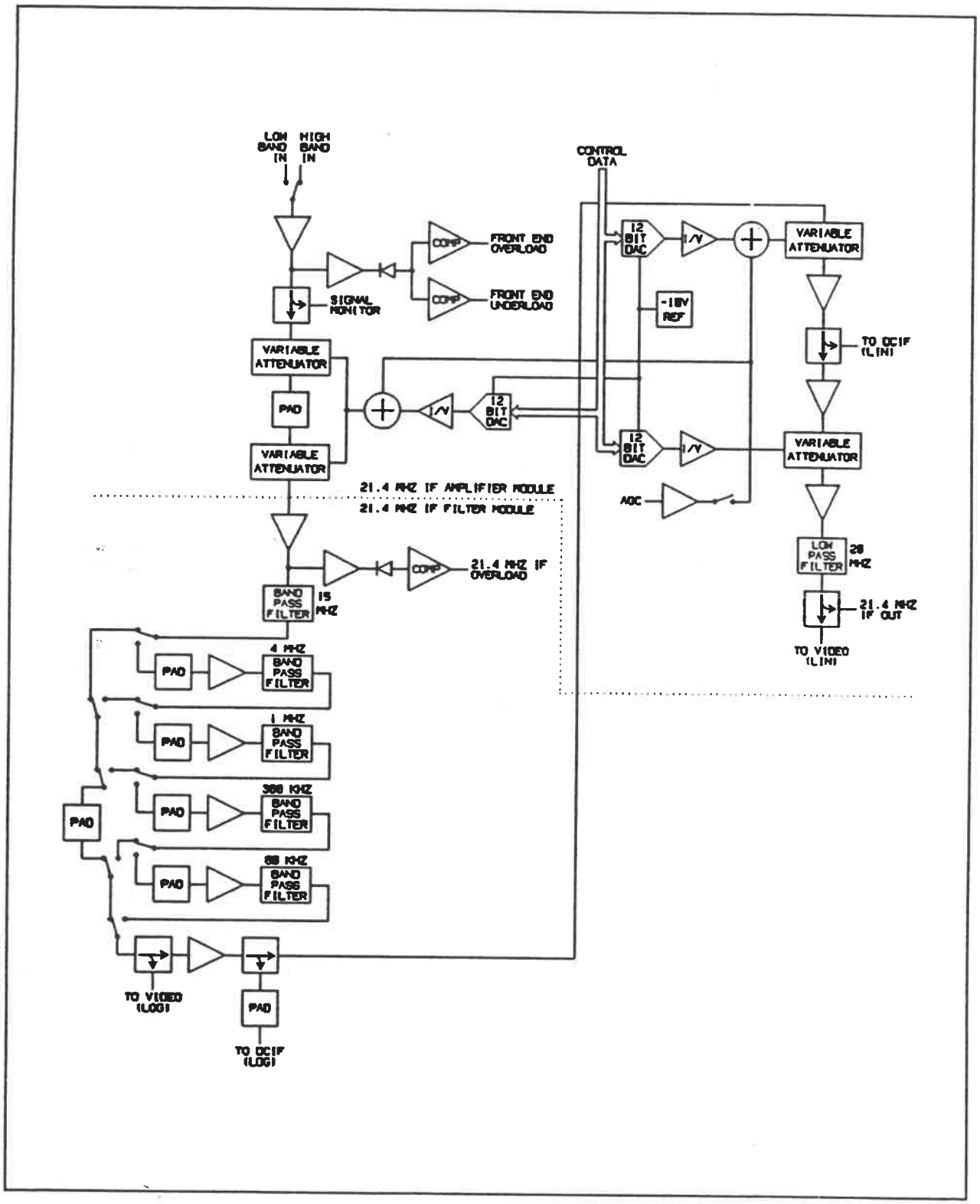


Figure 4-8: 21.4 MHz IF Section Block Diagram

There are four variable attenuator circuits in the module, all identical in implementation but different in how they are controlled. Each has a controllable range of approximately 20 dB. The first two are placed in tandem after the signal monitor output pickoff, with a pad (R35 - R37) between them.

Each attenuator circuit is based on a pair of PIN diodes (CR13, CR14 in the first circuit). These components can vary their impedance of a high-frequency signal based on their DC bias. The signal level must be small for the effect to be linear. The circuitry surrounding the PIN diodes is provided to AC-couple the signal through the diodes, to supply the DC bias and its variation to the proper points, and to block the signal from entering the bias circuits. One diode (CR14 in the first circuit) acts as a coupling diode, for which increased bias will increase signal coupling. The other diode (CR13 in the first circuit) acts as a signal shunt to ground, so increased bias here will decrease the signal level at the output.

Attenuator bias is partly fixed and partly variable. The variable part is controlled partly by AGC (when enabled) and partly by the microprocessor controlling the radio, via DACs. AGC is developed in the video module (A1A9) and is delivered to the 21.4 MHz IF amplifier module as a slowly varying DC level. Entering the module it is amplified (U28) with offset adjusted via a trimmer (R100). This trimmer sets the AGC turn-on point. The output of the amplifier is clamped (CR28) and rectified (CR29) to positive values. A relay (K1) controlled by the cardcage backplane interface circuit acts as an AGC on/off function by connecting/disconnecting the AGC signal to the attenuator circuits. Another trimmer (R101) is provided after the relay to set the off-state contribution.

The first two attenuator circuits are driven by the AGC signal (when selected) and also by the output of one of the control DACs, called DAC A (one of the two separate outputs of U17, converted to voltage output by U12). The DAC output is 0 to +10 VDC. It is reduced via a resistive divider (R87, R88) and then precision rectified (U27, CR25), and then combined with the AGC signal and amplified (U27 again). This output is delivered to the attenuators. The effective voltage range for the attenuator circuits is about +2 to +10 Volts.

The output from the two tandem attenuator circuits is passed to the 21.4 MHz IF filter module where the signal is reduced to 15 MHz bandwidth or less. Returning from the 21.4 MHz IF filter module, the signal passes through the third attenuator circuit. This circuit is controlled by both the AGC voltage used to control the first two attenuator circuits, and also by the output of a second DAC, called DAC B (the other output of U17, converted to voltage output by another section of U12). The DAC output is reduced by a resistor pair (R79, R80), precision rectified (U26, CR23), and combined with the AGC signal and amplified (U26 again) to drive the attenuator circuit.

The output of the third attenuator circuit is amplified (U6), and the linear mode input for the DCIF module is picked off via a splitter (U7). The signal path then continues with another amplifier (U5), followed by the fourth attenuator circuit. This attenuator is provided for end-to-end (predetection) gain setting and is controlled by a DAC only, without contribution from the AGC. The DAC, called DAC C (one of the outputs of U16, converted to voltage output by a section of U12) drives the attenuator circuit directly. The output of the attenuator circuit is transformer-coupled (T1) to an amplifier (U3), through a noise filter (L2, L3, C5, C6, C9) to another amplifier (U2), and is finally sent to the linear detector on the video module, and to the 21.4 MHz IF output jack on the rear panel of the receiver, via a splitter (U1). The noise filter is a low-pass with its cutoff set at 30 MHz. This reduces out-of-band noise contributions from the circuitry located behind the bandpass filters.

A temperature compensation circuit is provided (based on U29 - U31, Q3, Q4, CR30 - CR32), but it is currently unused. If a wider operating temperature range is specified, then it may be placed in service.

The cardcage backplane interface circuit consists of buffering and latching for bus data bits, address decoding, level shifting, and DAC control. A status return circuit for overload and underload are also provided. A precision -10 VDC reference for the DACs (U4) is also provided.

Incoming data is buffered (U15) and passed to a latch (U14). Three of the latch bits are used directly, to enable band selection and AGC. Four more bits are decoded (U13) to form the bandwidth selects. Bus addresses are decoded (U18, U19) to control the data latch and the two DAC ICs (U16, U17). They feature two 12 bit DACs per package, mapped onto the 8 bit data bus. Here is the addressing for the module:

Address 50(hex) - 53(hex) = DAC IC #1 (U17):
- Address 50(hex) = DAC A LSDs:
  - Bits 0 - 7 = DAC A bits 0 - 7
- Address 51(hex) = DAC A MSD:
  - Bits 0 - 3 = DAC A bits 8 - 11
  - Bits 4 - 7 = (unused)
- Address 52(hex) = DAC B LSDs:
  - Bits 0 - 7 = DAC B bits 0 - 7
- Address 53(hex) = DAC B MSD:
  - Bits 0 - 3 = DAC B bits 8 - 11
  - Bits 4 - 7 = (unused)

Address 54(hex) - 57(hex) = DAC IC #2 (U16):
- Address 54(hex) = DAC C LSDs:
  - Bits 0 - 7 = DAC C bits 0 - 7
- Address 55(hex) = DAC C MSD:
  - Bits 0 - 3 = DAC C bits 8 - 11
  - Bits 4 - 7 = (unused)
- Address 56(hex) = DAC D LSDs:
  - Bits 0 - 7 = DAC D bits 0 - 7
- Address 57(hex) = DAC D MSD:
  - Bits 0 - 3 = DAC D bits 8 - 11
  - Bits 4 - 7 = (unused)

Note: DAC D is currently unused.

Address 58(hex) = load all DACs strobe (data unimportant)

Address 59(hex) = data latch:
- Bits 0 - 2 = bandwidth code:
  - 000 = 15 MHz*
  - 001 = (reserved for 8 MHz*)
  - 010 = 4 MHz*
  - 011 = 1 MHz*
  - 100 = 300 kHz*
  - 101 = 80 kHz*
  - 110 = (unused)
  - 111 = wideband*
- Bit 3 = bandwidth enable:
  - 0 = disable
  - 1 = enable
- Bit 4 = high/low band select:
  - 0 = high band (band 3)
  - 1 = low band (band 1/2)
- Bit 5 = band 1/band 2 select:
  - 0 = band 2
  - 1 = band 1
- Bit 6 = AGC enable:
  - 0 = disable
  - 1 = enable
- Bit 7 = (unused)

The bandwidth select lines are routed through the cardcage backplane to the 21.4 MHz IF filter module. The band 1/band 2, high/low band, and wideband select lines are also routed onto the cardcage backplane, for use by the microwave RF module and the low frequency RF module. The high/low band select line also drives a level shifter (U9) which provides the 0 and -8 Volt logic levels required by the GaAs FET switch on the module input.

The status return circuit takes its inputs from the front end overload and underload detection comparators. The underload input drives a retriggerable monostable multivibrator (U25) and recombination gate (U24) which ensures that underload must be present for at least 200 uS before underload status is placed on the bus. The backplane trace (B20) is driven through a tristate driver (U22). Meanwhile, the overload input is stretched and filtered (U22, CR22, C93), and drives both the backplane combined front end overload (B21) and the discrete 21.4 MHz IF front end overload (A17) traces through tristate drivers (U22). Currently the combined front end overload line is only driven by this circuit.

4.3.2 21.4 MHz IF Filter Module (A1A8)

This module takes its input from the 21.4 MHz IF amplifier module (A1A6) and provides outputs to the video module (A1A9) log input, the DCIF module (A1A11), and back to the 21.4 MHz IF amplifier module. Bandwidth selection control is taken from the cardcage backplane, supplied by the IF amplifier module, and back end overload detection outputs are placed the cardcage backplane as well.

The signal path begins by transformer-coupling (T1) the signal from the IF amplifier module to an amplifier (U1) which adds 14 dB of gain. The amplifier output is sampled by the back end overload detection circuit and is transformer-coupled (T2) to drive the 15 MHz bandpass filter. The overload detector consists of a transistor amplifier (Q1) followed by a diode detector (CR2) and storage capacitors (C12, C13). the detector output is sampled by a comparator, using a positive DC reference set by a trimmer (R1) as a threshold. The signal pulls a positive DC bias in the detector output downward, so that a signal in excess of -34 dBm at the module input pulls will pull the detector output below the comparator threshold, triggering an overload status condition. The comparator output is stretched and filtered (U3, CR3, C23) so that an impulsive overload will provide about a 1 uS status pulse. The filtered output is delivered to the cardcage backplane combined back-end overload line (A20) and the 21.4 MHz IF overload line (B18) via tristate drivers (U3).

The 15 MHz bandpass filter consists of an LC network (L7 - L9, C6, C7, C30 - C32). Its output feeds a GaAs FET switch (U6) which directs the signal either to the input or the output of the 4 MHz bandpass filter.

The 4 MHz filter begins with a 5 dB pad (R33 - R35) followed by an amplifier (U5) which adds 14 dB of gain, for a net gain of 9 dB. The amplifier is followed by an RLC network (L10 - L15, C36, C38, C40, C42, C43, C45, C47, C49, R19 - R21, R23 - R26) which establishes the filter characteristic. The network is followed by a GaAs FET switch (U9) which directs the output of the filter either to the input of the 1 MHz bandpass filter or to another GaAs FET switch (U22) which selects either the outputs of the 4 MHz filter or the 15 MHz filter for output from the overall filter section.

The 1 MHz bandpass filter begins with a 6 dB pad (R42 - R44) followed by an amplifier (U8) providing 14 dB of gain, for a net gain of 8 dB. The amplifier is followed by an LC network (L19 - L23, C54 - C72, C100), followed by a GaAs FET switch (U12) which directs the output of the filter either to the input of the 300 kHz bandpass filter or to another GaAs FET switch (U23) which selects either the output of the 1 MHz filter or the signal selected from the outputs of the 4 MHz and 15 MHz filters for output from the overall filter section.

The 300 kHz bandpass filter begins with a 2 dB pad (R56 - R58) followed by an amplifier (U11) providing 14 dB of gain, for a net gain of 12 dB. The amplifier is followed by an LC network (L26 - L29, C75 - C86, C105), followed by a GaAs FET switch (U15) which directs the output of the filter either to the input of the 80 kHz bandpass filter or to another GaAs FET switch (U24) which selects either the output of the 300 kHz filter or the signal selected from the outputs of the 1 MHz, 4 MHz, and 15 MHz filters, padded by 4 dB (R47, R48, R59), for output from the overall filter section.

The 80 kHz bandpass filter begins with a 7 dB pad (R67 - R69) followed by an amplifier (U14) providing 14 dB of gain, for a net gain of 7 dB. The amplifier is followed by a crystal filter (FL1), which is followed by a GaAs FET switch (U17) which selects either the output of the 80 kHz filter or the signal selected from the outputs of the 300 kHz, 1 MHz, 4 MHz, and 15 MHz filters, for output from the overall filter section.

The idea is that the radio will normally be used for receiving signals which are mostly impulsive, which means that signal level is directly proportional to bandwidth. Noise in band, however, is proportional to the square root of the bandwidth. Amplification has therefore been provided in each bandwidth filter which will normalize the noise, that is, the amplification factor is proportional to the square root of the reduction in bandwidth. For example, since the reduction in bandwidth between the 1 MHz filter and the 4 MHz filter is a factor of four, the 1 MHz filter section requires an overall extra gain of the square root of four, or two. In actuality, a 14 dB amplifier and a 6 dB pad are provided, with the odd 2 dB being absorbed by the passive filter components, switches, etc.

The bandwidth filters are Chebyshev type, with a 60 dB bandwidth approximately four times the 6 dB bandwidth. The switching is set up so that for any given bandwidth the signal must pass through the associated bandwidth filter and all wider ones as well, in sequence. In other words, for 300 kHz bandwidth, the signal passes through the 15 MHz filter, followed by the 4 MHz filter, followed by the 1 MHz filter, followed by the 300 kHz filter, with only the 80 kHz filter omitted. By doing this the gain is gradually increased as the bandwidth is gradually reduced, which yields the best dynamic range.

The output from the final selection switch drives a splitter (U18). One output of the splitter is routed to the log input on the video module through a pad (R78 - R80) for use in non-DCIF log mode. The other splitter output is transformer-coupled (T3) to an amplifier (U20) which provides 14 dB of gain. The amplifier drives another splitter (U19), one output of which is returned to the IF amplifier module at +10 dBm full scale. The other splitter output is routed to the log mode input of the DCIF module through an 8 dB pad (R81 - R84) at +2 dBm full scale.

The remaining cardcage backplane interface consists of level translators for the filter select lines provided by the 21.4 MHz IF amplifier module. The GaAs FET switches require logic levels of 0 and -8 Volts in complementary phases, which are provided by comparators acting as level shifters from the incoming TTL (U4, U7, U10, U13, U16). Incoming select signals are valid when low. Switching is set up so that a given filter output is routed to the module outputs when selected, or to the input of the next narrower filter stage when not selected. The 15 MHz filter is always in the signal path, one way or another.

4.4 DCIF Module (A1A11)

The DCIF module (A1A11) begins with a signal taken from the 21.4 MHz IF, provides programmable bandwidths from 200 Hz to 20 kHz, provides programmable back-end gain, and provides AM detection for its available bandwidths, producing an output which is sent to the video module. Note that the DCIF is only in use when one of its bandwidths is selected, and is completely bypassed and shut down otherwise.

The module consists of the following circuits:

- input section, consisting of an LO amplifier, quadrature splitter, and carrier elimination (envelope) filters
- gain recovery amplifiers for each phase
- programmable switched-capacitor filters for each phase
- multiplying DACs for each phase
- precision rectifiers for each phase
- a square-root-of-the-sum-of-the-squares circuit
- a programmable timebase with multiple outputs
- an overload detection circuit
- a logic and control circuit

These circuits perform the following receiver functions:

- narrow bandwidth filtering from 200 Hz to 20 kHz
- programmable gain in the back end, for proper gain distribution
- AM detection for narrow bandwidths
- back end overload status for narrow bandwidths

Discussion will proceed from signal input to signal output, with additional descriptions of peripheral circuits provided where appropriate. The block diagram of the section is shown in figure 4-9.

The signal path begins with the input section, which produces two output channels in quadrature. Each channel contains three programmable filters and two programmable amplifiers. Following all of that the channels must be recombined to form the output. The idea behind the DCIF lies in the fact that a signal may be split into two components which always differ in phase by 90 degrees, each phase may be identically processed, and the results recombined in a vector sum, without losing information. In the case of the DCIF, "processing" consists of converting to baseband, bandlimiting, and gain setting. By doing it this way the usual bulky, heavy crystal filters required for each desired bandwidth are eliminated. The drawback is that both phases must be processed *identically*. Identical in gain, in phase, in frequency response, and in DC offset. Any mismatch will produce distortion in the output, normally in the form of "motorboating", in which the beat frequency between the tuned signal from the 21.4 MHz IF and the 21.4 MHz LO, produced by the mixer/splitter, is imperfectly cancelled when the two channels are recombined. In order to minimize this problem a number of corrective factors and adjustments have been provided in the DCIF. These will be detailed as part of the following descriptions as well.

The input section is based on a quadrature mixer/splitter (U11) which mixes the input from the 21.4 MHz IF section with a fixed 21.4 MHz IF LO signal from the synthesizer section, thus converting the signal to baseband. The LO arrives on the module at -10 dBm and is amplified by an op-amp (U10) to +16 dBm. Through the source resistor, it drives the mixer/splitter at +10 dBm. The LO is transferred at a low level in order to minimize pickup by other modules. The signal input may be taken from either of two points in the 21.4 MHz IF, depending upon whether or not log compression is selected in the video section. Different inputs are required for the gain distribution to come out right. Input selection is performed by a relay (K1), set by the logic and control circuit. Of the four programmable gain stages in the 21.4 MHz IF, the tap for the DCIF in linear mode precedes the last one (which is responsible for setting end-to-end gain for the radio) and the tap for the DCIF in log mode precedes the last two, which cuts into the IF gain control range. In each case the correction must be made up in the DCIF's programmable gain stages. In practice, the linear tap sees up to 18 dB more gain from the 21.4 MHz IF than the log tap, but a full-scale signal at each input is -6 dBm. The selected signal drives the mixer/splitter directly.

The mixer/splitter has two outputs which differ in phase by 90 degrees, one called "in-phase" and the other "quadrature" (I and Q). Each output passes through a two-pole low-pass L-C filter to remove everything but the difference component from the signal. The bandwidth of the signal from the 21.4 MHz IF is always limited to 80 kHz, and the widest bandwidth expected from the DCIF is only 20 kHz, so a two-pole filter with its corner at 700 kHz is sufficient to get rid everything but the baseband signal. Components are selected during module test for the best match between channels. A trimmer (C33) is provided to adjust the mixer/splitter to exactly 90 degrees of phase shift between the outputs.

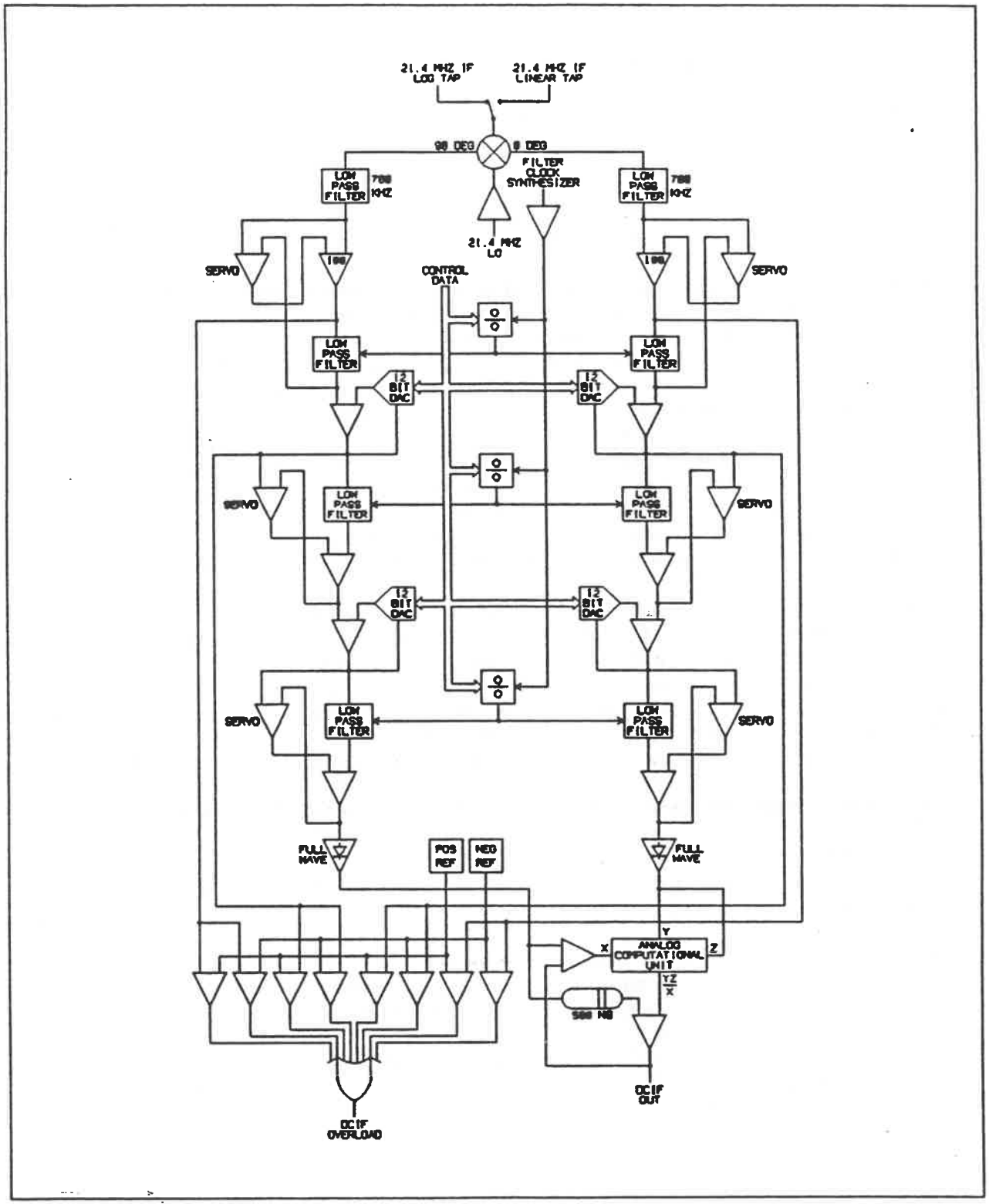


Figure 4-9: DCIF Block Diagram

After the filters, the outputs from the mixer/splitter are at at 50 mV peak, full-scale, so each output is provided with a 40 dB fixed-gain low-noise amplifier (U14 and U13). Full-scale outputs from these amplifiers are 5 Volts peak, and are clamped to +/- 7 Volts by diodes (CR3 - CR8), to prevent both turn-on transients and disabled-state servo drift from damaging the circuits which follow, which use smaller power supply voltages. The amplifiers also provide a pole of high-end rolloff with the corner at about 25 kHz, for noise filtering. The rolloff capacitors (C36, C42) and the timing capacitors in the servo amps (C28, C29) are matched in pairs before production. The servo gain-setting resistors (R34, R35, R39, R40) are selected during module test for the best match between channels. Servo gain must be set to match the gain of the signal amplifiers as well.

The gain-recovery amplifiers are followed by the first bandwidth filters. Each amplifier/filter combination is provided with a chopper-stabilized servo amplifier (U12) to eliminate any long-term DC components, since any offset will easily saturate the module output at narrow bandwidths (where bandwidth-compensating gain is highest). The overall structure at this point, in each channel, consists of a programmable filter, followed by a programmable gain unit, followed by another programmable filter, followed by another programmable gain unit, followed by another programmable filter. Although a single filter provides adequately sharp cutoff at the edge of the passband, a second filter is necessary in front to prevent aliasing around the filter clock, and a third filter is necessary in back to make sure that the clock of the second filter doesn't appear in the output at smaller bandwidths. A discussion of how the filters work will shed more light on this.

The filter ICs (U15, U16, U19, U20, U25, and U26) are switched-capacitor low-pass types with eight poles apiece. The middle one in each chain of three (U19, U20) sets the overall bandwidth and is a Bessel type (linear phase), selected to minimize impulsive overshoot. The other two are Butterworth types, selected to provide rapid rolloff without too much phase nonlinearity. The cutoff frequency of each filter is determined by the frequency of an applied clock signal, and by a select line which determines whether the cutoff will by 1/75 or 1/150 of the clock frequency for the Bessel filter, or 1/50 or 1/100 of the clock frequency for the Butterworth filters. Gain through the filters inside the passband is near unity, though with a bit of DC offset. Dynamic range is about 60 dB for a full-scale input of +/- 5 Volts. Offset of the second and third pairs of filters is nulled by servo amplifiers (U22, U28) in conjunction with unity-gain signal amplifiers (U21, U27). The servo timing capacitors (C77, C90, C97, C99) are matched before production.

The filter works by sampling the input at the applied clock rate and then processing it. This means that there is a Nyquist point at half the clock rate, above which any signal present at the input will begin to reflect at the output down inside the passband. It is therefore necessary to band-limit the input of each filter so that there is no signal component above half the clock frequency with an amplitude greater than 60 dB below full scale. Furthermore, the clock frequency will appear in the output and must also be filtered out.

Incoming bandwidth is 80 kHz from the 21.4 MHz IF. In the worst case, the selected bandwidth is 200 Hz, which, since we're now at baseband, requires a low-pass filter with a cutoff at 100 Hz. For the middle filter, assuming that a 150:1 ratio has been selected, the required clock rate is 15 kHz. The Nyquist frequency is therefore 7.5 kHz, and we need to be sure that there is no signal going into the filter at or above this frequency. That is what the pre-filter does. It's own Nyquist frequency is well above the incoming bandwidth.

Meanwhile, the output from the middle filter will contain clock products at 15 kHz, which while outside the maximum passband of 10 kHz is still low enough to cause trouble at the recombination stage. A post-filter is provided to take care of the situation. Clock products from the post filter are too high in frequency to bother the recombination circuitry. Note too that clock products from the pre-filter, at 7.5 MHz or so, are too high to bother the middle filter either.

Three different clock frequencies are therefore required. A timebase with multiple outputs has been provided to accommodate this. This timebase consists of a programmable phase locked loop in the synthesizer section and a programmable counter-timer chip (U2) in the DCIF section. The output from the phase-locked loop ranges from 3 to 9 MHz in 50 kHz steps (but is shut off when the DCIF is not in use) at -10 dBm. When it arrives on the DCIF module it is squared up by a comparator (U1) and clocks the counter-timer chip. The counter-timer chip contains three programmable dividers which can range from division by 1 to division by 65,536. One output is provided for each pair of filter chips, matched up in the I and Q channels. Using various combinations of PLL frequency and divider ratio, many different bandwidths may be programmed.

This takes care of filtering. The channel recombination circuit effectively eliminates residual clock content from the module output for wider passbands.

The other big consideration is gain. The following factors contribute:

- fixed-value gain setting and recovery from the mixer/splitter and filter losses
- variable gain setting due to bypassing the end-to-end gain control in the 21.4 MHz IF
- variable gain setting due to (in log mode) bypassing 1/3 of the gain control range in the 21.4 MHz IF
- variable gain setting for noise level equalization, which varies with selected bandwidth

CW signals passing through the DCIF remain constant in amplitude when they are tuned within the selected bandwidth. Impulsive signals are reduced in the same proportion as the bandwidth. In other words, an impulse coming in at 80 kHz bandwidth will be reduced by 52 dB at a selected bandwidth of 200 Hz. Broadband noise is reduced in proportion to the square root of the reduction in bandwidth, so that noise in a 200 Hz bandwidth is 26 dB less than the noise in an 80 kHz bandwidth. In the R-110, noise at the output is equalized with changing bandwidth by adding gain in proportion to the square root of the change. Thus DCIF requires 20 dB more gain at 200 Hz bandwidth than it does at 20 kHz, with many other values in between.

IF gain control has a range of 50 dB. In log mode the DCIF is expected to provide 1/3 of this range, or about 17 dB. The end-to-end gain control in the 21.4 MHz IF has about the same range, but in practice the necessary variation is considerably smaller, on the order of 5 dB. This must also be available in the DCIF.

The DCIF therefore needs a maximum gain control range of at least 25 dB, and optimally over 30 dB to allow for extreme cases. Fixed gain is also necessary. Since the dynamic range of the programmable filters is marginal for log mode, programmable gain has been provided in two places, once after the pre-filter and once after the main filter. This allows for a two step reduction in bandwidth and a two step recovery of gain, which minimizes degradation in dynamic range by keeping impulsive signals closer to full-scale in amplitude, while gradually reducing the bandwidth.

Gain control is implemented by means of multiplying digital to analog converters (U18 and U23) which multiply an applied signal by a digital code. In this case a pair of dual 12 bit DACs are used, each DAC supplying gain control for matching points in each channel in each of its halves. Output is in current mode, and is converted to voltage mode by op-amps (U17, U24), which are again dual units to best match the channels to one another. Trimmers to null any DC offset (R41, R46, R60, R65) are also provided. The DACs are connected in gain mode rather than attenuation mode, so that the gain for each DAC is set by the formula

$$gain = \frac{4096}{code}$$

As this formula indicates, the granularity of gain control is greatest at when gain magnitude is smallest, and vice versa. It is still within 1% of optimum at the highest gains required, however, and is still closely matched between channels at any setting. While very high gain values are possible using this circuit, they are unnecessary as implemented in the DCIF, and in any case will eventually be slew rate limited by the selected ICs.

Once filtering and gain are taken care of, the two channels must be recombined. Since they are in quadrature, a vector sum is required. Algebraically, this means taking the square root of the sum of the squares. Electrically, the job is performed by an "analog computation unit" IC (U37) and surrounding circuitry. The ACU can't deal with negative-going inputs, so each channel is provided with a precision rectifier circuit. Each circuit begins with a fast op-amp (U29, U34) with diodes in the feedback (CR9 - CR12) to produce two half-waves of precision rectification. Each half-wave is provided with a buffer amplifier (U30, U35), and the results are combined in a final summing amplifier (U31, U36) to produce a full-wave rectified output. DC offsets cause proportional distortion here, and are trimmed out both at the inputs (R84, R106) and at the summing amps (R93, R121). Gains in the half-waves are matched by selecting resistors during module test (R85, R88, R112, R116), and gains between the I and Q channels are matched by a trimmer in the Q channel (R105).

The analog computational unit has three inputs called X, Y, and Z, and one output. The output is equal to YZ/X. A pair of unity-gain summing amplifiers (U32, U38) and a buffered delay (L59, C130, L60, C131, and U33) comprise the rest of the recombination circuit. A trimmer (R100) is provided to compensate the gain in the delay amplifier for losses in the reactive components.

The rectified I channel drives both the Y and Z inputs of the analog computational unit, producing I^2/X. The output of the analog computational unit is summed with the delayed, rectified Q channel output (the delay is provided to match the delay of the ACU, which is about 500 uS). The output of this summing amplifier (U38) is again summed with the rectified output of the Q channel, this time without the delay. The result is fed back to the X input of the ACU. The output of the circuit (and of the DCIF) is taken from the output of the first summing amplifier. Algebraically, we have

$$V_o = \frac{I^2}{V_o + Q} + Q$$

$$V_o(V_o + Q) = I^2 + Q(V_o + Q)$$

$$V_o^2 = I^2 + Q^2$$

$$V_o = \sqrt{I^2 + Q^2}$$

The output therefore provides full-wave envelope detection, and at full scale will produce five Volts peak. Dynamic range is about 60 dB for most bandwidths, and impulsive overshoot is well controlled.

Overload detection is performed in two places in each channel: at the output of the gain recovery amplifier following the mixer/splitter, and at the output of the first programmable gain stage. Separate detectors are provided for signals both too positive-going and too negative-going. The detection circuit consists of comparators (U39, U40) whose outputs are wire-ORed to form a single status line. The threshold for the positive-going detector (U39) is set to +5 Volts, while the threshold for the negative-going detector (U40) is set to -5 Volts. Hysteresis is provided around the comparators, inverted by a transistor (Q2) in the case of the negative detector. The status line feeds the logic and control circuit.

The logic and control circuit handles the interface to the cardcage bus and provides address recognition, control bit latching, and status return for the DCIF. Address recognition is provided by decoders (U5, U6). Data and control lines from the bus are passed through buffers (U3, U9) and are passed to the timebase counter-timer (U2), the gain DACs (U18, U23) (along with some address lines), and to a latch (U4) which stores the discrete control bits. The counter-timer and the DACs have internal data latches.

Here is the address mapping of the DCIF:

Addresses 40(hex) - 43(hex) = counter-timer:
- Address 40 = divider #1 load data
- Address 41 = divider #2 load data
- Address 42 = divider #3 load data
- Address 43 = mode control

Address 44(hex) - 47(hex) = first gain DAC:
- Address 44 = I channel load data (lower 8 bits)
- Address 45 = I channel load data (upper 4 bits):
  - Bits 0 - 3 = data
  - Bits 4 - 7 = spare
- Address 46 = Q channel load data (lower 8 bits)
- Address 47 = Q channel load data (upper 4 bits):
  - Bits 0 - 3 = data
  - Bits 4 - 7 = spare

Address 48(hex) - 4B(hex) = second gain DAC:
- Address 48 = I channel load data (lower 8 bits)
- Address 49 = I channel load data (upper 4 bits):
  - Bits 0 - 3 = data
  - Bits 4 - 7 = spare
- Address 4A = Q channel load data (lower 8 bits)
- Address 4B = Q channel load data (upper 4 bits):
  - Bits 0 - 3 = data
  - Bits 4 - 7 = spare

Address 4C(hex) = discrete control bit latch:
- Bit 0 = filter #1 and filter #3 ratio select:
  - 0 = 100:1
  - 1 = 50:1
- Bit 1 = filter #2 ratio select:
  - 0 = 150:1
  - 1 = 75:1
- Bit 2 = input select:
  - 0 = linear mode IF tap
  - 1 = log mode IF tap
- Bit 3 = timebase clock and status driver enable:
  - 0 = disable
  - 1 = enable
- Bits 4 - 7 = spare

Address 4D(hex) = DAC load strobe:
- Bits 0 - 7 = spare

Writing to the DACs consists of sending new data to any DAC address which requires it and then writing to the DAC load strobe address, which will cause all four DACs to be updated simultaneously. Data is buffered in the DACs without being actually applied until the strobe is received. Data written to the strobe address is not used -- it is the act of writing which creates the strobe.

A level shifter (U7) is used to convert ratio select bits to the logic levels used by the filter ICs. The input select signal is level shifted and then drives a transistor switch (Q1), which in turn controls the coil of the input select relay (K1). The timebase and status on/off switch acts as an on/off switch for the DCIF: when the DCIF is not in use it is set to "off", and when the DCIF is activated it is set to "on". It disables the timebase by disabling the comparator (U1) which squares up the input from the timebase PLL in the synthesizer section. It disables the status return by disabling the input to the bus status line drivers (U8). These drivers are configured so that their outputs are either tristate (and pulled up by the control circuitry in the front panel assembly) or active low. Two drivers are used by the DCIF: one for the common back-end overload line (STAT2) and one for the DCIF-specific overload line (STAT6).

4.5 Video Module (A1A9)

The video module (A1A9) consists of the following subsections:

- the wideband AM detector
- the log detector
- the BFO (beat frequency oscillator) and its mixer
- the carrier removal (envelope) filter
- the settable noise filter
- the video output amplifier
- the Z axis output amplifier
- the back end video overload detector
- the logic and control section

Using these circuits, the following receiver functions are performed:

- wideband AM detection
- narrowband AM post-processing (detection performed by DCIF)
- wideband log detection and narrowband log-characteristic compression
- BFO detection
- video noise filtering
- video output
- Z axis output
- audio signal source
- DVM signal source
- AGC signal source
- back-end overload detection

The implementation of each of these functions will be described individually. A block diagram of the video module is shown in figure 4-10.

There are three signal inputs to the video module: two from the 21.4 MHz IF and one from the DCIF module. The 21.4 MHz IF is tapped in two different places, once for AM and BFO detection and once for log detection, so that the gain distribution will work out correctly in each case. The requirements for each are different because the log detector has over 60 dB of dynamic range while the linear detector has only a little more than 30 dB. The BFO uses the same input as the AM detector because here the available dynamic range is not a consideration.

The 21.4 MHz IF input destined for wideband AM detection is routed to the detector circuit through a pad (R24 and R25). The value of the pad is selected during module test to place the full-scale input at the threshold of detector overload. While the detector itself is basically a diode (CR1), dynamic range is maximized by placing the diode behind a tuned amplifier which steps the signal level up to a point where the effect of the turn-on characteristic of the diode is minimized. The tuned amplifier is based on a transistor (Q1) and a low-Q tuned network (L6, L7, C26, R33, R34). The diode is followed by an op-amp (U17). The gain of the op-amp is set during module test (by selecting R76 and R77) to establish end-to-end gain. Another diode (CR2) provides temperature compensation and DC offset balance. The detector circuit is followed by the carrier removal filter, an 8-pole low-pass L-C implementation with its corner at 8 MHz. This filter is also used by the log detector.

The output of the filter provides the input for a second, settable video noise filter. This filter is a one-pole low-pass R-C configuration, in which any combination of four capacitors may be selected by the logic and control circuit. In practice only one (or none) is selected at any given time. Which capacitor is selected depends on the radio's selected bandwidth. The corner frequency for each step is shown in table 4-2.

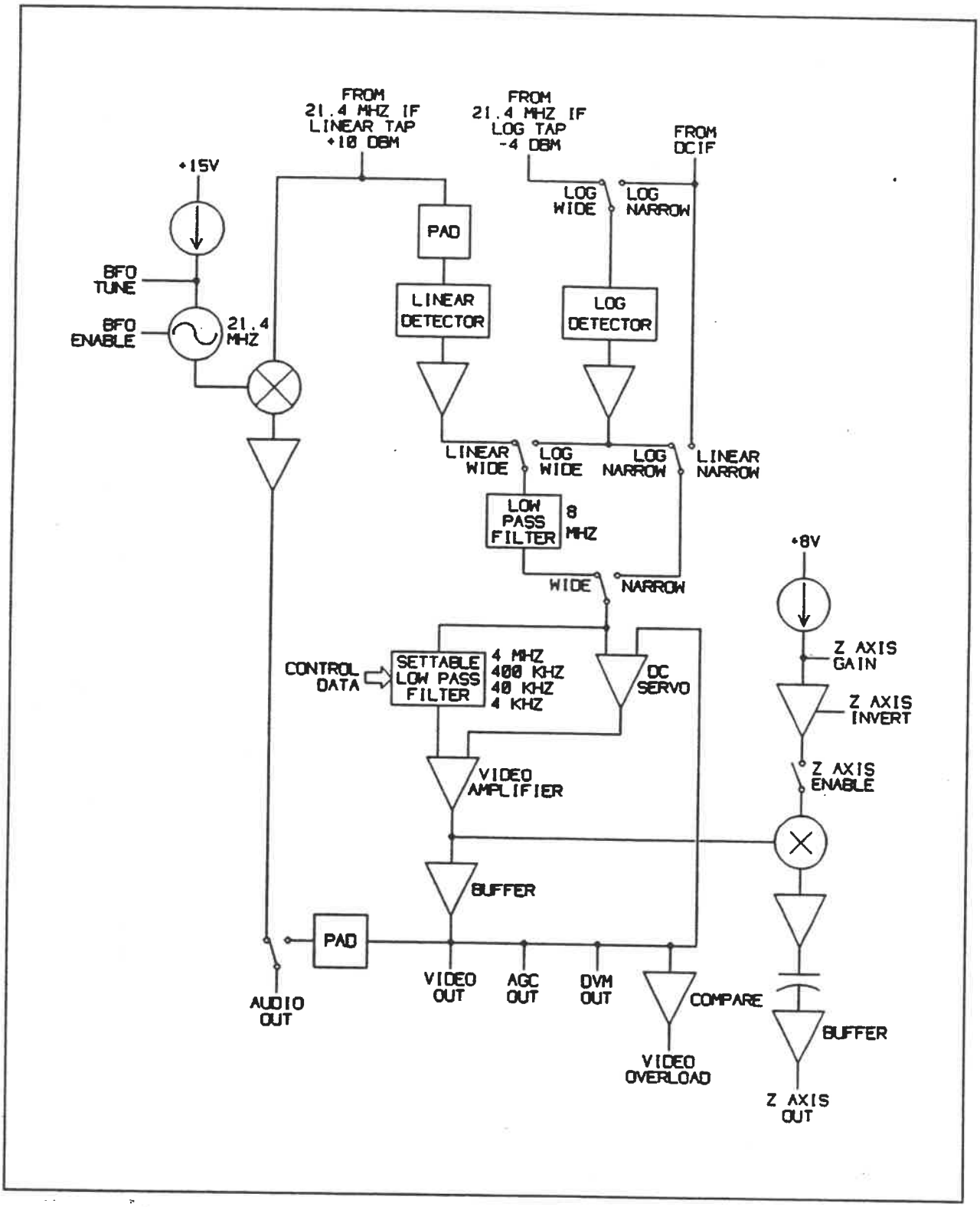


Figure 4-10: Video Module Block Diagram

Table 4-2: Video Noise Filter Selection

Bandwidth Range	Filter Corner
200 Hz - 2 kHz	4 kHz
2.5 kHz - 20 kHz	40 kHz
80 kHz	400 kHz
300 kHz - 1 MHz	4 MHz
4 MHz - 15 MHz	None

The video filter feeds the video output amplifier, which consists of a wideband opamp (U19), followed by a video buffer (U20), and DC-stabilized by a servo amplifier (U18). The servo integrates the difference between the output of the video buffer and the input taken *before* the settable filter, using a very slow time constant. Its output is subtracted from the input taken from the settable filter to eliminate any internal DC offset from the amplifier.

The video buffer is capable of driving multiple 50 Ohm loads, and is used to supply the video, audio, DVM, and AGC outputs, and the detector overload circuit. Of these, only the video and DVM outputs are 50 Ohms, since they are the only ones that need to retain full bandwidth off of the module.

End-to-end gain of the wideband AM detector function is 12 dB, so that a +10 dBm input will produce a full-scale output of 0 to 4 Volts peak. Dynamic range at full scale output is at least 30 dB.

The input for the log detector can come from one of two places, either from the other 21.4 MHz IF input (the one that *doesn't* supply the wideband AM detector) or from the DCIF. Selection is made by a relay driven by the logic and control circuit. A termination resistor is switched onto the 21.4 MHz IF input when it is not in use. Furthermore, the input from the DCIF may be switched around the log detector, bypassing it, when a linear characteristic is desired. When routed through the log detector the DCIF signal, while it arrives already detected and carrier-filtered, is given the same log-compression gain characteristic as the detected signal from the 21.4 MHz IF.

The log detector consists of a pair of log amplifier/detectors (U1 and U2) followed by a linear amplifier (U3) which provides a voltage output. The IF signal from the input is fed in series from the first log amp to the second, while their detected video outputs are summed at the voltage amplifier. An input offset adjustment (R6) is provided to null the output of the log amps. A resistor (R20) is selected during module test to set the full scale output level at the output of the voltage amplifier. The output of this amplifer is fed to the same 8-pole carrier removal filter used by the wideband AM detector, with a relay (K2) performing the selection. From there the signal path is the same as that taken by the wideband AM signal, through the video noise filter and the main video amplifier to the video, audio, DVM, and AGC outputs, and to the Z axis output and detector overload circuits.

Gain is set so that at full scale, every 10 dB coming into the log detector will produce 500 mV at the video output. Dynamic range at full scale is in excess of 70 dB. The RF sections of the log amplifier/detectors have a bandwidth of 120 MHz, while their video outputs have a bandwidth of at least 8 MHz.

The BFO detector consists of a 21.4 MHz Clapp oscillator based on a crystal (Y1) and driven by a transistor (Q4), fine-tuned by a varactor diode (CR3). An on/off switch is provided by a FET switch (U6), which disables the oscillator by removing power from it. Tuning frequency control is provided by a potentiometer on the front panel. A constant current source based on a FET (Q3) drives the front panel control, developing a voltage which varies linearly with its setting while requiring only one "hot" line and a return running off of the module. The voltage derived from the control setting is used to tune the varactor. A trimmer (R112) on the module is used to locate the proper range of tuning adjustment.

The oscillator drives a mixer (U21), the other input of which is the *same* tap of the 21.4 MHz IF used by the wideband AM detector. The difference output generated by the mixer is offset from baseband by an amount determined by the front panel control setting, within a range of +/- 4 kHz. The output of the mixer is filtered to remove unmixed and summed products, and is amplified by an op-amp (U22). The output of this amplifier is sent to the audio output, selected by a FET switch (U6), which is driven from the logic and control circuit. For a full-scale input of +10 dBm, the output will be 1.6 Volts peak-to-peak. Dynamic range is not a consideration because BFO is used for detection of CW signals.

Narrowband AM detection is provided by the DCIF, where detection is a byproduct of the bandwidth-limiting process. Detected narrowband AM arriving from the DCIF may be switched to pass through the log detector by means of a relay (K1). This will result in the same log compression characteristic that is used for wideband AM, but with a slightly different gain distribution, since the DCIF is now part of the signal path. Alternatively, another relay (K2) may switch the signal from the DCIF around both the log detector and the carrier-suppression filter, routing it directly to the envelope filter and the video output amplifier. This allows the linear gain characteristic of the DCIF to be retained, along with a dynamic range much wider than that of the wideband AM detector. In this mode the full-scale input from the DCIF, which is zero to five Volts, produces a zero to four Volt output from the video amplifier, for a net attenuation of the signal. If the log detector is switched in, then a similar overall attenuation applies, although the signal from the DCIF must be attenuated to -4 dBm full-scale before entering the log detector.

Turning to module outputs, the signal for the video output connector on the front panel of the radio is taken from the output of the video output amplifier buffer (U20) through a resistor which establishes a 50 Ohm source impedance. This driving point also provides the source for several more outputs, including the DVM module output and the AGC output, and partially for the audio output. It also drives the overload detector circuit. The output provided for the optional DVM module passes through a resistor which also provides a 50 Ohm source impedance. The output to the AGC circuits doesn't need such wide bandwidth and low noise, however, and so its source resistor is set to give it a source impedance of 750 Ohms, thus reducing the load on the video amplifier. The AGC output feeds a number of AGC amplifiers in the 21.4 MHz IF section. Likewise, the signal to the audio output is first attenuated through a resistive divider and then selected by a FET switch (U10). The other selection available for audio is the output of the BFO circuit, selected by another FET switch (U6). As mentioned above, the output from the BFO circuit is 1.6 Volts full scale, while the resistive divider on the video amplifier produces a full-scale output of 1.3 Volts. The audio output is passed to the audio amplifier circuit on the X Axis/Audio Amplifier PCB in the front panel assembly, which features a volume control and a maximum gain of about 50.

The Z axis output is driven by a separate amplifier which features on/off, gain, and inversion controls. It is also AC-coupled. Gain is set by a potentiometer on the front panel. A constant current source based on a FET (Q2) produces a voltage which is proportional to the control setting while requiring only one "hot" line and a return connection to the front panel control. This voltage drives an op-amp (U4), which develops a DC gain-setting voltage. Inversion control is provided by a FET switch (U6), set by the logic and control circuit, which acts to make the opamp inverting or non-inverting, thus producing either a positive or negative gain-setting voltage ranging from -5 to +5 Volts. The gain-setting voltage from the opamp passes through another FET switch (U6 again) which acts as an on/off switch by reducing the gain-setting voltage to zero when the switch is opened. This will attenuate the Z axis signal by about 60 dB at low frequencies, and by at least 40 dB at 8 MHz.

The gain-setting voltage forms one input for a four quadrant multiplier (U7), the other input for which is taken from the main video amplifier, from a point between the leading op-amp (U19) and the following buffer (U20), via AC-coupling capacitors (C109 and C110). The current output of the multiplier is then converted to voltage by an op-amp (U8). The voltage is then AC-coupled by a set of capacitors (C53, C55, C56), and provided with adequate current drive by a video buffer (U9). The output of the buffer is passed through a resistor to set the source impedance to 50 Ohms. The Z axis output is then routed to a connector on the rear panel of the radio.

With the Z axis amplitude control set to maximum, the amplitude at the Z axis output will be approximately 1.5 times that at the video output, not counting any DC offset at the video output. Bandwidth for each is limited by previous bandwidth, carrier removal, and video noise filtering, except that the low-end corner for the Z axis output is at about 3.8 Hz.

The overload detection circuit consists of a high-speed comparator (U5) connected to the output of the main video amplifier. A trimmer (R44) sets the threshold value, which is 4.1 Volts at the video output. The output of the comparator feeds drivers in the logic and control circuit which place the overload status on the cardcage bus.

The logic and control circuitry consists of address decoding from the cardcage bus (U13, U15), bit latches for the various controls (U14, U16), relay drivers (U12), and status return drivers (U11). There are three double-pole, double-throw relays (K1 - K3), four single-pole, single-throw relays (K4 - K7), and five single-pole, single throw FET switches (U6, U10) to control. In addition, a couple of enable bits are provided for future slideback and pulse stretch options.

The first latch controls the seven relays. It is mapped to cardcage bus address 7E(hex). Bit assignments are as follows:

Bits 0 - 3 = video filter selection:
Bit 0 = 4 MHz filter (K6, C100)
Bit 1 = 400 kHz filter (K7, C101)
Bit 2 = 40 kHz filter (K5, C99)
Bit 3 = 4 kHz filter (K4, C98)
0 = disabled
1 = enabled
Bit 4 = log amp input selection: (K1)
0 = DCIF input
1 = 21.4 MHz IF input
Bit 5 = log/lin detector selection: (K2)
0 = linear detector
1 = log detector
Bit 6 = video output selection: (K3)
0 = from 21.4 MHz detection
1 = from DCIF detection
Bit 7 = spare

In practice, when a lower frequency video filter is selected, higher filters are omitted to save power in the relay coils.

The last three relays (K1 - K3) are set to specific states for each of the various operating modes. Table 4-3 shows the various combinations.

Table 4-3: Video Relay Selection

State	Log Input Selection (K1)	Log/Lin Selection (K2)	Output Selection (K3)
Wideband Linear	DCIF (0)	Linear (0)	21.4 MHz IF (0)
Wideband Log	21.4 MHz IF (1)	Log (1)	21.4 MHz IF (0)
DCIF Linear	DCIF (0)	Linear (0)	DCIF (1)
DCIF Log	DCIF (0)	Log (1)	DCIF (1)

Relay control lines are passed through relay drivers (U12) which provide diode-clamped current sinks for the relay coils. The relays all use 5 Volt coils.

The second latch controls the FET switches and provides spare control bits for future options. It is mapped to cardcage address 7F(hex). Bit assignments are as follows:

Bit 0 = BFO enable:
0 = disable
1 = enable
Bit 1 = Z axis enable:
0 = disable
1 = enable
Bit 2 = Z axis invert:
0 = normal
1 = invert
Bit 3 = slideback enable (future option):
0 = disable
1 = enable
Bit 4 = pulse stretch enable (future option):
0 = disable
1 = enable
Bits 5 - 7 = spare

Most of the FET switches (U6) are open when the controlling latch bit is 0, closing when the bit is set to 1. Only one of the switches (U10), the one which is used to connect the BFO output to the audio output, is the other way around. This allows the same state of the same control bit to control two switches in opposite states.

Finally, the output of the detector overload circuit is routed onto the cardcage bus by a pair of tristate drivers (U11). These are connected so that their outputs are tristate (and pulled high with a resistor) when status is good (no overload), and driven active low when status is bad. Two cardcage status lines are driven: the common back end overload status line (STAT2) and a line dedicated specifically to detector overload status (STAT7). Status is sensed by the processor in the front panel assembly and also appears at the status/control connector on the rear panel of the radio.

4.5.1 Audio Output Amplifier

The audio output amplifier is part of the X axis/audio amplifier PCB (A2A4), located in the front panel assembly behind the audio and video connectors and controls. It takes its input from the audio output of the video module and drives the front panel audio output jack. In between it provides the operator with an output volume control and also mixes in the audible indicator signal from the control section (bypassing the volume control used for the signal from the video module).

The circuit consists of a preamp and a power amp. The signal from the video module passes through DC blocking capacitors (C13 and C14) and a log-taper volume control mounted on the front panel, and is routed from there to the preamp IC (U2). The combination of the DC-blocking capacitors and the volume control potentiometer produce the low-end corner frequency of the bandpass, at about 16 Hz. The preamp provides a gain of 35 for small signals and a diode limiting circuit (CR1 - CR6) which gradually reduces gain for larger signals. A capacitor in the feedback of the preamp (C10) establishes the high-end corner frequency of the bandpass at about 32 kHz. The input from the audible indicator circuit located on the interface PCB in the front panel assembly is passed through a DC-blocking capacitor (C5) and is mixed with the output of the preamp at the input of the power amp IC (U1). Gain for the input from the preamp is 1.5, while gain for the input from the audible indicator is unity. The output of the power amp is passed through a current-sensing resistor (R1) which allows the power amp to limit current to about 3 Amps. The output is routed to the front panel audio output jack, where it can drive a low-impedance (8 Ohms or less), fairly reactive load to about 4 Volts peak before the soft limiting in the preamp takes over.

The audible indicator signal is level-controlled back on the I/O PCB (A2A2). At full output it is about 2 Volts peak. Full-scale input from the video module is about 1.3 Volts peak from the linear detector and about 1.6 Volts peak-to-peak from the BFO detector. With the volume control set to maximum, gain overall gain for the signal from the video module is 52.5.

The audio amplifier shares the X Axis/Audio Amplifier PCB with the X axis output buffer, which is described in paragraph 4.8.3. The module is provided with two separate pairs of power supplies, one pair to supply the X axis buffer and the audio preamp, and one pair to supply the audio power amp. Each pair of supplies is provided with a separate return, and grounds on the module are separated from one another. The audio output jack on the front panel is isolated from the sheet metal with insulating washer, so that the audio output is completely isolated from the rest of the radio. This was done in order to prevent the high current draw at the audio output from modulating the supplies to the other modules. In addition, the audio power amp is provided with large filter capacitors (C1, C6) to reduce current surges on its supply lines. Separate regulators are provided for it (and the analog supply requirements of the control section) in the power supply.

The audio power amp IC is heatsinked to the front panel bulkhead assembly.

4.6 Synthesizer Section

The synthesizer section produces the fixed and tuneable local oscillator frequencies used for converting the signal at the receiver's input to the various intermediate frequencies. It also provides the programming frequency for the swiched capacitor filters in the DCIF. The section is implemented in the following modules:

- fixed LO synthesizer module, A1A15
- low frequency synthesizer module, A1A16
- microwave synthesizer module, A1A17
- part of the microwave RF module, A1A1
- part of the preselector module, A1A2

In addition, the synthesized frequency produced by the fixed LO module for the switched capacitor filters in the DCIF (which isn't fixed in frequency despite the name of the module) is passed to programmable dividers in the DCIF module (A1A11), which effectively act as part of the synthesizer.

The block diagram of the section is shown in figures 4-11 and 4-12.

4.6.1 Local Oscillator Usage

The receiver uses three different conversion schemes and a total of four intermediate-frequency stages (including the DCIF). The synthesizer generates the local oscillators used for these stages, as shown in table 4-4.

Table 4-4: Local Oscillator Usage

IF Frequency	LO Frequency
Band 1: 1 kHz - 250 kHz	
First IF: 3.001 MHz - 3.25 MHz	3 MHz
Second IF: 21.4 MHz	24.401 MHz - 24.65 MHz
Band 2: 250 kHz - 15 MHz	
First IF: 21.4 MHz	21.65 MHz - 36.4 MHz
Band 3: 15 MHz - 1 GHz	
First IF: 1445 MHz - 1455 MHz	1470 MHz - 2450 MHz
Second IF: 545 - 555 MHz	2 GHz
Third IF: 21.4 MHz	523.6 MHz - 533.6 MHz

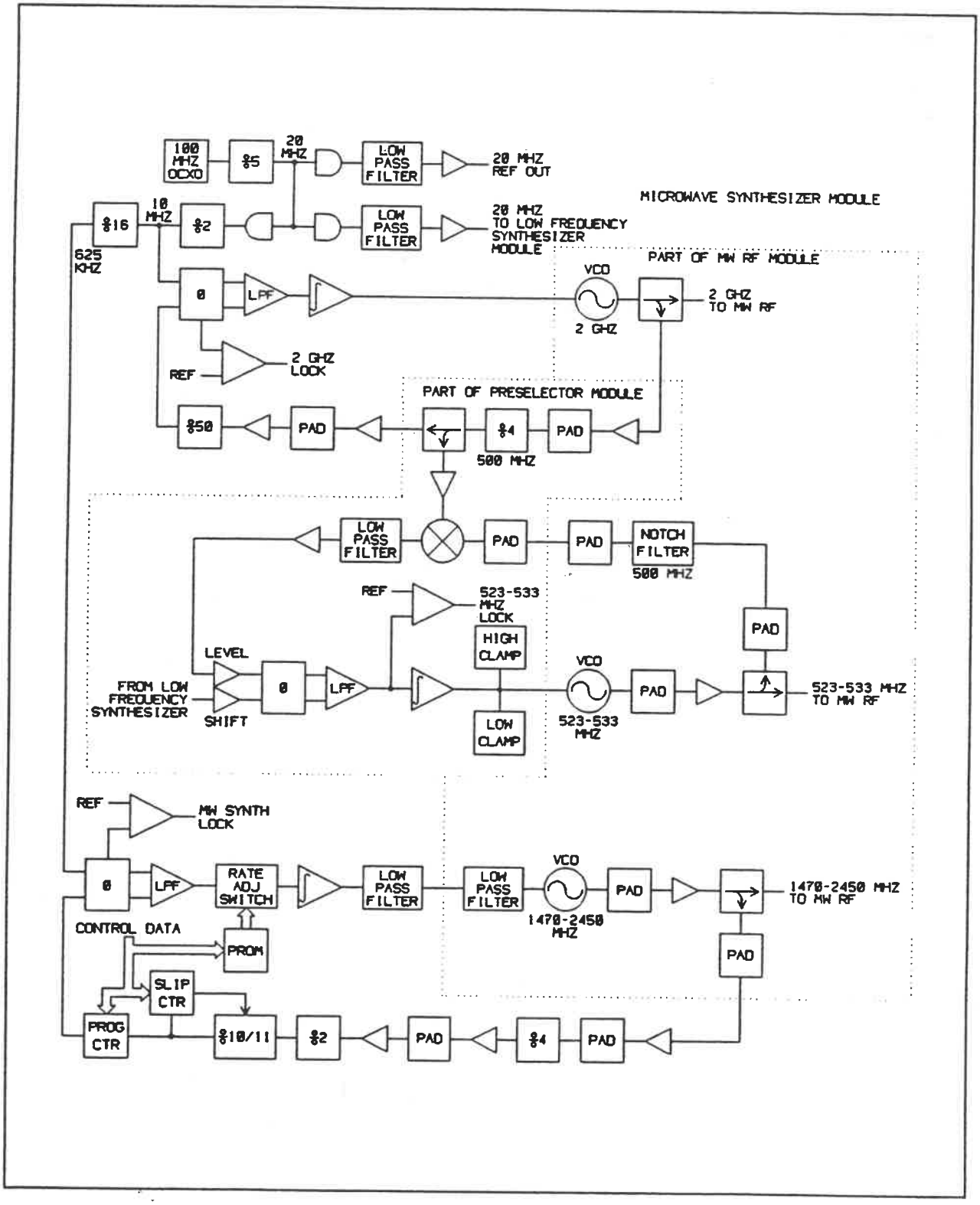


Figure 4-11: Synthesizer Section Block Diagram Part 1

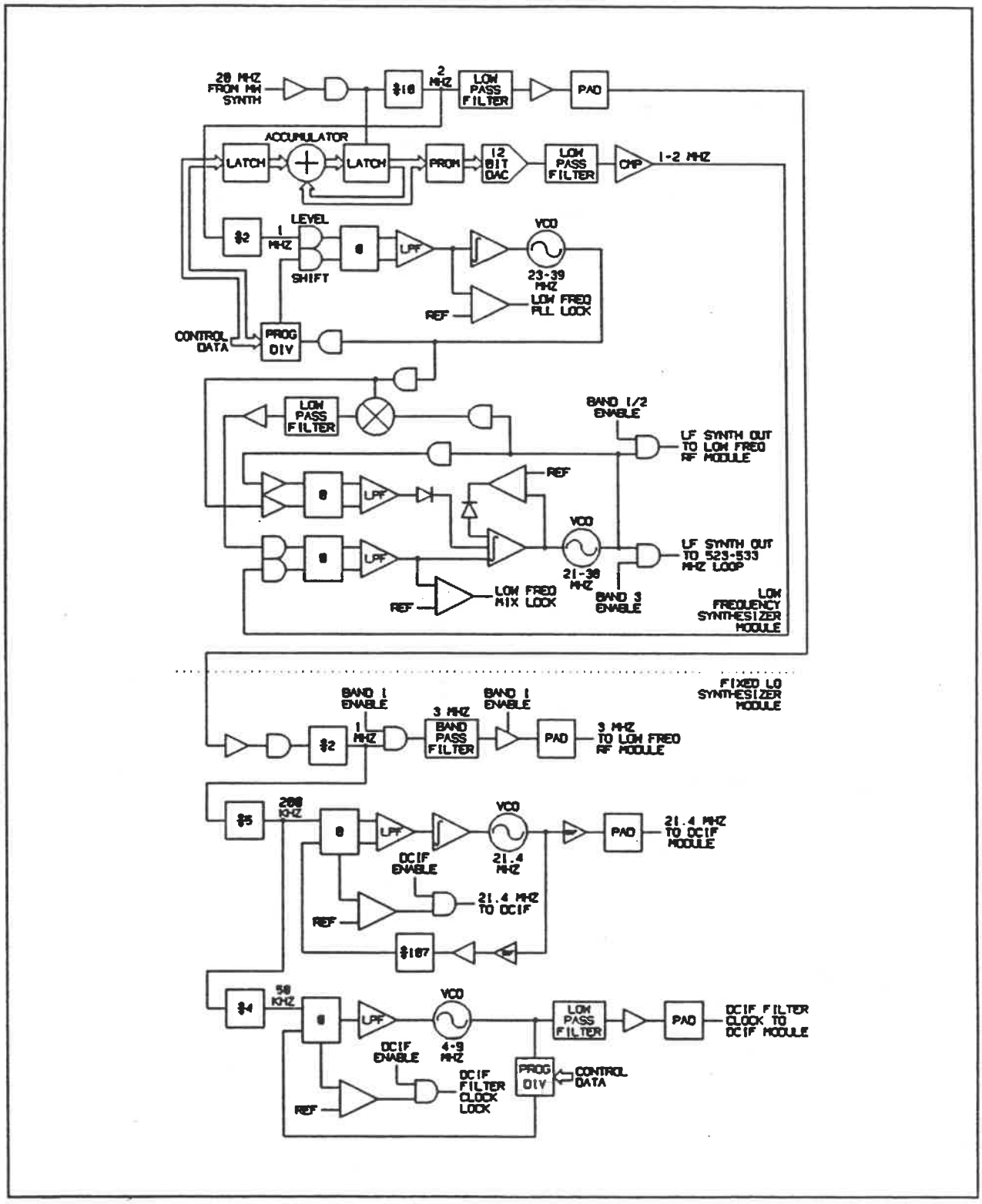


Figure 4-12: Synthesizer Section Block Diagram Part 2

In order to reduce the LO bleed-thru in the front end of the receiver when tuned between 15 MHz and 20 MHz (bottom end of band 3), the first and third LO frequencies are shifted. The first LO is moved up 5 MHz and the third LO is moved down 5 MHz so that the result is still 21.4 MHz for the third IF. This puts the L.O. bleed-thru after the upper break frequency of the first IF and before the lower break frequency of the second IF. As a result, when the receiver is tuned below 20 MHz the first LO is well out of band for the first and second IF, providing maximum LO rejection.

4.6.2 Microwave Synthesizer Module (A1A17)

This module contains the 100 MHz oven-stabilized crystal oscillator (U33) used as the reference for the entire receiver. It contains the control sections for the two microwave synthesizers, the other parts of which are located in the microwave RF module (A1A1) and the preselector module (A1A2). It generates a 20 MHz reference for the low frequency synthesizer module (A1A16), and another 20 MHz for the rear panel reference output jack. Finally, there is a cardcage backplane interface circuit.

One of the microwave synthesizers produces a fixed 2 GHz output. The other one is programmable from 1470 MHz to 2450 MHz in 5 MHz steps.

The crystal oscillator feeds an ECL digital divider (U36) which outputs 20 MHz. This is buffered by TTL (U18), amplified (U16), and padded (R48 - R50) to -10 dBm for output to the low frequency synthesizer module (A1A16). The ECL output is again buffered by TTL (U18), amplified (U17), and padded (R55 - R57) to -10 dBm for output to the rear panel reference output connector. Finally, the ECL output is buffered by TTL (U19), divided by 2 using a toggle flip-flop (U22) to yield 10 MHz, which is the reference for the 2 GHz synthesizer. The 10 MHz reference is then divided by 16 (U34) to yield 625 KHz, the reference for the programmable microwave synthesizer. A jumper selection (E5 - E7) is provided to bypass the divide-by-2, yielding a 1.25 MHz reference for future improvement of the programmable synthesizer.

The 10 MHz reference feeds the phase comparator (U24) of the 2 GHz synthesizer. The outputs of the phase comparator are filtered and combined (U21), and then integrated (U20) to form the tuning voltage for the loop VCO, which is located in the microwave RF module (A1A1A4 U4). Besides feeding the microwave module conversion circuits, the output of the VCO is padded (A1A1A4 R16 - R18, R19 - R21) to -12 dBM and sent to the preselector module, where it is re-amplified (A1A2A1 U1) and padded (A1A2A1 R2 - R4), and drives a divide-by-4 prescaler (A1A2A1 U2), yielding 500 MHz. The output of the prescaler drives a splitter (A1A2A1 U3), one output of which provides a 500 MHz fixed frequency to the 530 MHz PLL circuit. The other output is routed back to the microwave synthesizer module at -16 dBm, where it is amplified (U25, U26) and padded (R76 - R78) to drive a divider chain consisting of a divide-by-2 (U40) and two divide-by-5s (U39, U38), yielding 10 MHz at the output. This output is fed back to the other input of the phase comparator, closing the loop. Another output of the phase comparator is filtered (R72, C70) to drive a level comparator (U37) which acts as a lock detector. It drives a LED (CR9) and is fed to the status return portion of the cardcage backplane interface circuit.

The programmable microwave synthesizer is based on the 625 kHz reference. The reference drives one input of the phase comparator (U15). The outputs of the phase comparator are filtered and combined (U14), and then integrated (U13). The integrator provides the tuning voltage for the VCO (A1A1A2 U3) located in the microwave RF module. The output frequency of the VCO is nonlinear with tuning voltage, which makes the loop gain frequency-dependent. To normalize the loop gain to some extent a FET switch (U12) is used to vary the integration rate with tuned frequency. Since there are only five possible settings, this is a fairly rough adjustment. In addition, a trimmer (R30) is provided to trim out the offset of the phase comparator and combiner. The trimmer is set to minimize the reference sidebands in the output of the VCO. Since the offset contribution from the phase comparator and combiner depends on the setting of the corrective FET switch, a second FET switch (U11) is provided to scale the contribution of the trimmer as well. Both FET switches are controlled by a lookup table in PROM (U5), which is addressed by the coarse tuning data supplied to the loop dividers.

The phase comparator also drives a low-pass filter (R47, C47) and level comparator (U37) which acts as a lock detector. The output of the level comparator drives a LED (CR8) and is returned on the cardcage backpane via the interface circuit.

In the microwave RF module, the output of the VCO is padded (A1A1A2 R4 - R6) and amplified (A1A1A2 U4) to provide the 1470 - 2450 MHz LO for the microwave hardware. It is coupled by a microstrip directional coupler, padded (A1A1A2 R9 - R11) to yield -15 dBm, and returned to the microwave synthesizer module. There it is amplified (U7) and padded (R19 - R21), and ends up feeding a divide-by-4 prescaler (U9), yielding 367.5 - 612.5 MHz. The output of the prescaler is amplified (U10), padded (R15 - R17), and amplified again (U8) to drive a divide-by-2 prescaler (U4), yielding 183.75 - 306.25 MHz. There is therefore a fixed prescaling division by 8, which is what yields the 5 MHz tuning steps from the 625 kHz loop reference. The output of the second prescaler feeds the programmable divider circuit, consisting of a divide by 10/11 prescaler (U1), a decade skip counter (U3), and an 8 bit programmable divider (U6). The 10/11 prescaler divides the incoming frequency by 11 until the skip counter counts out, whereafter it divides by 10. The skip counter halts after counting out, until the programmable divider produces an output. This output reloads the skip counter and starts the cycle over again. In this way the skip counter implements the less significant part of the load data, and the programmable divider the more significant part. The output of the programmable divider drives the remaining input of the phase comparator, completing the loop.

The load data for the loop is determined by first dividing the desired output frequency by 5 MHz and forming the quotient in decimal. The last (units) digit is the load value for the skip counter. The remaining digits are then formed into a binary number. The programmable divider is loaded with one less than this number to provide the necessary ratio.

Finally there is the cardcage backplane interface circuit. This consists of a data bus buffer (U29), a pair of data latches (U27, U28), and address decoders (U30, U32). There are also tristate drivers (U31) for the status return lines, and enabling gates (U35) for them. The programmable loop lock status signal drives the backplane's common lock status line (A21) and its own individual line (B17) as well. The 2 GHz loop lock status signal drives the common lock status line as well, and also its own individual line (A16).

The two data latches store 6 bits each. One controls the programmable loop skip counter and provides an enable bit for the status return. The other controls the programmable divider, which uses 6 bits of load data. Addressing is as follows:

Address 78(hex) = skip counter latch:
Bits 0 - 3 = skip counter bits 0 - 3
Bit 4 = unused
Bit 5 = status return enable

Address 79(hex) = programmable divider latch
Bits 0 - 5 = programmable divider bits 0 - 5

Since the microwave synthesizers are only used when tuning in band 3, the status return enable bit is effectively a tuning-in-band-3 select bit. The loops remain running even when tuning is not in band 3. The PROM which controls the FET switches in the programmable loop is controlled by the five most significant bits of the programmable divider data.

4.6.3 523 - 533 MHz Mixer Loop

In tuning band 3 the signal is first converted to 1445 MHz - 1455 MHz, then to 545 - 555 MHz, then to 21.4 MHz. The conversion to the third IF requires an LO ranging from 523.6 MHz - 533.6 MHz. This is the function of the circuit described here. It consists of a mixer loop which adds the 500 MHz fixed frequency (divided from the 2 GHz fixed LO output) to the band 3 output of the low frequency synthesizer module (A1A16). The circuit is located in the preselector module (A1A2) and part of the microwave RF module (A1A1).

The output from the programmable low frequency synthesizer arrives at -10 dBm and is converted to TTL (A1 Q2) to drive one input of the phase comparator (A1 U7). This is located on a subassembly inside a can for shielding. The outputs of the phase comparator are filtered and combined (U7) and then integrated (U6) to form the VCO tuning voltage. The tuning voltage is clamped on the low side by a sensing circuit (U3, U4) which compares it to a reference set by a trimmer (R13). It is clamped on the high side by another sensing circuit (U3, U5) set by another trimmer (R14). The tuning voltage drives the VCO (A1A1A6 U3) located in the microwave RF module. The output of the VCO is padded (A1A1A6 R8 - R10) and amplified (A1A1A6 U2) to drive a splitter (A1A1A6 U1). One output of the splitter drives the signal conversion mixer, while the other one is padded (A1A1A6 R4 - R6), high-pass filtered (A1A1A6 L1, T1, T2, C1, C3) to provide reverse isolation from the 500 MHz fixed frequency, and padded again (A1A1A6 R1 - R3) to -12 dBm, at which level it is returned to the preselector module. There it is padded once more (A1 R9 - R11) and mixed (A1 U5) with a 500 MHz fixed frequency picked off from the 2 GHz fixed LO. The 2 GHz fixed LO contains a divide-by-4 preselector (A1 U2) followed by a splitter (A1 U3). One output of the splitter is padded (A1 R5 - R7) and amplified (A1 U4) to provide the 500 MHz input to the mixer. The output of the mixer is filtered (A1 L4, L5, C13, C15, C37) to select the difference component, and then amplified (A1 U6) and converted to TTL (A1 Q1) to drive the other input of the phase comparator, completing the loop.

The output needs to be 523.6 - 533.6 MHz to properly convert the incoming 545 - 555 MHz signal to 21.4 MHz. The fixed input to the mixer contributes 500 MHz, so the programmable low frequency synthesizer needs to be tuned in the range of 23.6 MHz - 33.6 MHz in band 3.

4.6.4 Low Frequency Synthesizer Module (A1A16)

This module contains a direct digital synthesizer (DDS), settable from 1 to 2 MHz, a tuneable phase locked loop programmable from 19 - 38 MHz, a mixer loop which combines the output of the programmable loop with the output of the DDS, a 2 MHz pickoff to provide a reference for the fixed LO synthesizer module (A1A15), and a logic interface for the cardcage backplane. The mixer loop is provided with safety features to ensure that it is always in the proper relationship to its two inputs.

The reference for the module comes in at -10 dBm from the microwave synthesizer (A1A17) module. It is amplified (U2) and then squared up by a logic gate (U3). This provides the clock for the DDS. It is also divided by 10 using a digital bi-quinary divider (U4), producing 2 MHz. This is filtered (C4, L31, C115), amplified (U1), and then set to -10 dBm using a pi network (R2 - R4). This is sent to the fixed LO module, where it is used as the reference for the 3 MHz multiplier, the 21.4 MHz fixed LO used by the DCIF, and the DCIF filter clock. The 2 MHz output from the divider is also divided again by 2, using the other section of the bi-quinary divider (U4), yielding 1 MHz. This is the reference for the programmable loop.

The direct digital synthesizer is contained mostly in an LSI circuit (U5). This IC contains two duplicate implementations, of which only one is used by the module. The circuit consists of a 32 bit accumulator, plus latches. There are four input latches, each connected to the incoming data bus. Data is loaded one latch at a time, determined by the applied address. When all four are loaded the set can be applied simultaneously to a second latch, 32 bits wide, by a strobe. This 32 bit latch forms one input of the accumulator. The accumulator consists of a 32 bit adder and output latch, with the output of the latch wrapped around to become the other input. the strobe for the output latch is supplied by the applied reference clock, which the module supplies at 20 MHz as described above. If the value loaded into the input latch is determined to be the fraction of the output frequency expected with each reference clock, the circuit then becomes a phase accumulator and the output latch is an indication, in encoded digital form, of the current phase of the output waveform.

The LSI circuit contains the phase accumulator and a lookup table. The output latches of the phase accumulator supply a 12 bit wide lookup table in ROM which provides the encoded values for a sine wave (actually in cosine form so that the waveform will be at its endpoints when the accumulator rolls over, rather than at the more sensitive zero crossings). The remainder of the DDS consists of a 12 bit latch (U6, U7), strobed by the LSI circuit, which acts to deskew the data. The latches are followed by a high-speed 12 bit DAC (U9), the output of which is a stairstep approximation of a sine wave. The stairstep is at the reference frequency of 20 MHz, while the sine wave is at a frequency determined by both the reference frequency and the value loaded into the input latches. The DAC is followed by a low-pass filter (A3 L1 - A3 L3, A3 C1 - A3 C3) to remove the stairstep, and a comparator (A3 U1) to square up the result. The filter and the comparator are located on a subassembly (A1A16A3) inside a can for shielding. The output of the comparator forms one of the inputs for the mixer loop.

The DDS is set to range from 1 - 2 MHz. The output is the value loaded into the input latches, divided by 2^32, times 20 MHz, or

$$Freq = \frac{N}{214.7483648}$$

in Hz, where N is the load value. Resolution is sufficient to set the frequency to within a small fraction of 1 Hz.

The 1 MHz reference for the programmable phase locked loop is derived from the 20 MHz reference from the microwave synthesizer module, as described above. The reference is converted to ECL logic levels (U16) and feeds one input of the phase comparator (U17). The other input of the phase comparator comes from an 8 bit programmable divider (U12), again converted to ECL levels (U16 again). The outputs of the phase comparator are filtered and combined (U30), and then integrated (U31). The filtered and combined signal also drives a window comparator (U27) which acts as a lock detector. The output of the window comparator drives an LED (CR1) and the bus interface logic described below. The integrated output forms the tuning voltage for the VCO, which is located on a subassembly (A1A16A1) inside a can, for shielding. This subassembly has four outputs, three of which are used, and two enable inputs, neither of which is used. One output is squared up by a comparator (U14) and drives the programmable divider (U14). The other two feed the mixer loop.

A trimmer (R36) is provided to trim out the offset of the phase comparator, combiner and integrator. The trimmer is set so that the reference sidebands in the VCO output are minimized.

The frequency of the programmable loop is set according to the equation

$$Freq = (N+1) * 1 \text{ MHz}$$

in 1 MHz steps, where N is the divider load code. The legal range is 19 to 38 MHz.

The mixer loop has as its inputs the DDS output and the programmable PLL output. The output of the mixer loop is the difference between them, so that it can range from 17 to 37 MHz with resolution to a small fraction of 1 Hz.

The reference for the mixer loop phase comparator (U19) is fed by the DDS output, converted to ECL logic levels (U18). The outputs of the phase comparator are filtered and combined (U20) and then integrated (U21). The filtered and combined signal feeds a window comparator (U27) which acts as a lock detector. The output of the window comparator drives a LED (CR2) and the bus interface logic described below. The integrated output forms the tuning voltage for the loop VCO, located on a subassembly (A1A16A2) located inside a can, for shielding. This subassembly is identical to the one used for the programmable loop, but in this case all four of the outputs and both of the enables are used. One output is sqared up by an amplifier (U29) running in saturation. The output of this amplifier drives a transformer (T1) with a 13:1 impedance ratio. The transformer provides a 50 Ohm drive for the LO input of a mixer (U32) at about +6 dBm. The other input of the mixer is driven by the output of the programmable PLL through a pad (R81 - R83) which is set to minimize the unwanted mixing products at the output. The output of the mixer is low-pass filtered (L27, L28, C95 - C97) to extract the difference product. The filter feeds another amplifier (U33), also running in saturation, which in turn drives another 13:1 transformer (T2), which drives the other input of the phase comparator through a length of 50 Ohm line (W2) and an ECL level converter (U18 again).

A trimmer (R58) is provided to trim out the offset of the phase comparator, combiner and integrator. The trimmer is set so that the reference sidebands in the VCO output are minimized.

The low-pass filter following the mixer is cut to about 2.5 MHz. Two aspects of the mixer loop are therefore worth noting:

- If the mixer VCO is more than 2.5 MHz away from the programmable loop VCO then the mixer loop is open, since the mixer output will be cut off by the filter which follows it. This may be the case at powerup.

- The mixer loop may lock on either the sum or the difference of the programmable loop and the DDS.

Additional circuitry has been provided to ensure that the mixer loop locks and operates in the correct orientation. A phase comparator (U25) compares the buffered (U26) output of the mixer loop to the buffered (U28) output of the programmable loop. The outputs of the phase comparator are filtered and combined (U24). The filtered and combined output drives the mixer loop integrator so that if the mixer loop frequency is ever higher than that of the programmable loop, the sensing circuit will then force the mixer loop VCO frequency down.

A comparator (U23) compares the mixer loop VCO tuning voltage to a trimmable reference (R68). It senses when the VCO is tuned below its legal minimum. When it triggers it charges a capacitor (C85) which then feeds the loop integrator, forcing it to tune the VCO higher as it slowly discharges.

If the mixer loop VCO is tuned more than 2.5 MHz below the programmable loop, but still within its legal range, the mixer filter will block the difference frequency, opening the loop. However, the loop phase comparator will then see no input from the filter, which it interprets as zero frequency, a too-low condition. It will therefore increase the VCO frequency in normal fashion, until the loop locks as usual.

There are two more outputs from the mixer loop VCO subassembly, each with its own enable input. One is used for the band 3 tuning and is delivered to the preselector module (A1A2) through a pad (R99 - R101) which sets the level to -10 dBm. The other is used for band 1 and 2 tuning and is delivered to the low frequency RF module (A1A5), again at -10 dBm. The enable lines are driven by the cardcage backplane interface circuitry described below.

Overall, the output frequency of the module is

$$\begin{aligned} Freq_{OUT} &= Freq_{PLL} - Freq_{DDS} \\ &= [(N_1 + 1) * 1\ \text{MHz}] - \left[\left(\frac{N_2}{214.7483648}\right) * 1\ \text{Hz}\right] \end{aligned}$$

where N_1 is the PLL load code and N_2 is the DDS load code.

The cardcage interface circuitry consists of a data bus buffer (U11), a data latch (U10), address decoding (U8, U13, U15), and tristate drivers (U22) for the status return lines. Lock detection from the programmable loop drives the backplane's common lock status line (A21) and its own discrete status line (A15). Lock detection from the mixer loop also drives the common lock status line (A21), and again its own discrete status line (B15).

The DDS IC requires 32 consecutive addresses. These are allocated to bus addresses 00(hex) - 1F(hex). The data latch is redundantly mapped into addresses 0E(hex)/1E(hex) within the address space of the DDS. This is the address which strobes the second stage input latch of the DDS, allowing the accumulator input data, which must be loaded in four pieces, to be applied to the accumulator simultaneously. By placing the data latch at this address as well, the programmable loop, the load value for which is supplied by the data latch, may also be updated at the same time, since data applied to the DDS strobe address is unimportant.

Data latch bit assignments are as follows:

Bits 0 - 5: programmable loop divider code
Bits 6 - 7: band select code:
- 00 = band 1 enable
- 01 = band 2 enable
- 10 = band 3 enable
- 11 = unused

The band select code is decoded with a spare section of one of an address decoder IC (U15). The band 1 and band 2 selects are ORed (U3) to provide a combined band 1/2 select line. The band 1/2 select drives the band 1/2 output enable of the mixer loop VCO subassembly. The band 3 select does the same for the VCO band 3 output enable.

4.6.5 Fixed LO Synthesizer Module (A1A15)

The low frequency RF input module (A1A5) requires a 3 MHz fixed LO to upconvert the low frequency input by that amount. This is provided by the fixed LO module at -3 dBm. The 20 MHz reference from the low frequency synthesizer/DDS module (A1A16) arrives at -10 dBm and is amplified (U2) and then squared up by a logic gate (U3). It is then divided by 2 using a toggle flip-flop (U19), yielding 1 MHz. The output is passed through an enabling gate (U3 again) and filtered (L7 - L11, C20 - C25) for the third harmonic at 3 MHz. Proper operation of the filter depends on the input level, set by a resistive divider (R24, R25). The result is amplified (U8) and set to -3 dBm by a pi network (R26 - R28). This provides the output for the low frequency RF module. Everything past the enabling gate is located inside a can, for shielding.

The DCIF uses a fixed 21.4 MHz reference to convert the 21.4 MHz IF directly to baseband. The clock circuit, located in the Fixed LO module (A1A15), is a single phase-locked-loop. The reference for the loop is taken from the 3 MHz multiplier circuit described above at the point at which it is at 1 MHz. From there it is divided by 5 to form 200 kHz, using a bi-quinary digital divider (U6). This is the reference for the loop. The phase comparator (U18) compares the reference to the output of an 8 bit divider (U4). The output of the phase comparator is filtered (U16) and integrated (U15) to form the control voltage for a VCO based on a transistor (A1 Q1) and a tuning diode (A1 CR2). The output of the oscillator is buffered (A1 U2) off of the module at -10 dBm and is sent to the DCIF module (A1A11). It is also buffered (A1 U1) and amplified (A1 U3) to feed the divider (A1 U4) which feeds the phase comparator. The divider provides a ratio of 107, which establishes a VCO output of 21.4 MHz in phase lock. A low-pass filter (R43, C53) and comparator (U17) connected to the phase detector provides lock detection. The output of the comparator drives a LED (CR2) and backplane status lines (the common lock line at A21 and the 21.4 MHz-specific line at A14) through an enabling gate (U13) and tri-state drivers (U14). The VCO, its output buffers and amplifier, and the loop divider comprise a subassembly (A1A15A1) located between vertical shielding walls, for isolation.

The DCIF also requires a programmable timebase for its switched-capacitor filters. This is provided in the form of a phase locked loop on the fixed LO module and programmable dividers on the DCIF module. The phase locked loop can range from 4.8 MHz to 8.8 MHz. The reference for the loop is taken from the 200 kHz reference used by the fixed 21.4 MHz phase locked loop and is divided by 4 using the remaining sections of the bi-quinary counter (U6), yielding a 50 kHz reference for the loop. The phase comparator (part of U5) compares this to the output of an 8 bit digital counter (U4). The output of the phase comparator is filtered and integrated (part of U5 again) and supplies the control voltage for the VCO (still another part of U5). The output of the VCO feeds the divider, and is also filtered (C4, L17, C54), amplified (U1), and set to -10 dBm by a pi network (R1 - R3) to feed the DCIF. The divider may be set from about 96 to 176 to provide the required range of outputs, in 50 kHz steps. A low-pass filter (R15, C13) and comparator (U7) connected to the output of the phase comparator provides lock detection. The output of the comparator drives a LED (CR1) and backplane status lines (the common lock line at A21 and the DCIF filter clock-specific line at B14) through an enabling gate (U13) and tri-state drivers (U14).

The backplane interface for the module consists of a data bus buffer (U10) and address decoding (U9, U12), plus a two bit control latch (U11). One bit is set according to whether tuning is in band 1. When set, the bit is used to enable the 3 MHz multiplier through its enabling gate (U13). It also is used to switch the supply to the 3 MHz output amplifier (U8) on and off via a transistor switching circuit (Q1 - Q3). The other control bit is set according to whether the DCIF is in use. When set it is used to enable the DCIF filter clock VCO (U5) and divider (U4), the fixed 21.4 MHz divider (A1 U4), and the enabling gates (U13) for the status line drivers. It is also used to switch the supply to the 21.4 MHz VCO (A1 Q1) on and off via a transistor switching circuit (Q4 - Q6).

The data bus feeds the control latch and the DCIF filter clock loop divider (U4). The address usage is as follows:

Address 70(hex) = control latch:
- bit 0 = band 1 select
- bit 1 = DCIF select
- bits 2 - 7 = unused

Address 70(hex) = DCIF filter clock divider ratio
- bits 0 - 7 = ratio bits 0 - 7

The output of the DCIF filter clock will be

$$Freq = (255 - N) * 50\ \text{kHz}$$

where N is the code sent to the divider address.

4.7 Cardcage Backplane (A1A20)

The cardcage backplane is a passive implementation which provides power and digital control signals for the plug-in modules and the microwave RF module (A1A1). The backplane provides 16 sockets for plug-in modules, numbered J2 - J17. The assembly numbers of the plug-in modules match the socket that they plug into (e.g., the video module, A1A9, plugs into the J9 socket of the backplane). J1 is the power and control header for the microwave RF module, which, while it doesn't plug directly into the backplane, fits adjacent to it and is connected to it via a discrete-wire pigtail. See table 4-5.

Table 4-5: Cardcage Backplane Connector Usage

Connector	Usage
J1	Microwave RF Module (A1A1) Cable
J2	Preselector Module (A1A2)
J3	Spare
J4	Spare
J5	Low Frequency RF Module (A1A5)
J6	21.4 MHz IF Amplifier Module (A1A6)
J7	Spare
J8	21.4 MHz IF Filter Module (A1A8)
J9	Video Module (A1A9)
J10	Spare
J11	DCIF Module (A1A11)
J12	Spare
J13	Spare
J14	Spare
J15	Fixed LO Synthesizer Module (A1A15)
J16	Low Frequency Synthesizer Module (A1A16)
J17	Microwave Synthesizer Module (A1A17)
J18	Control Section Interface Cable

Power is provided from the power supply via discrete wires, passing through the cardcage sidewall via filtered feed-thrus. Some supplies are shared with the front panel assembly. Power supply voltages available on the backplane include:

- +5 VDC and separate return
- +/- 8 VDC and separate return
- +/- 15 VDC and separate return
- +50 VDC and separate return

Note that while the return lines for the various power supply voltages are kept separate by the backplane, the microwave module requires +5 VDC, -8 VDC, and +15 VDC, but uses only the +5 return and the +/- 15 VDC return. Furthermore, these two returns are bridged together inside the module.

The sockets for the plug-in modules consist of 64 contact, double-row DIN connectors. Power distribution and connections to the front panel assembly account for most of the contacts, which for these signals are bussed in common across the backplane. The remaining lines are available for use by discrete logic signals between specific sockets, and it is this set of connections which prevents any plug-in module from working in any socket.

The interface to the front panel assembly is in the form of a 37 conductor ribbon cable, attaching to the backplane at J18. All of these lines are bussed across the backplane as a single group, and are located on inside layers of the backplane, shielded on top and bottom by the +5 VDC and return planes. The driven lines are active only when a command is being issued to a plug-in module, and the status return lines are active only when a status change occurs, so most of the time all of the lines are in static states, which reduces noise.

The standard connector pinout for the plug-in modules is shown in table 4-6. The current selection of dedicated traces is shown in table 4-7. The usage of the status signal lines is shown in table 4-8.

Table 4-6: Backplane Connector Standard Pinout

Contact	Usage	Contact	Usage
A1	-15 VDC	B1	-15 VDC
A2	15 RTN	B2	15 RTN
A3	+15 VDC	B3	+15 VDC
A4	-8 VDC	B4	-8 VDC
A5	8 RTN	B5	8 RTN
A6	+8 VDC	B6	+8 VDC
A7	+50 RTN	B7	+50 VDC
A8	(Available)	B8	(Available)
A9	(Available)	B9	(Available)
A10	(Available)	B10	(Available)
A11	(Available)	B11	(Available)
A12	Status 18	B12	(Available)
A13	Status 16	B13	Status 17
A14	Status 14	B14	Status 15
A15	Status 12	B15	Status 13
A16	Status 10	B16	Status 11
A17	Status 8	B17	Status 9
A18	Status 6	B18	Status 7

Table 4-6: Backplane Connector Standard Pinout (Continued)

Contact	Usage	Contact	Usage
A19	Status 4	B19	Status 5
A20	Status 2	B20	Status 3
A21	Status 0	B21	Status 1
A22	Clear*	B22	Thresh
A23	Address 6	B23	Write*
A24	Address 4	B24	Address 5
A25	Address 2	B25	Address 3
A26	Address 0	B26	Address 1
A27	Data 6	B27	Data 7
A28	Data 4	B28	Data 5
A29	Data 2	B29	Data 3
A30	Data 0	B30	Data 1
A31	+5 RTN	B31	+5 RTN
A32	+5 VDC	B32	+5 VDC

Note: "Available" denotes a contact which has no standard, bus-wide usage. It may be dedicated for use between specific connectors. "Thresh" is reserved for the threshold indicator output of the AM slideback function.

Table 4-7: Backplane Connector-Specific Pinout

Contact	Starting Connector	Ending Connector	Usage
A8	J2	J6	Wideband Enable*
B8	--	--	(Unused)
A9	J2	J6	Band 3 Enable*
B9	J6	J8	80 kHz BW Enable*
A10	J6	J8	300 kHz BW Enable*
B10	J6	J8	1 MHz BW Enable*
A11	J6	J8	4 MHz BW Enable*
B11	J6	J8	15 MHz BW Enable*
B12	J5	J6	Band 1/2 Enable

Note: In the above table entries, a trace is placed on the backplane which connects the indicated contact on the "starting" connector, the "ending" connector, and all connectors in between. The "wideband enable*" and "band 3 enable*" traces are also delivered to J1, the microwave module power and control header.

Table 4-8: Backplane Status Line Usage

Contact	Signal	Usage
A21	Status 0	Combined Synthesizer Lock
B21	Status 1	Combined Front End Overload
A20	Status 2	Combined Back End Overload
B20	Status 3	Front End Underload
A19	Status 4	(Spare)
B19	Status 5	Video Overload
A18	Status 6	DCIF Overload
B18	Status 7	21.4 MHz IF Overload
A17	Status 8	RF Overload
B17	Status 9	Prog MW Synthesizer Lock
A16	Status 10	2 GHz Synthesizer Lock
B16	Status 11	530 MHz Mixer Loop Lock
A15	Status 12	LF Prog Synthesizer Lock
B15	Status 13	LF Mixer Loop Lock
A14	Status 14	21.4 MHz Synthesizer Lock
B14	Status 15	DCIF Filter Clock Lock
A13	Status 16	(Spare)
B13	Status 17	(Spare)
A12	Status 18	(Spare)

4.8 Control Section

The control section administers the operation of the receiver. Taking its inputs from the front panel and the IEEE-488 interface, it supplies control signals to the receiver's relays, switches, amplifiers, attenuators, and synthesizers, and status information to the front panel displays, the rear panel status outputs, and again to the IEEE-488 interface. Physically, the control circuitry resides on the processor PCB, the interface PCB, and the switch/display PCB, all located in the front panel assembly. Modules in the cardcage, such as the DCIF and video modules, contain latches and buffers to interface data to and from the control section as well. Figure 4-13 is a block diagram of the control section.

The receiver has three main control modes:

- manual mode, in which all functions are controlled by the front panel.
- remote mode, in which tuned frequency, IF bandwidth, input attenuation, gain, log/linear detector selection, and other functions are controlled by the IEEE-488 interface.
- MDC mode, provided for operation in conjunction with the companion R-1180 microwave down-converter, in which the downconverter's RF input selection, RF input attenuation, and frequency tuning are controlled by the R-110 over the IEEE-488 interface.

In remote mode the remote indicator on the front panel is illuminated. In MDC mode the MDC mode indicator on the front panel is illuminated. The two modes are mutually exclusive, so much so that if one is selected the operator must then manually disable it and enable the other one before the other one will operate.

A block diagram of the control section is shown in figure 4-13.

4.8.1 Switch/Display PCB (A2A1)

The switch/display PCB (A2A1) is attached directly to the back of the receiver's front panel, using standoffs. All of the radio's pushbuttons, displays, and indicators are directly connected to this PCB. The frequency tuning and IF gain controls are connected to it as well, via pigtails.

The tuning and gain controls are quadrature optical shaft encoders attached to the front panel and connected to the switch/display PCB with 4-conductor ribbon cables (J1, J2). Each control requires four connections in order to operate. Two of these are +5 Volts and ground. The other two are the encoder outputs, and the relationship in which pulses occur on them determines the direction of rotation of the shaft. The encoder produces about 200 pulses on each line per rotation of the shaft. These occur 90 degrees out of phase from one another, so that if one is used as a trigger then the other may be used as a directional indicator, since it will be high for rotation in one direction and low for rotation in the other. The two signal lines from each encoder are delivered to the interface PCB (A2A2) for processing.

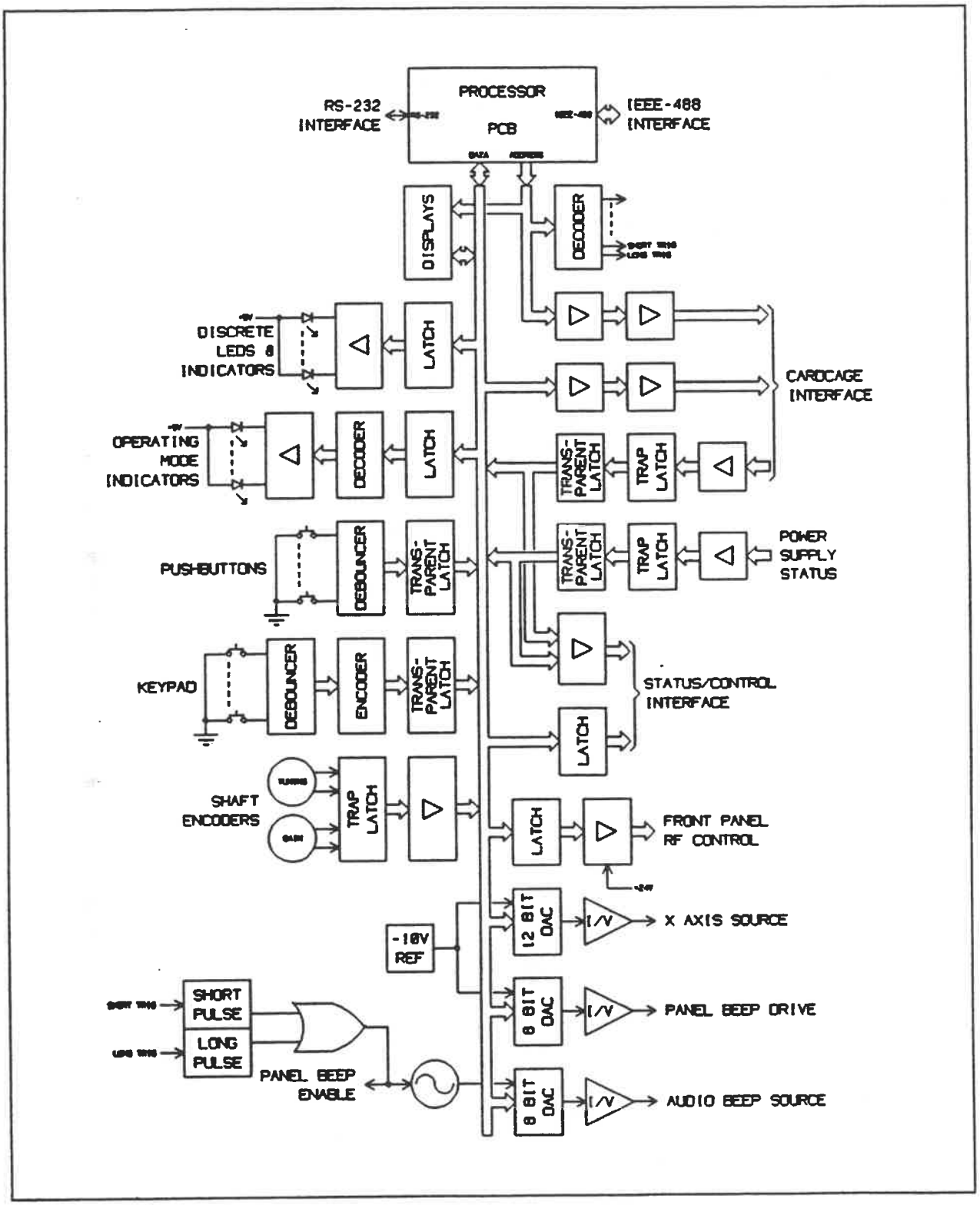


Figure 4-13: Control Section Block Diagram

Indicators consist of single LEDs mounted within some of the pushbuttons (S1, S2, S7 - S9, S14 - S16, S32, S34), and rectangular LED lightbars above and below the general-purpose alphanumeric displays (DS7 - DS34). Displays are scanned LED matrices, packaged four per module (DS1 - DS6). All are mounted directly on the PCB, along with the pushbuttons (S1 - S11, S14 - S32, S34). Each LED indicator and lightbar is driven separately by the interface PCB, through high-current bus driver ICs (U1, U2, U4 - U6). Note however that the operating mode lightbars (the row below the tuning display) are mutually exclusive in use and are therefore driven through a decade decoder (U3), so that only one of them may be illuminated at any given time. A four bit code is delivered from the interface PCB to control the decoder, and the coding is shown in table 4-9. The display modules are "intelligent" and are driven using data, address, and control buses from the interface PCB. The pushbuttons are single-pole, single-throw components with one side connected to ground. A signal line from the other side of each is delivered to the interface PCB. The front panel audible indicator (SP1), a piezo transducer, is also provided. It too is controlled from the interface PCB, through a switching transistor (Q1).

Table 4-9: Operating Mode Indicator Codes

Code	Indicator
0	"TUNE"
1	"START"
2	"STOP"
3	"STEP"
4	"RATE"
5	"SCAN"
6	"STORE"
7	"RECALL"
8	"GPIB"
9	"REMOTE"

Each of the alpha displays provides four characters. The characters are made up of rectangular 5 x 7 matrices of LEDs, which are scanned automatically in two dimensions by the IC to produce the desired ASCII character. This scanning, combined with the fact that 840 individual LEDs are being driven, results in a significant and highly modulated current draw. Filtering in the form of capacitors (C1, C8, C17 et al) and an inductor (L1) are provided in order to keep as much of this as possible off of the supply and ground lines. In addition, the alpha displays use separate +5 Volt and ground planes, isolated from those used by the rest of the PCB and supplied by separate wiring from the power supply. Finally, conductive filter screens are embedded in the display windows on the front panel to limit radiation from the radio. The brightness of the displays is settable to 0%, 25%, 50%, or 100%, so if necessary the amount of display noise may be reduced in special testing situations by turning off the displays for the duration of the test. Since brightness is set by varying the duty cycle of the scanning within the displays, only the full-off setting will effectively reduce the noise. The scanning frequency is generated internally by one of the displays (DS1) and is sent from there to the other five.

The switch/display PCB mates with the interface PCB using 50 and 60 pin headers (P1, P2).

4.8.2 Interface PCB (A2A2)

The function of the interface PCB (A2A2) is to connect the intelligence of the processor PCB (A2A3) to the front panel controls and indicators, the cardcage hardware, and the rear panel status/control connector. The two main external interfaces, the IEEE-488 and the RS-232, reside directly on the processor PCB. One additional function of the interface PCB is to provide the source signal for the X axis output. The interface with the processor PCB consists of power and a control bus. The bus has eight bidirectional data lines, eight unidirectional address lines, and separate read, write, and clear lines. An interrupt request line is also provided in the interface, but is currently unused.

All of the front panel's pushbuttons, indicators, and displays are mounted on the switch/display PCB (A2A1), and the frequency tuning and IF gain control shaft encoders are connected to it. Signals from the pushbuttons and shaft encoders are returned as discrete lines. Signals destined for the LEDs mounted inside the pushbuttons and lightbars are also delivered as discrete signals, except that those destined for the mode indication lightbars (located below the tuning display on the front panel) are delivered as a four bit code, to be decoded on the switch/display PCB. The tuning, attenuation, gain, and bandwidth displays are made up of intelligent ICs, which have data, address, and control lines delivered to them by the interface PCB.

The front panel's pushbutton switches are single-pole, single-throw parts with one side connected to ground. Inputs from these switches must be debounced, which is provided for by ICs (U20, U27, U29, U35, U37, U39) which act as shift registers. Data from a switch is shifted and all stages inside are compared to one another. When all are in the same state it is judged that the switch has attained a stable state and that state is presented at the output. The debouncers generate their own shift clock, set by an external capacitor (C23, C39, C42, C49, C52, C55). Data from the debouncers which service the keypad pushbuttons ("0" - "9", "H", "K", "M", "C", ".") are encoded by a pair of octal priority encoders (U33, U41), whose outputs are gated together (U31) to form a single four-bit code. The priority and code for each pushbutton is shown in table 4-10. When a particular keypad pushbutton is pressed, all those of lower priority are locked out, while each of those of higher priority is able to supercede the one being pressed if it too is pressed. If no button is pressed then the lowest priority input takes over. The code produced is the complement of the priority of the highest priority button being pushed. This scheme was chosen for its static nature (no scanning clock required) and low parts count rather than for any advantage to the prioritization of the pushbuttons.

Table 4-10: Keypad Key Codes

Key	Priority	Code
None	0 (low)	15
"0"	1	14
"1"	2	13
"2"	3	12
"3"	4	11
"4"	5	10
"5"	6	9
"6"	7	8
"7"	8	7
"8"	9	6
"9"	10	5
"."	11	4
"H"	12	3
"K"	13	2
"M"	14	1
"C"	15 (high)	0

The code from the keypad encoder, plus the debounced signals from the other pushbuttons which aren't encoded, are routed to the interface PCB's internal data bus via tristate buffers (U19, U26, U38).

Each of the two shaft encoders on the front panel, when rotated, produces two pulse trains in quadrature, the phase relationship between the two depending upon the direction of rotation. This can be interpreted as a trigger line and a direction line. Two flip-flops (U15, U16) are used for each encoder to sense rotation and direction. Both flip-flops are clocked by the trigger line. One is always set high to indicate that a trigger has occurred, while the other latches the state of the direction line at the time the trigger occurs. All four of the resulting latch lines are routed to the data bus through tristate drivers (U17). When the data is read over the bus the driver is enabled with a strobe line. The end of the strobe pulse is used to generate a clear pulse for the four latches. The reset pulse is generated by setting a flip-flop (U18) and then using its output to immediately reset it, delayed through a gate (U31). This readys the latches for the next trigger from the shaft encoders.

Latches on the data bus (U18, U21, U22, U30, U32) store data which controls the front panel discrete LEDs and lightbars. One set of lightbars, those used to indicate the current operating mode of the radio (the row located below the tuning display on the front panel) are mutually exclusive, so that only one may be illuminated at a time. A decoder is provided on the switch/display PCB to ensure this, so our latch here supplies the decoder with a four bit code. Control signals for the LEDs and lightbars pass through current drivers on the switch/display PCB, so no heavy loading is present here.

The tuning, attenuation, gain, and bandwidth displays consist of intelligent modules which provide four characters each. These modules require a bus interface similar to that used internally by the interface PCB. Each IC requires eight data lines, three address lines, a chip select line, a clear line, and read and write strobes. The chip selects are derived as part of the address decoding on the interface PCB, while the rest are connected directly to the interface PCB's internal bus. A character is displayed by sending its ASCII code to the appropriate address. If the eighth data bit is set as well then the "attribute" (such as blinking) for that character is enabled as well. Brightness is settable through one of the addresses as well.

The cardcage backplane bus is an extension of the interface PCB bus. However, the backplane bus data lines are unidirectional (write only) and only seven address lines are provided. Tristate buffers (U6, U28) are placed between the interface PCB bus and the lines leading to the cardcage. These buffers are enabled only when the eighth address bit is low. This effectively dedicates half of the available interface addresses, 00(hex) to 7F(hex), to the cardcage. These lines do not go directly to the cardcage, but pass first through further buffering on the processor PCB.

The backplane bus also provides eighteen discrete status return lines. The standard protocol on these lines is that a high line indicates good status, while a low line indicates bad status. Bad status may be very short-lived, but must still be detected, and so a set of status capture latches (U7 - U14, U46) are provided. There are eighteen independent flip-flops, each of which may be preset by a particular status line going low. Outputs from the flip-flops are routed to the interface PCB's internal bus through tristate buffers (U34, U36, U47). The flip-flops attached to a given buffer are written low at the end of the read strobe for that particular buffer. If the status is still bad, then the preset overrides the write to the flip-flop and it remains set. In addition, the first four status lines are also passed to the rear panel status/control connector through another buffer (U40) without being latched. The more important cardcage status signals have been assigned to these lines (unlock, front end overload, back end overload, and front end underload).

Four discrete status signals are also received from the power supply, although only three are currently used (AC high, AC low, and DC regulation). These are treated like the cardcage status lines, presetting flip-flops (U44, U45) when low, and the outputs of the flip-flops being routed to the data bus through a tristate buffer (U47). These four lines are also passed, unlatched, through a buffer (U40 again) to the rear panel status/control connector.

The ICs which buffer data onto the data bus are actually tranparent latches. While they normally track their inputs, during read strobes they freeze their outputs in order to ensure a stable reading.

Sixteen more lines are passed to the rear panel status/control connector, but these are set by latches (U42, U43) connected to the interface PCB bus. They allow the microprocessor to indicate its internal status, or allow it to control hardware outside the radio without resorting to the IEEE-488 interface.

The two front panel RF input relays, the RF input attenuator, and possibly a future ground loop isolator (GLI), are all controlled by a latch (U24) connected to the interface PCB data bus, through a relay driver (U1) which provides a 24 Volt source for each line. Separate connectors are provided for the input relay (J3), the RF input attenuator (J1), the GLI (J2), and the band select relay (J4). The relay driver and the connectors are provided with a separate ground return, kept independent all the way back to the power supply, for noise isolation. The relays are latching types, so the firmware will only drive them for a short time. The attenuator and GLI are non-latching, and will be driven continuously.

All latches coming off of the data bus are are cleared when the clear line from the processor PCB is strobed. This clear strobe is also passed on to the front panel displays and to the cardcage.

The interface PCB provides the source for the audible indicator function. This function has two destinations: the audible indicator on the switch/display PCB (a piezo transducer) and a mix into the audio output. Both begin the same way but end up being processed differently.

Two indications are possible, a short one and a long one. The duration of each is controlled by a one-shot pulse generator (U23), each triggered by a write strobe at a different address. The outputs of the two one-shots are ORed together (U25) to form an enable for the circuitry which follows. For the front panel transducer the enable signal is buffered by a gate (U25 again) and then drives a transistor switch on the switch/display PCB, which in turn sinks current through the transducer. Meanwhile, the enable also drives a transistor switch (Q2) on the interface PCB, which in turn switches a sine wave oscillator (U48, CR1, CR2, C67, C71, R3 - R6) on and off. The sine wave isn't very clean, but its fundamental is about 1 kHz, at about 1.5 Volts peak-to-peak. The output of the oscillator feeds one reference input of a dual 8-bit multiplying DAC (U49), which sets the amplitude of the signal from zero to full scale, in proportion to the code written into the DAC, from 0 to about 2 Volts peak-to-peak. The output of the DAC is current mode, and is converted back to voltage mode by and op-amp (U48 again). This signal is delivered to the X axis/audio amplifier PCB (A2A4) via a coax connector (J8). The other half of the dual DAC is used to set the amplitude of the front panel transducer. A -10 Volt reference (U51) supplies the reference, while another op-amp (U48 again) converts back to a voltage output. A transistor (Q1) is placed in the feedback loop to provide an adequate supply current for the transducer. The amplitude is again set in proportion to the code written into the DAC (a separate code, at a separate address, from that used for the audio amplitude), from 0 to +10 Volts.

The X axis output signal is also created here. The same -10 Volt reference (U51) feeds the reference of a 12 bit DAC (U50). The output of the DAC is converted to voltage mode by an op-amp (U48 again) and is passed to the X axis/audio amplifier PCB through a coax connector (J7). The signal amplitude is set in proportion to the code written into the DAC, from 0 to +10 Volts. In this case the code must be written in two pieces, first the upper four bits to one address, followed by the lower 8 bits to another. The data from the first write are not applied until the lower bits are written, at which time all twelve are applied simultaneously.

The interface to the processor PCB consists of address decoding to form chip selects and read and write strobes (U2 - U5, U25). Of the 256 addresses available from the 8 address lines, the mapping is implemented as follows:

Address 00(hex) - 7F(hex) = sent to cardcage

Address 80(hex) - AF(hex) = reserved by processor PCB

Address B0(hex) - FF(hex) = used by interface PCB

A detailed map of the R-110's bus addressing is given in Appendix B.

The physical interface to the switch/display PCB consists of two headers (J5, J6). The interface PCB mates directly to the back of it. The physical interface to the processor PCB consists of two more headers (P1, P2). The processor PCB mates directly to the back of the interface PCB.

4.8.3 X Axis Output Buffer

The X axis output from the interface PCB (A2A2) is buffered on the X axis/audio amplifier PCB (A2A4) on its way to the X axis output connector on the front panel. The buffer circuit consists of a one-pole R-C lowpass filter (R8, C18) and an input loading resistor (RX), followed by a unity-gain video buffer (U3). The filter has a corner at about 1.6 kHz and the buffer can drive the 0 to +10 Volt output of the X axis source into 50 Ohms if necessary. The circuit shares the PCB with the audio amplifier circuit. See paragraph 4.5.1 for a description of the power supply connections to this PCB.

4.8.4 Processor PCB (A2A3)

The processor PCB (A1A3) contains an 80C31 microcontroller, static RAM, EPROM, EEPROM, IEEE-488 and RS-232C interfaces, and several peripheral functions. The PCB manages all receiver operations and supports an interface bus for front panel and cardcage sensing, display and control. Figure 4-14 is a block diagram of the processor PCB.

The microprocessor (U7) operates on four address spaces, of which two are internal to itself and two are external. There are about 90 byte-wide internal RAM locations, some of which are addressed as special-purpose registers and some as general-purpose registers. Access to these constitues the first address space. Some of the registers may also be addressed as individual bits. 256 different internal bits may be accessed. This constitutes the second address space. Externally, separate address spaces are provided for instructions and data, with 65536 byte addresses available for each. Data addresses are read/write, while instruction addresses are read only.

The microprocessor currently operates with an 11.0592 MHz clock, based on a crystal (Y1). This clock rate provides a basic instruction cycle of 1.1 microseconds. The external data bus consists of eight address/data lines, eight upper address lines, read and write strobes for the data space, a read strobe for the instruction space, and a strobe for the required external lower address latch (U8).

Reset for the PCB is provided by a reset controller IC (U13). This resets the microprocessor directly on powerup and whenever the +5 Volt supply drops below 4.5 Volts. The microprocessor provides a number of discrete I/O pins, one of which is assigned as a soft reset. It is ORed with the output of the reset controller (U21). The combined reset is routed to the IEEE-488 controller on the processor PCB, and also strobes the clear line on the bus to the interface PCB (A2A2), which sends it in turn to the front panel displays and the cardcage. The reset controller is also connected to a pushbutton switch (S1) which provides a manual reset capability.

The microprocessor contains a serial port function. This becomes an RS-232 interface with the addition of a driver/receiver (U10) and a baud rate generator. One of the microprocessor's internal counter-timers provides the baud rate, using the processor clock as a reference. Discrete microprocessor I/O pins are used for DTR and RTS sensing, and DCD and DSR drive. A standard female DB-25 connector (J4) is provided on the PCB, but in normal use this connector is unavailable to the outside world. It is currently used for service functions only. It is configured as data communications equipment (DCE) so that it may be easily connected to the serial port of a computer.

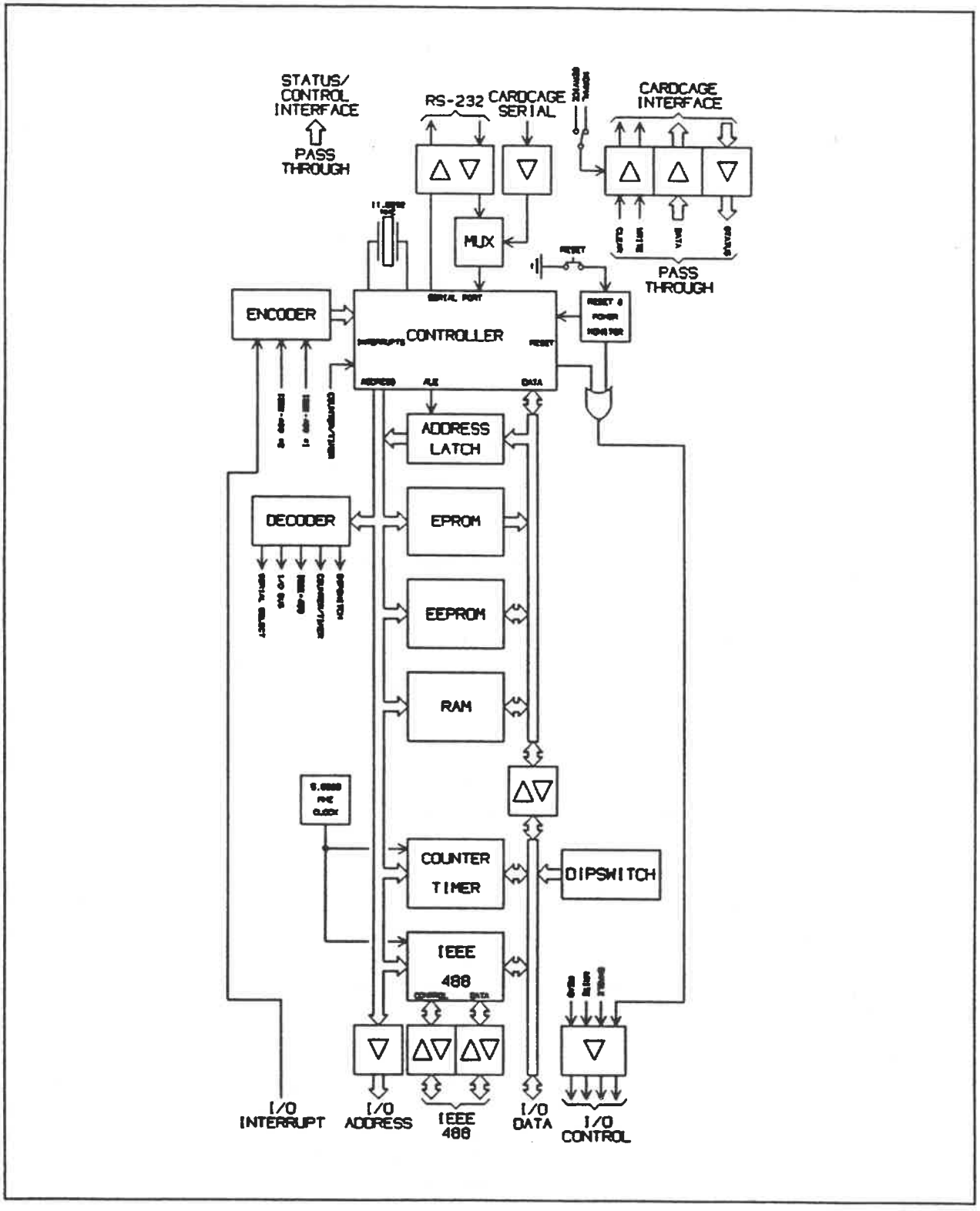


Figure 4-14: Processor PCB Block Diagram

The receive data line of the serial port is provided with a series of gates (U21, U23, U26) which select between the RS-232 driver receiver and a coax connector (J2), passed through a buffer (U6). This is currently unused, but is provided for a future application in which a plug-in module in the cardcage will need to return serial data to the microprocessor. Selection is controlled by a one-bit latch (U22) connected to the data bus.

The microprocessor contains two counter-timers. One is dedicated as the baud rate timebase for the serial port, as mentioned above. The other is used as a time clock, referenced to the microprocessor clock. It produces an internal interrupt about every 80 mS. The interrupt is used to do things (other than scanning) for certain fixed amounts of time, such as strobe the RF input select relay, which is a latching type and doesn't need to be continuously driven.

An external counter-timer IC (U19) is also provided. It is referenced to a separate clock oscillator (U24) running at 5 MHz. Although it contains three separate counter-timer circuits, the IC is dedicated exclusively to scan timing. All three circuits are connected in cascade, with the last output setting a status flip-flop (U22) which sends an interrupt request to the microprocessor. The microprocessor responds by stepping the scan and strobing a write address to clear the flip-flop. This address is shared with the serial port data select flip-flop, so while data isn't important when writing to clear the interrupt request, data must still be written so as to keep the serial select in the proper state.

The microprocessor provides two external interrupt request lines. One is dedicated to the external counter-timer. The other is driven by a priority encoder (U20) which presents an interrupt request and a two-bit code to the microprocessor. Three request lines drive the encoder, two from the IEEE-488 controller and one from the interface PCB. None are currently used.

The IEEE-488 controller (U27) is a TMS9914A, a standard implementation. It uses the 5 MHz oscillator as an operating clock, and standard driver/receivers (U28, U29) to connect it to the external bus. It may be configured as a talker or listener (in remote mode) or as a controller (in MDC mode). The device trigger function, DMA, and service request interrupts are currently unused.

An eight-bit dipswitch (S3) is routed to the interface bus through a tristate buffer (U17). It is currently used to set the IEEE-488 interface address for the radio (factory setting is 16) and the serial port baud rate (factory setting is 1200).

External permanent memory is provided by a 32k x 8 EPROM (U11). This contains the operating instructions for the microprocessor and most of the fixed data tables. It is located in the lower half of the instruction address space. The lower half of the data address space, minus the last 256 bytes, is occupied by a 32k x 8 EEPROM (U14), which, while permanent, may be reprogrammed repeatedly in socket. It contains changeable data tables and provides the nonvolatile storage capability. The upper halves of both memory spaces are combined and shared by a 32k x 8 RAM (U12). This provides volatile data storage, and also, since it is shared between the memory spaces, allows code to be loaded on the fly and then run, as an aid to development, initialization, and service. The remaining 256 bytes of the data space is reserved for I/O functions, for which an interface bus is provided.

Provision is made for future expansion of the operating code. When the code exceeds 32k bytes a larger EPROM will be required. When this happens a 64k part will be adopted. Jumpers (E1 - E9) are provided to accommodate this. It will cause the address map to change, because the upper halves of code and data memory can no longer be shared. It will no longer be possible to download code and execute it on the fly.

The main address decoder consists of gates (U9, U23, U26) which divide the external memory spaces in half and then identifies the last 256 bytes of the first half of the data space for I/O. This circuit is also used to subtract this segment from the memory space of the EEPROM (U14), which would otherwise also be selected.

Secondary address decoding is provided for the peripheral functions. A decoder (U18, U21) maps the on-board peripherals into the I/O space. A detailed hardware memory map is provided in Appendix B, but here is the map for the processor PCB, in short form:

Code Address 0000(hex) - 7FFF(hex) = EPROM (U11)
Code Address 8000(hex) - FFFF(hex) = RAM (U12) (shared)

Data Address 0000(hex) - 7EFF(hex) = EEPROM (U14)
Data Address 7F00(hex) - 7FFF(hex) = I/O (see below)
Data Address 8000(hex) - FFFF(hex) = RAM (U12) (shared)

I/O Address 80(hex) - 83(hex) = dipswitch (S3, U17) (read)
I/O Address 80(hex) - 83(hex) = external counter-timer interrupt clear (U22) (write)
I/O Address 80(hex) - 83(hex) = serial receive data select (U22) (write)
I/O Address 84(hex) - 87(hex) = external counter-timer (U19)
I/O Address 88(hex) - 8F(hex) = IEEE-488 controller (U27)

The dipswitch, external counter-timer interrupt clear, and serial port receive data select are all redundantly mapped -- that is, only one address is required to perform the functions, but they are mapped to four addresses for ease of address decoding. I/O addresses which are not used by the processor PCB -- 00(hex) - 7F(hex) and 90(hex) - FF(hex) -- are available for use by the interface PCB, the front panel displays, and the cardcage.

The I/O bus is taken from the microprocessor bus by passing the data lines through a tristate transceiver (U16), the first eight address lines and the read and write strobes through tristate buffers (U15, U25), and the combined clear line and a bus enable line (developed by the address decoding circuit) through more buffers (U25). The bus enable line also enables the transceiver and tristate buffers, so that the I/O bus is at high impedance (and pulled up) when not in use. This bus is routed to the interface PCB, which in turn routes it to the front panel displays. The link to the cardcage begins at the interface PCB, but must pass back through the processor PCB to get there. This link is completely independent of the other circuitry on the processor PCB, even to the extent of having its own separate power supply and ground return. Buffers (U1 - U3) are hooked to this clean power to act as a data line filter between the control section and the cardcage. Status return lines from the cardcage and the power supply are also buffered (U4 - U6) to provide filtering. These buffers are normally always enabled, but a switch (S2) is provided which will tristate them when they are not actively in use, as a service aid.

The lines running from the interface PCB to the rear panel status/control output connector also pass through the processor PCB, but there is no circuitry involved other than traces to link the input and output connectors.

4.8.5 IEEE-488 Interface

Following is a general description of the IEEE-488 interface. Descriptions of bus commands are given in Appendix A.

The IEEE-488 interface is a digital data communications interface consisting of eight parallel data lines, eight control lines, and eight ground lines. A double-row 24 pin connector is specified for the interface, along with jackscrew retainers. The complete specification is given by the Institute of Electrical and Electronics Engineers (IEEE) as their specification number 488, copies of which are available from them. There are now two parts to the standard, 488.1 and 488.2. The first part is mostly a hardware and timing specification, while the second part defines various command, query, and response protocols.

The specification defines three sorts of devices which may be connected to the bus. These are controllers, talkers, and listeners, and a particular piece of hardware may be any or all of these. There may be multiple controllers on the bus, but only one may be active at any given time. A protocol is defined whereby active control may be passed from one to another. One of the controllers is considered to be "system controller", meaning that it may regain control of the bus whenever it wants to without resorting to the normal transfer protocol.

The controller assigns other devices on the bus as active talkers or listeners. There may be only one active talker at a time, whereas there may be multiple listeners. The active talker drives the eight bus data lines, and the listeners sense them. The controller may make itself a talker or listener as well.

Three of the control lines act as handshaking for transfers on the data lines. The active talker drives **Data Available** (DAV) and the listeners share control of **Not Ready for Data** (NRFD) and **Not Data Accepted** (NDAC). Each byte transferred across the data lines goes through a handshaking protocol in which the talker signals that data is available and all listeners must acknowledge when they receive it. The speed of the transfer is therefore determined by the response time of the last listener to acknowledge.

There remain five other control lines. These are described as follows:

Attention (ATN): The ATN line is used by the controller to interrupt the currently active talker. When ATN is asserted the talker stops driving the data and DAV lines and everybody waits for the controller to send a command. With ATN asserted the controller can then drive the data and DAV lines and issue commands. Commands are received by all devices on the bus, regardless of their currently assigned state. When the controller stops asserting ATN it also stops driving the data and DAV lines, and any assigned talker can then resume driving them.

Remote Enable (REN): The REN line is driven by the controller in charge and allows devices on the bus to be placed under control of the bus when it is asserted. When the controller stops asserting it, all devices on the bus return to local (manual) control.

Interface Clear (IFC): The IFC line is strobed by the controller in charge when it wants to reset the system to its base state. It acts as a master reset.

End or Identify (EOI): The EOI line is unique in that it is the only line with more than one function. In conjunction with a command state (ATN asserted) it triggers parallel polling. In conjunction with a data state (ATN unasserted) it can be used to indicate the last character of a data string.

Service Request (SRQ): The SRQ line is the only control line other than handshaking that is driven by the bus slave devices rather than the controller. The line is used as an interrupt request and is shared by all devices on the bus not in control. When the controller senses it being asserted it must serially poll the devices on the bus which may be responsible for asserting it. Several devices may assert it simultaneously.

4.8.6 Microprocessor Firmware

The firmware that controls the 80C31 microcontroller consists of two major sections: the monitor and the application code. The monitor acts as a mini-operating system which can converse with an operator over the RS-232 interface and also run the application package. It is resident at the bottom of code memory, so that it contains the first level of interrupt and reset servicing as well. The RS-232 capability is limited to service functions at the present time: if no video terminal is connected, then execution automatically branches to the application code from the monitor on powerup (after some initialization of hardware and storage).

The application code senses the settings of the front panel controls (in local modes), the status from the various sections, and the status of the IEEE-488 and RS-232 interfaces. Based upon these inputs, it determines the operating modes of the receiver and what action needs to be taken. It sends data to the front panel indicators and displays, to the receiver hardware, and to the IEEE-488 interface.

The monitor is structured as a loop which waits for input from the RS-232 interface. When it receives data, it parses it against its list of legal command forms. If no match is found, then it will send an error message and resume the input loop. If the command is successfully parsed, then the monitor will execute the command and then, unless the command causes execution to branch out of the monitor, it will again resume the input loop.

The 80C31 microcontroller delegates specific addresses at the bottom of code memory for reset and interrupt branch locations. These branches are handled automatically by the microprocessor without recourse to the firmware, but firmware must be present at these locations to control the servicing of these functions. Resets are serviced by branching to the monitor startup code, which initializes the microprocessor hardware. Interrupts are handled by branches to specific locations in the application code.

The application code begins by initializing its storage, the front panel hardware state, and the RF section hardware state. It then begins a polling loop which checks various front panel controls, IEEE-488 interface status, RF, IF, video and synthesizer section status, and power supply status. New control values read from the front panel, etc., are compared against stored previous values. Any difference causes a dedicated subroutine to be executed to service the change. Interrupts are briefly enabled in the polling loop between one individual status check and the next. This prevents interrupts from occurring during servicing of differences, since this servicing often uses subroutines and storage that is also used by the interrupt service routines, and these routines are neither recursive nor re-entrant.

Meanwhile, a timeclock (based on an internal timer in the 80C31 and referenced to the microprocessor clock) is continuously running. It requests an interrupt every 80 msec or so, and is used for functions that require real-time delays (scanning excepted). The service routine checks to see what is enabled and which of those need servicing. It calls a separate service routine for each one that needs it. A separate hardware timer is used for scanning. It is programmable to four or more digits of resolution, and is used to request interrupts for updates of the cardcage hardware and the front panel during scans, at the specified step rate.

The application code uses all five of the available memory addressing modes: internal bit, internal byte, internal stack, external code, and external data. Internal bit addresses not dedicated to hardware registers are used for application code flags. Remaining internal RAM is divided between stack space and most-often-used or time-critical single-byte storage. External instruction memory in part holds the application and monitor code (EPROM), and also tables of fixed data. External data memory holds the I/O map, nonvolatile read/write storage (EEPROM), and volatile read/write storage (RAM). The I/O map provides a firmware connection to hardware other than RAM, EPROM and EEPROM located outside of the 80C31. Nonvolatile read/write storage holds the calibration tables and data, and nonvolatile state storage. Volatile memory holds the working data and storage that can't fit into the internal RAM of the microprocessor, and also the volatile state storage. In addition, since upper external instruction and data space is shared, code can be loaded into RAM and run as well.

The firmware is written in assembly language for the 80C31 microcontroller, using a number of macros to effectively extend the instruction set. While the assembler and linker allow for relocation of modules, at the present time all object code is ORGed to absolute addresses.

4.9 Power Supply

The power supply section has been designed to provide regulated DC power for the receiver electronics while minimizing conducted and radiated interference. The supply uses extensive shielding and filtering, toroidal magnetics, and special mechanical construction techniques to reduce emissions and to control susceptibility. Figure 4-15 is a block diagram of the power supply.

The power supply is part of the rear panel assembly of the receiver, and consists of a housing containing an input power receptacle, fuses, and EMI filters, a toroidal power transformer, line voltage selection switches, a cooling fan, and a PCB including rectifiers, filter capacitors, linear regulators mounted on heat-sink sub-assemblys, voltage monitors, and the DC output connector. The fuses interrupt the line power if the receiver is connected to an improper voltage or if internal malfunctions occur. Monitor circuits on the rectifier/regulator PCB check the line and the power supply outputs for out-of-tolerance conditions, driving indicators on the front panel and providing status signals for the IEEE-488 interface and the rear panel's status/control output connector.

Functionally, the power supply consists of three main parts: the unregulated supply, the regulated supply, and the voltage monitors. The DC voltages available from the regulated supply are shown in table 4-11.

Table 4-11: Power Supply Output Connector Pinout

Output Name	Power Supply Connector Pin	Destination(s)
+5 VDC	15	Cardcage, Front Panel Buffer
+5 RTN	16	Cardcage, Front Panel Buffer
Front Panel +5 VDC	1	Front Panel Logic
Front Panel +5 RTN	3	Front Panel Logic
Switch +5 VDC	14	Front Panel Pushbuttons
Switch +5 RTN	16	Front Panel Pushbuttons
+8 VDC	12	Cardcage
+/-8 RTN	25	Cardcage
-8 VDC	13	Cardcage
+15 VDC	11	Cardcage, Front Panel Audio
+/-15 RTN	23	Cardcage, Front Panel Audio
-15 VDC	24	Cardcage, Front Panel Audio
Front Panel +15 VDC	9	Front Panel Logic
Front Panel +/-15 RTN	7	Front Panel Logic
Front Panel -15 VDC	21	Front Panel Logic
Audio Output +15 VDC	10	Front Panel Audio
Audio Output +/-15 RTN	19	Front Panel Audio
Audio Output -15 VDC	22	Front Panel Audio
+24 VDC	6	Front Panel Logic
+24 RTN	8	Front Panel Logic
+50 VDC	18	Cardcage
+50 RTN	20	Cardcage
AC High Status	5	Front Panel Logic
AC Low Status	17	Front Panel Logic
DC Unreg Status	4	Front Panel Logic

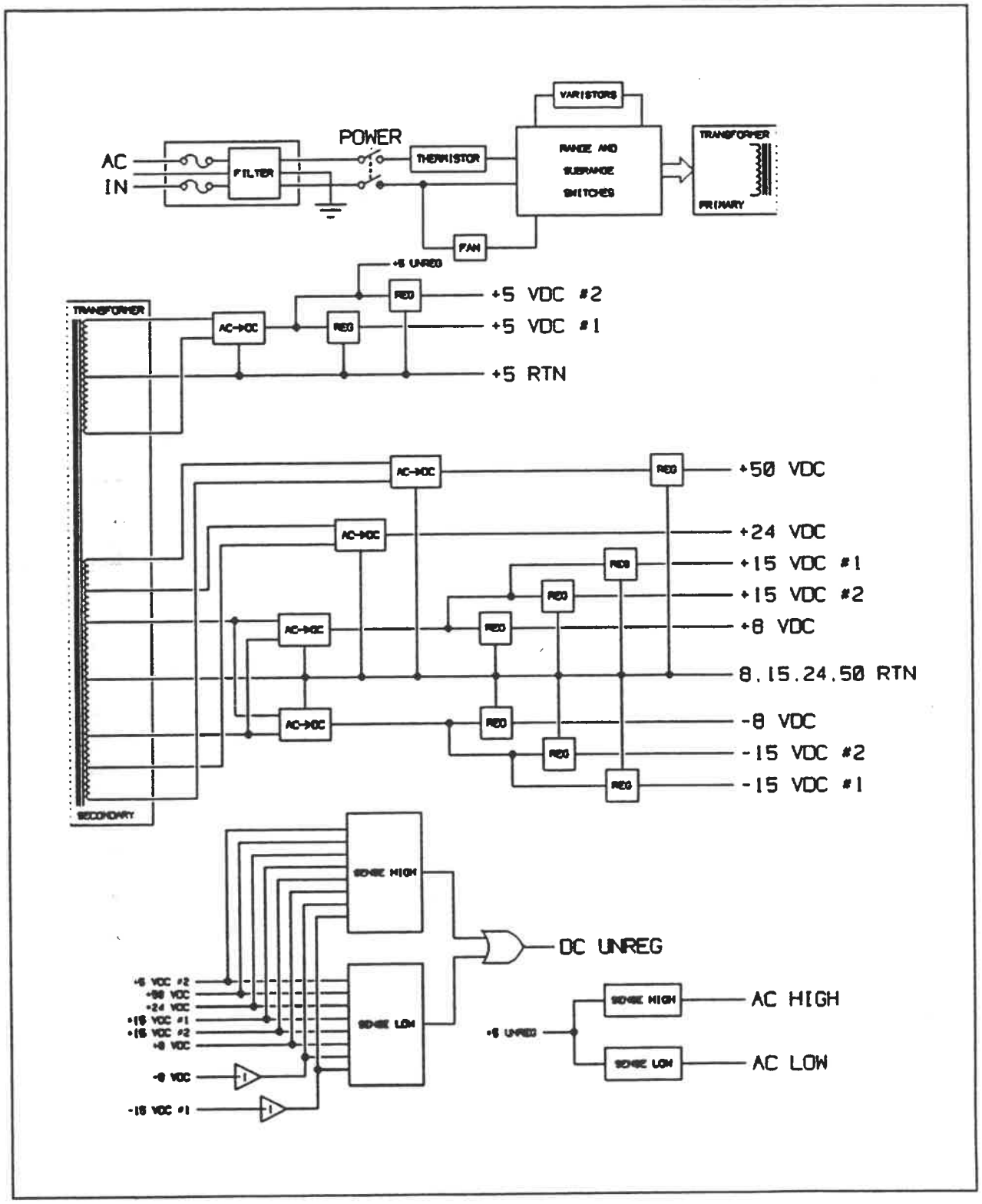


Figure 4-15: Power Supply Block Diagram

4.9.1 Unregulated Supply

The unregulated supply consists of the AC receptacle with fuses and EMI filtering, the inrush limiter, the front panel power switch, the fan, the AC voltage range switches, the line spike suppressors, the power transformer, the rectifiers, and the filter capacitors. Power enters the unit via the line receptacle, which contains the line filters and a pair of fuse holders. One is used for line and one for neutral when connected to 115 VAC; for 230 VAC, one is used for each of the hot lines. The line filter is designed to provide 30 - 50 dB of bidirectional filtering of frequencies in the kHz-MHz range. After passing through the fuses and EMI filter, the AC is routed to the front panel power switch. For 115 VAC operation, both hot and neutral are switched; for 230 VAC, both hot lines are switched. AC from the power switch returns to the rear panel, passes through a thermistor (TM1) to reduce the surge at powerup, and is bypassed with a pair of varistors (VR1, VR2). These devices shunt very short duration spikes, providing line spike protection for the receiver.

The AC then goes to the voltage selection switches. The AC voltage range switch selects either 115 or 230 volt operation by connecting the dual primaries of the power transformer (T1) in parallel or in series, respectively. The AC voltage subrange switch selects one of six line conditions, from well below nominal to well above, by selecting one of six taps on one of the power transformer primaries for service. The fan is connected across the transformer primaries so it always receives 115 VAC no matter whether 115 or 230 VAC is applied to the receiver.

The power transformer has eight secondary windings. Two are used as a center-tapped source for the rectifiers (D10, D11) supplying the +5 VDC regulators. The other six windings are "stacked" to yield a multiple-tapped secondary feeding the rectifiers for the +50 (D2, D3), +24 (D4, D5), and +/-15 VDC (D6 - D9) outputs. The +/-8 VDC outputs are derived from the same rectifiers that feed the +/-15 VDC outputs.

Rectifying and filtering circuits are mounted on the printed circuit board. Discrete rectifiers are connected for full-wave rectification in all circuits. The transformer windings, harness, and circuitry are specially configured to reduce noise caused by high crest-factor currents: each winding on the transformer terminates at the same point (no hybrid connections within the transformer), twisted pairs attach to the terminations, harness geometry is controlled, rectifiers are located close to their power source, diode packs are used to reduce wire length, etc.

4.9.2 Regulated Supply

The regulated portion of the power supply consists of part of the printed circuit board, plus the heat sink assemblies mounted to it. Overall, the PCB contains the rectifiers and filter capacitors of the unregulated supply, regulator components, the AC line-range detectors, and the regulator status monitor.

All regulators except for +24 VDC and +50 VDC are implemented with low-dropout linear integrated circuit devices which operate with minimal headroom; these improve the efficiency of the power supply, cutting both power consumption and power dissipation. The +50 VDC regulator uses a linear integrated circuit regulator as well, but with normal headroom constraints. However, current draw on this output is minimal. Each regulator incorporates short circuit protection and thermal overload protection. The +24 VDC supply is unregulated, but is used only to drive relay coils, an application for which regulation requirements are minimal. Protection is nevertheless provided by a series resistor which will limit the current drawn in case of a short circuit.

All DC outputs except for +24 VDC are fixed in amplitude using precision resistive dividers or fixed-value ICs. No trimming of the output voltages is available.

4.9.3 Power Supply Monitoring

The power supply monitor circuits check for AC line high and low, and regulated output high and low for most of the DC outputs. Most of the checking is done with a pair of power supply monitor ICs (U10, U11). These ICs use timing capacitors (C26 - C31) to allow the ICs to ignore short glitches in the output. A reference is provided in each IC, set to 2.5 VDC. This establishes the undervoltage comparison thresholds for both the regulator and line monitors. An external resistive divider (R32, R36) divides the reference to 1.7 Volts to provide the regulator overvoltage comparison threshold. The voltage sense lines pass through resistive dividers to properly match these thresholds. Monitor functions are as follows.

For line voltage high detection, unregulated +5 VDC is divided (R22, R35) and compared to the reference by the line low sense circuit of one of the monitor ICs (U11). In normal operation the sensed voltage is lower than the reference and therefore a fault status is generated. This status is inverted by a transistor switch (Q1) so that status is now good when the sensed voltage is below the reference. The output of the transistor forms the AC line high status signal and is sent to the front panel logic circuitry for processing and distribution.

For line voltage low detection, unregulated +5 VDC is divided (R20, R33) and compared to a reference by the line low sense circuit of the other monitor IC (U10). In normal operation the sensed voltage is above the reference and therefore no fault condition is generated. The output from the monitor IC forms the AC line low status signal and is sent to the front panel logic circuitry for processing and distribution.

For DC regulation monitoring, both overvoltage and undervoltage conditions are sensed, based on comparison to a reference and a fixed fraction of it. Note that sensing is reversed from what is normally expected, because the undervoltage threshold is higher (2.5 Volts) than the overvoltage threshold (1.7 Volts). What happens is that the monitor internally adds the reference to a quarter of the external threshold comparison voltage, producing an internal overvoltage comparison threshold of 2.925 Volts. Each monitor IC produces both undervoltage and overvoltage status signals; all four signals are combined using open-collector drivers (U12) to form a single regulation status line which is sent to the front panel logic circuitry for processing and distribution.

One IC (U10) monitors the cardcage +/-15 VDC and +/-8 VDC lines, while other (U11) monitors +24 VDC, +50 VDC, cardcage +5 VDC, and front panel +15 VDC (shared by front panel logic and the audio output). This leaves front panel +5 VDC and front panel -15 VDC unmonitored, but the front panel +5 VDC may be omitted because without it the front panel logic will not be able to receive and process the status information anyway. Note that a resistor (R38) is used to further loosen the tolerance on the +24 VDC monitor line.

4.9.4 Power Supply Usage

The power supplies are used by the various modules and assemblies of the radio as shown in table 4-12.

Table 4-12: Power Supply Usage

	+5 #1	+5 #2	+8	-8	+15 #1	-15 #1	+15 #2	-15 #2	+24	+50
Control Section	X	X					X	X	X	
X Axis/Audio Amplifier PCB					X	X	X	X		
Microwave RF Module		X		X	X					
Preselector Module		X			X	X				
Low Frequency RF Module			X	X	X					
21.4 MHz IF Amplifier Module		X	X	X	X	X				
21.4 MHz IF Filter Module			X	X						
Video Module		X	X	X	X	X				
DCIF Module		X	X	X	X	X				
Fixed LO Synthesizer Module		X			X	X				
Low Frequency Synthesizer Module		X			X	X				
Microwave Synthesizer Module		X			X	X				X

4.10 Chassis Wiring

There is very little discrete chassis wiring in the R-110. The most obvious wiring is the coax harness running across the tops of the cardcage plug-in modules. These are shown in the harness diagram (493055) provided in section 6. An additional coax harness (493750, 493755) is provided in the rear panel assembly to connect the rear panel monitor jacks. See the assembly drawing (493700) for placement. The front panel assembly also contains coax cables, both flexible and semi-rigid (493670, 493671). See the assembly drawings (493600, 493607) for placement. Several front panel subassemblies sport pigtails which plug into printed circuit boards. Wiring of a given pigtail is part of the associated subassembly. See the front panel assembly drawings and the schematic (493601) for details.

Three ribbon cables are required. One 37 conductor ribbon links the front panel assembly to the cardcage backplane. A shielded 24 conductor ribbon extends the IEEE-488 interface from the front panel assembly to the rear panel connector. A shielded 25 conductor ribbon links the rear panel status/control output connector to the front panel assembly. All of these are captive to the cardcage assembly. See the assembly drawing (493050) for details.

An eight-wire pigtail (493065) links the microwave RF module (A1A1) to the cardcage backplane. This pigtail plugs in at each end, and is not captive to the cardcage.

The rear panel assembly contains discrete wiring for the AC input module, the range switch, and the fan. A four-wire pigtail is provided for connection of the power switch on the front panel, and a two-wire pigtail is provided for connection of the fan. All DC power comes from a 25 pin D-sub connector on the power supply printed circuit board. See the assembly drawing and schematic (493700, 493701) for details.

Finally, the cardcage is provided with a wiring harness. One part of this harness is a four-wire pigtail which links the front panel power switch to the rear panel assembly. It mates with connectors at both the front and rear panels. The rest of the harness provides DC power distribution for the front panel and the cardcage. A 25 pin D-sub connector brings power from the rear panel assembly, and delivers it to the front panel assembly via 9 pin and 15 pin D-subs. The harness is captive to the cardcage, and is hard-wired to it via feed-through capacitors. Power wiring passes through the feed-throughs and ends at soldered connections to the cardcage backplane. See the assembly drawing and schematic (493050, 493051) for details.

Discrete wiring in the R-110 is color coded, where possible. DC power supply voltages and returns are each given a unique color code. Signal wiring is more limited. See table 4-13.

Table 4-13: Discrete Wire Color Coding

Usage	Color
+5 VDC	Green
+5 RTN	White/Green
+8 VDC	Brown
8 RTN	White/Brown or White/Blue
-8 VDC	Blue
+15 VDC	Red
15 RTN	Gray
-15 VDC	Violet
+24 VDC	Orange
+24 RTN	White/Orange
+50 VDC	Yellow
+50 RTN	White/Yellow
AC (Line)	Black and White Twisted Pair
Signals	White or White/Black
Signal Ground or Non-Specific Ground	Black
Coax	Unspecified

R-110 RECEIVER MANUAL ADDENDUM: WIDEBAND OPTION

1. INTRODUCTION

The wideband option adds three extra bandwidths to the standard selection of the R-110B receiver. To do so it adds a new signal path in a separate cardcage plug-in module and replaces the video module as well.

There are currently two sets of wide bandwidths available: 20 - 40 - 100 MHz, and 40 - 100 - 200 MHz. One or the other may be chosen, but not both.

The wideband option is available for both the R-110 and the R-110B receivers. This document is an addendum to their technical manuals. Excerpts may be added to the user's manuals as applicable.

2. INSTALLATION

Physically, the wideband option consists of a new plug-in module for the receiver's cardcage, plus a replacement for the video module, plus modifications to the cardcage coax cable harness. While installation is not especially complicated, it is normally done at the factory during the original construction of the receiver. Retrofitting of the option in the field is possible, but it is recommended that this only be done by authorized factory field service personnel. In addition to installing the modules, configuration storage in the firmware must be modified, using a controlled-access procedure.

3. USAGE IN MANUAL MODE

The three new bandwidths are added to the selections accessed via the bandwidth up/down pushbuttons on the front panel of the receiver. When the widest standard bandwidth (15 MHz in most receiver configurations) is selected, pressing the "bandwidth up" button will select the first of the wideband filters, and so on. Pressing the "bandwidth down" button will select narrower bandwidths until the standard bandwidths are again selected. The buttons have an "auto-increment" mode, in which a new selection is performed every half second or so if a button is held down.

The wideband option uses a signal path that is separate from most of the receiver circuitry. The signal is taken from the wideband (1450 MHz) IF, and amplified and filtered. The signal returns to the normal signal path at the video detector, which has been upgraded as part of the wideband option to afford a wider bandwidth output. The separate wideband signal path places restrictions on the use of the wideband option, due to the fact that the 21.4 MHz IF is bypassed. This means that:

- Only the first conversion is available for tuning. This means that tuning is in increments of 5 MHz.
- The Band 1 and Band 2 signal paths are unavailable. This means that the minimum legal tuned frequency in wideband mode is 20 MHz.

The receiver protects against illegal conditions by refusing to tune below 20 MHz when wideband is selected, and refusing to select a wide bandwidth when tuned below 20 MHz. When in wideband mode only the tuned frequency of the first conversion is displayed, i.e. a multiple of 5 MHz.

The wideband signal path provides its own, separate programmable gain circuits. Although there are only two of these, as opposed to four in the normal signal path, the manual adjustment range of 50 dB is maintained, and is still set via the front panel gain control knob and display.

AGC is also provided for. Usage is the same as for the narrower bandwidths. The function is selected via the appropriate keypad alternate function.

Front end overload and underload detection circuits are provided, and drive the same cardcage status lines as the detectors in the normal signal path. They are used when auto-attenuation is enabled. With auto-attenuation disabled, a front end overload indication when wideband is enabled may be alleviated by increasing the input attenuation, using the appropriate front panel pushbutton.

A new video circuit is provided with the wideband option that is used for both wide and normal bandwidths. This video circuit accepts inputs from the wideband module, the 21.4 MHz IF module, and the DCIF. While the wideband signal path contains a separate detector, the video module provides an output buffer that is capable of delivering the widest available (200 MHz IF) bandwidth into 50 Ohms. In doing so a compromise was settled upon, in that the maximum video output is 3 Volts, as opposed to the 4 Volts available from the standard video module.

Log detection and BFO are unavailable in wideband. If one of these functions is selected at the same time that a wide bandwidth is selected, then the indicator associated with that function will blink. The Z axis output is available. The pulse stretch and slideback options, if present, are operational in wideband mode as well.

In summary, significant effort has been made to make manual control and monitoring of the wideband signal path as similar as possible to that of the normal signal path. The main differences, as mentioned above, are the restricted tuning range and resolution, the reduced maximum video output amplitude, and the lack of some video functions.

4. USAGE WITH IEEE-488 AND PROPRIETARY EXTERNAL INTERFACES

The IEEE-488 interface allows an external host computer to command and monitor the receiver's operation. The proprietary external interface allows receiver cardcage status plus the output of the DVM option to be transmitted to the host computer more quickly than is possible over the IEEE-488 interface. It nevertheless must operate in conjunction with the IEEE-488 interface since it is unidirectional (transmit only).

The IEEE-488 interface in the R-110 receiver has been designed to be compliant with the requirements of IEEE-488.2, which describes communications protocol, defines a number of "standard" commands and queries, and requires that many features that were options in IEEE-488.1 be present.

The standard and proprietary commands and queries supported by the basic R-110 receiver, and the R-110B, are given in their respective technical manuals. Those pertaining to the wideband option will be reviewed here.

The normal bandwidth commands and queries are extended when the wideband option is present. Wide bandwidths may be commanded in the same manner as normal bandwidths, e.g. <BW 100E6>. If the standard query is issued when a wide bandwidth is selected, the response will be in the standard format, e.g. <100E6>. The wide bandwidths are added to the list returned in reponse to the <BW? ALL> query.

The same restrictions apply here as in manual tuning: the tuning range is limited to 20 MHz on the low side, and tuning is limited to multiples of 5 MHz. A tuning command containing a frequency that is not a multiple of 5 MHz will be rounded to the nearest legal value. A tuning command containing a frequency below 20 MHz will be rejected.

The proprietary interface outputs buffered overload, underload, and lock status signals, along with DVM data if that option is present. The front end overload and underload signals are taken from the wideband signal path when a wide bandwidth is selected, and from the 21.4 MHz IF otherwise.

5. THEORY OF OPERATION

The hardware that is unique to the wideband option consists of the wideband filter module and the wideband video module. The operation of those two modules will be described here. Descriptions of the rest of the signal path and the supporting hardware, such as synthesizers, the controller, and the power supply, are described in the R-110 and R-110B technical manuals.

The signal feeding the wideband filter module is taken from the microwave module at the output of the first mixer, using a solid state switch. Only one stage of amplification has been provided in front of the mixer, so the signal level at this point is typically very low. The result of the first conversion is an IF frequency of 1450 MHz. No filtering is performed on the signal from the mixer output before passing it to the wideband filter module.

5.1. Wideband Filter Module Operation

The input signal from the microwave module is first given three stages of amplification, increasing the signal level by about 23 dB. Overload / underload conditions are sensed here, using a coupling consisting of a PCB trace laying parallel to the trace containing the main signal. Overload and underload conditioning will be described later. The main signal is then distributed to one of three IF filters, using solid state switches. Unlike the 21.4 MHz IF filters, these are not daisy-chained. Instead, only one filter is selected at a time. Depending on which option has been ordered, these filters can be 20, 40, and 100 MHz, or 40, 100, and 200 MHz. The outputs of the two wider filters are padded to reduce their amplitude, in accordance with the gain scheme that maintains noise amplitude constant over all bandwidths. This means that the amplitude of a given filter output must be reduced by the square root of its ratio to the bandwidth of the next narrower filter. These filters not only set the IF bandwidth, they also act to isolate the 1450 MHz IF signal from the variety of signals produced by the mixer in the microwave module.

Just as the signal was sent to a particular filter using solid state switches, the output of the selected filter is obtained by a second set of switches. The signal from the selected filter is passed through a voltage controlled attenuator, and from there is delivered to a set of four more gain stages. The control for the variable attenuator is supplied by a D/A converter, described later. The attenuator has a range of about 25 dB.

The output of the second set of gain stages is passed through a filter with a bandwidth of 200 MHz, to reduce out-of-band noise. The signal is then passed through a second variable attenuator, also controlled by a D/A converter. The output of the attenuator feeds four more gain stages through a coupling that again consists of a trace laying parallel to the signal trace. The tap signal from the coupling is sent to the IF output when wideband is enabled, using a solid state switch to select between it and the 21.4 MHz IF output. The signal level delivered to the IF output is a function of input signal level the input attenuation setting, selected bandwidth, and the IF gain setting. The maximum gain is about 15 dB.

The output of the set of four gain stages is padded lightly to set the signal level to approximately +6 dBm with -52 dBm at the module input. This signal feeds the wideband detector, which consists of two more gain stages driving a pair of diodes, followed by a buffer amplifier to ensure sufficiently high impedance at the diodes. The gain of this amplifier is less than unity because it is limited to about 1 Volt output at the necessary bandwidth, while the diodes need to be driven as strongly as possible in order to maximize the instantaneous dynamic range. The output of the buffer amplifier is sent to the wideband video module.

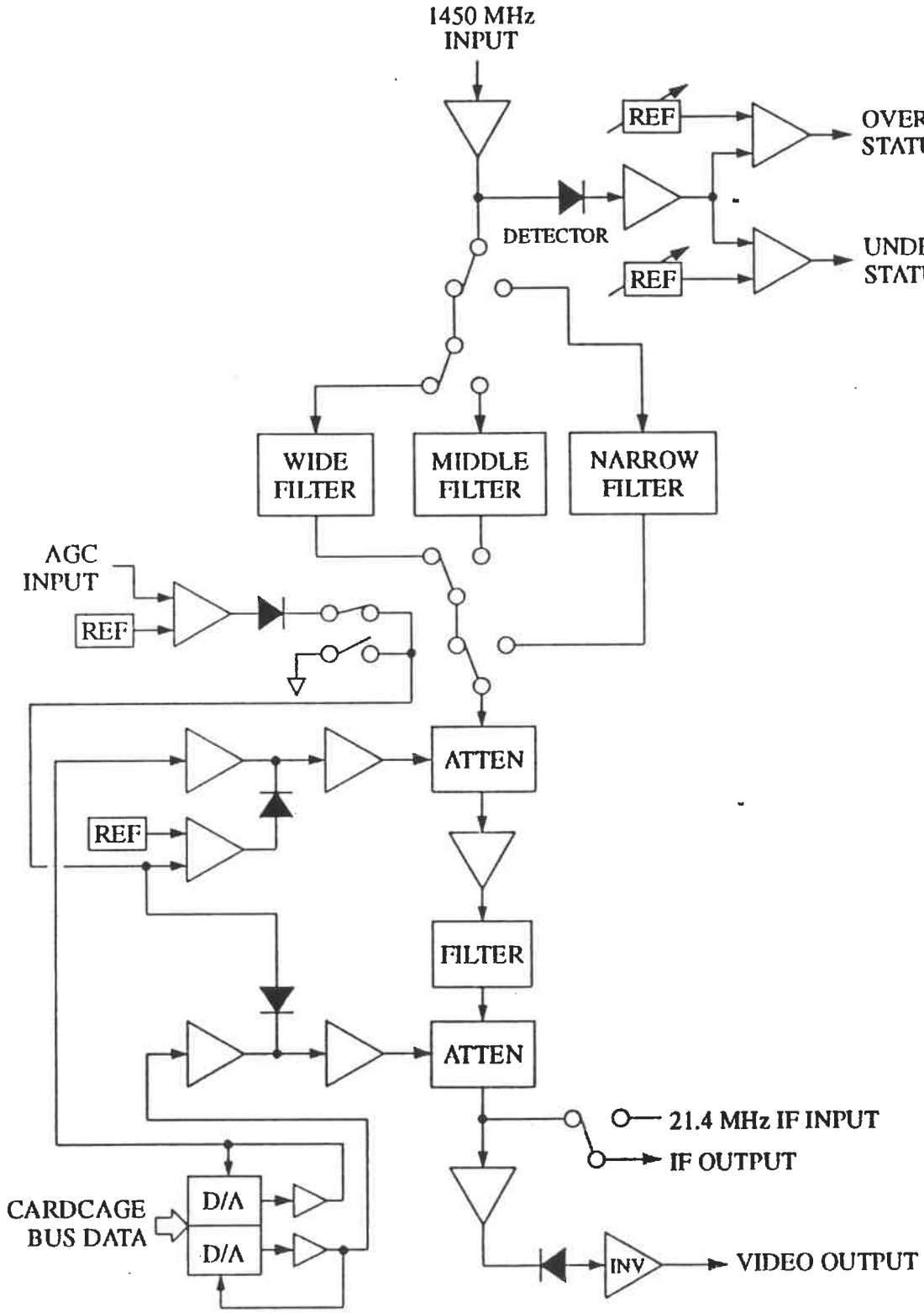


Figure 1: Wideband Filter Module Block Diagram

The overload / underload pickoff is peak detected with a diode and a low-pass filter, and is then buffered by an opamp. The amplifier output is fed to individual comparators for overload and underload, the references for which are set by trimpots, based on a reference that provides temperature correction by means of a diode and an opamp buffer. The comparator outputs are gated with an enable signal, and finally control individual drivers that are set up to provide a high-impedance output to the cardcage status lines (which are supplied with pullup resistors) when status is "good", and to provide a low-driven output when status is "bad". Overload status is applied to cardcage bus STAT1, and underload status is applied to cardcage bus STAT3, both of which are shared with similar status signals supplied by the 21.4 MHz IF. The 21.4 MHz IF will not be enabled when the wideband option is in use, and vice versa.

Intelligent gain control is provided by a double 12 bit D/A converter IC, which is connected to the cardcage control bus. Since this is an 8 bit bus, four addresses are used to load data into holding registers in the IC, plus a fifth address to apply all of it to the outputs simultaneously. The D/A converter IC outputs are current mode, so a pair of opamps are used to convert to voltage mode, as required by the attenuators. Note that the attenuators are not perfectly linear, so that the firmware maintains individual and unique calibration tables for each of them. One of the procedures required when initially configuring a receiver or when replacing the wideband filter module is to connect the receiver to an IEEE-488 interface-based system and run an automated calibration program on the host computer. This updates the calibration tables for the attenuators and provides gain control accuracy that is nominally within 1 dB of the front panel display for "regular" signals. A +10V precision reference is inverted by an opamp to provide a stable reference voltage for the D/A converters.

Automatic gain control (AGC) is provided by a circuit that takes its input from the video signal, buffers and peak-detects it, and combines it into the signals from the D/A converter outputs. This is somewhat complicated, involving several stages of selectable gain and offset tweaking, depending upon whether or not AGC is enabled. Diodes couple the AGC voltage into the gain control signals, so that the AGC is only effective when the attenuation required is greater than that set by the D/A converters. When operating with AGC enabled, the front panel gain control is normally left set to maximum, to give the AGC circuit its maximum control range. The AGC signal to the first attenuator is delayed from that to the second, to avoid degrading the noise figure.

As described above, filter selection is performed by solid state switches, with only one filter selected at a time. Control of these switches is provided by a latch connected to the cardcage control bus. Latched control bits drive comparators, which output the required (non-TTL) control voltages for the switches. The same latch also supplies control bits for wideband and overall module enable.

5.2. Wideband Video Module Operation

The wideband video module performs the same functions as the standard video module, with increased bandwidth for those functions that involve the wideband signal path. The log detector, 21.4 MHz linear detector, and BFO are essentially duplicates of the circuitry on the standard module. The video and Z axis amplifiers are different. Additional connectors are provided for wideband inputs and outputs.

There are four signal inputs to the wideband video module: one from the wideband filter module, two from the 21.4 MHz IF, and one from the DCIF module. The 21.4 MHz IF is tapped in two different places, once for AM and BFO detection and once for log detection, so that the gain distribution will work out correctly in each case. The requirements for each are different because the log detector has over 70 dB of dynamic range while the linear detector has only a little more than 30 dB. The BFO uses the same input as the AM detector because here the available dynamic range is not a consideration.

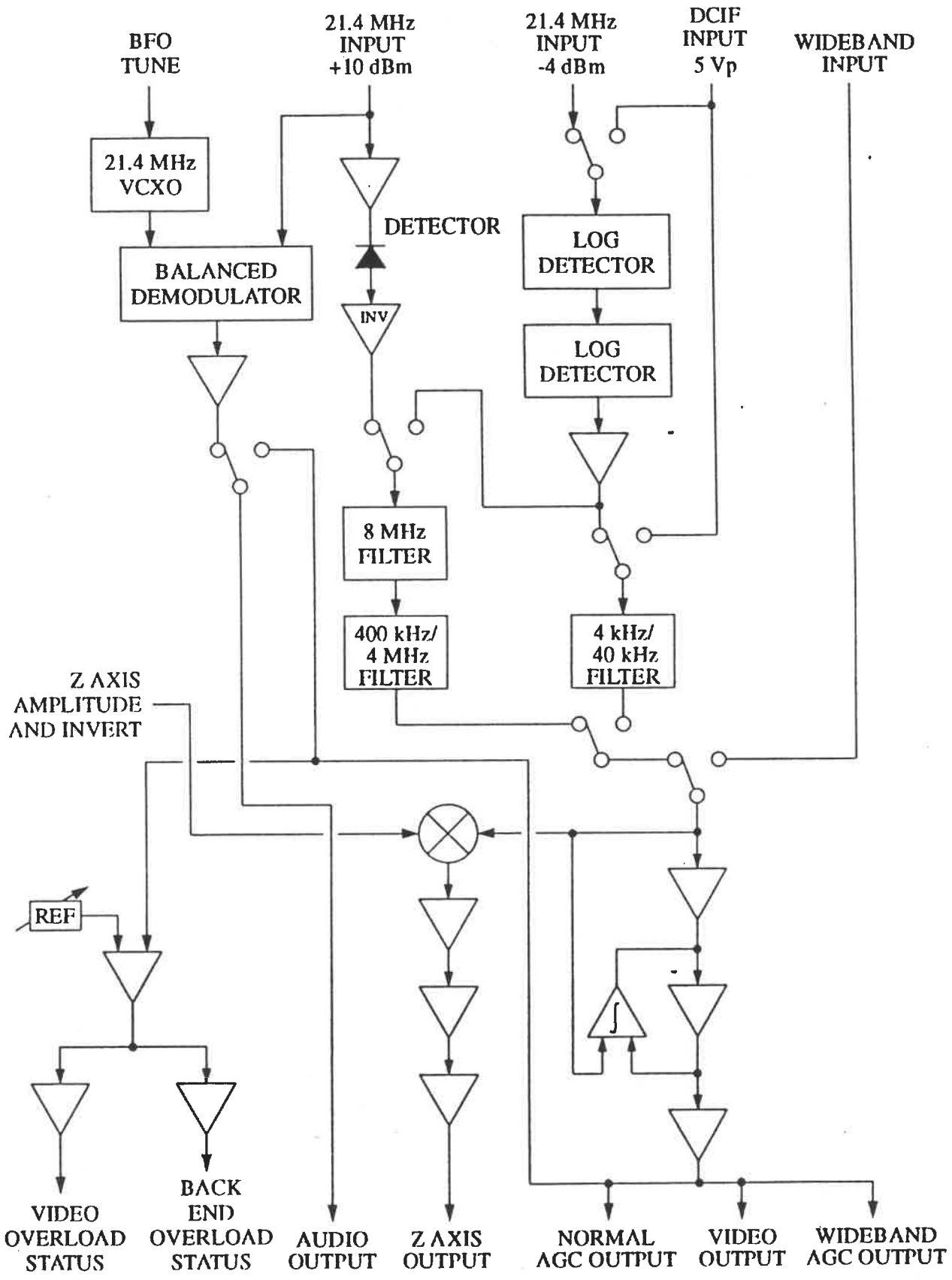


Figure 1: Wideband Video Module Block Diagram

The 21.4 MHz IF input destined for wideband AM detection arrives at at a maximum level of +10 dBm and is routed to the detector circuit throught a pad and an AC coupling. The pad is selected to place the full-scale value of the input at the detector overload threshold. While the detector itself is basically a diode, dynamic range is maximized by placing the diode behind a tuned amplifier which steps the signal level up to a point where the effect of the turn-on characteristic of the diode is minimized. The tuned amplifier is based on a transistor and a low-Q tuned network. The diode is followed by an opamp, to maintain the impedance at the detector diode and to provide thermal compensation. The gain of the opamp is trimmed during test to establish end-to-end gain. A second transistor acts as a switch to disable the detector when it is not in use. The detector is followed by a carrier-removal filter that consists of a series of L-C low-pass filters, totalling 8 poles with a corner at 8 MHz. This filter is also used by the log detector.

End-to-end gain of the 21.4 MHz AM detector is 10 dB, so that a +10 dBm input will produce a full-scale output of 0 - 3 Volts peak. Dynamic range at full scale output is at least 30 dB.

The output of the filter provides the input for a second, selectable video noise filter. This filter is a one-pole low-pass R-C configuration, in which any combination of two capacitors may be selected by the firmware. In actual usage only one (or none) of these is selected at a time, however. The corners are at 400 kHz and 4 MHz. Selection is based on the selected 21.4 MHz IF bandwidth. Table 1 shows the correlation between IF bandwidth and the selected video filter, including the filters in the DCIF video signal path (described below).

The input for the log detector can come from one of two places, either from the other 21.4 MHz IF input (the one that doesn't supply the AM detector) or from the DCIF. Selection is made by a relay under the control of the firmware. A termination resistor is switched onto the 21.4 MHz IF input when it is not in use. Furthermore, the input from the DCIF may be switched around the log detector, bypassing it, when a linear characteristic is desired. When routed through the log detector, the DCIF signal, even through it arrives already detected and carrier-filtered, is given the same log-compression gain characteristic as the detected signal from the 21.4 MHz IF.

The log detector consists of a pair of log amplifier/detectors, which output in current mode, followed by a linear amplifier, which provides a voltage output. The IF signal from the input is fed in series from the first log amp to the second, while their detected video outputs are summed at the voltage amplifier. An input offset adjustment is provided to null the output of the log amps. A resistor is selected during module test to set the full scale output level at the output of the voltage amplifier. The voltage amplifer output is sent along two paths. One path is to the same 8-pole carrier removal filter used by the 21.4 MHz AM detector, selected by a relay under firmware control. The other path is through another relay that selects between this and the raw DCIF input, again under firmware control. The signal that is selected by the relay is passed through another video filter, which provides a fixed corner at 40 kHz and a selectable corner at 4 kHz. The outputs of this and the other video filter are now recombined into a single path, using another relay, again under firmware control. This signal is padded and delivered to yet another relay, that selects between it and the input from the wideband filter module. This signal, then, is delivered to the video and Z axis amplifiers.

Gain of the log detector is such that at full scale, every 10 dB coming in will produce 375 mV at the video output. Dynamic range at full scale is in excess of 70 dB. The front end of the log detector has a bandwidth of 120 MHz, much greater than the 8 MHz maximum bandwidth of the carrier removal and video filters that follow.

The BFO detector consists of a 21.4 MHz Clapp oscillator based on a crystal and driven by a transistor, fine-tuned by a varactor diode. An on/off switch is provided by a FET switch, which disables the oscillator by removing power from it. Tuning frequency control is provided by a potentiometer on the receiver front panel. A constant current source based on a FET drives the front panel control, developing a voltage which varies linearly with its setting while requiring only one "hot" line and a return running off of the module. The voltage derived from the control setting is used to tune the varactor. A trimmer on the module is used to set the center frequency, while a variable inductor is used to set the adjustment range.

The oscillator drives a mixer, the other input of which is the same tap of the 21.4 MHz IF used by the AM detector. The difference output generated by the mixer is offset from baseband by an amount determined by the front panel control setting, whthin a range of +/- 4 kHz. The output of the mixer is filtered to remove unmixed and summed products, and is amplified by an opamp. The output of this amplifier is sent to the audio output when enabled, routed by a FET switch under firmware control. For a full-scale input of +10 dBm, the output will be 1.6 Volts peak-to-peak. Dynamic range is not a consideration because the BFO is used for detection of CW signals

Table 1: Video Noise Filter Selection

Bandwidth Range	Filter Corner
200 Hz - 2 kHz	4 kHz
2.5 kHz - 20 kHz	40 kHz
50 kHz - 200 kHz	400 kHz
300 kHz - 2 MHz	4 MHz
4 MHz - 15 MHz	None

The video amplifier is upgraded in the wideband video module. It consists of three stages, plus a DC servo amplifier. The first two stages provide gain, with the first stage providing most of it because the second, while it can provide high output levels, is limited in its maximum gain capability. The final stage is a unity gain buffer that drives the video output on the front panel of the receiver through a resistor that sets the source impedance to 50 Ohms. It also feeds the 21.4 MHz IF and wideband filter module AGC inputs, the audio output (through a FET switch that selects between the video output and the BFO output), and the video overload detector. The maximum available output is 3 Volts peak, and the maximum bandwidth is about 100 MHz.. The DC servo amplifier is looped around the second stage amplifier, acting as an integrator that compares the input to the output and generates a correction voltage to yield zero DC output. Trimpots are provided to pre-correct the offset for both the wideband and 21.4 MHz IF / DCIF inputs. The appropriate trimpot voltage is selected by means of FET switches.

The Z axis amplifier is also upgraded in the wideband video module. It consists of an analog multiplier followed by a current-to-voltage converter, followed by an amplifier stage and an output buffer stage. The analog multiplier is used for gain control and signal inversion. A constant current source based on a FET drives a potentiometer on the front panel of the receiver. The pot setting therefore establishes the voltage drop across it, requiring only a hot line and a return, which can be configured as a coax cable to minimize noise pickup. The voltage is buffered by an opamp and selectively inverted by a FET switch in conjunction with another amplifier, under firmware control. The FET switch sets the gain of the amplifier to +/-1 by supplying signal to both differential inputs (gain = +1) or grounding the positive input (gain = -1). The output of this amplifier provides the control voltage for a four-quadrant multiplier that processes the video signal accordingly. The output of the multiplier is in differential current mode, and is converted to single-ended voltage mode by an opamp. The next stage adds gain and generates a large output signal range. The final stage is a unity-gain buffer followed by a resistor that sets the source impedance to 50 Ohms. The output capability of this circuit is again 3 Volts peak at 100 MHz bandwidth.

The overload detector consists of a high-speed comparator that measures the video output against a reference set by a trimpot. The output is inverted by a transistor that provides a faster slew rate and also extends narrow pulses. The transistor output controls a pair of drivers that drive two of the cardcage bus status lines. The drivers are configured to have high-impedance outputs when status is "good" (the cardcage bus status lines are supplied with pullup resistors to make this state float high), and low-driven outputs when status is "bad". This allows multiple drivers to be connected to a single status line, with any one of them able to report "bad" status. The two cardcage bus status lines used here are STAT2 (back end overload) and STAT7 (video module overload). Currently each of these two lines is used only by the video module.

The cardcage bus control interface consists of address decoding and a pair of latches. The latches provide control for video filter selection, DCIF / 21.4 MHz IF / wideband input selection, log detector selection, BFO selection, and Z axis selection and inversion control.

6. MAINTENANCE AND FIELD SERVICE ADJUSTMENTS

Preventative maintenance for the wideband option hardware is the same as for the rest of the receiver. Hardware calibration may be required periodically, or when a module is replaced. Field service adjustments are described in the following paragraphs.

6.1. Wideband Filter Module Field Service Adjustments

The wideband filter module provides just two field service adjustments, these being the overload and underload thresholds. In order to have access to the adjustment components, the module must be raised above the cardcage using a cardcage bus extender and coax cable extensions.

6.1.1. Overload Threshold Adjustment

Procedure:

1. Remove the coax cable from module connector J1 and connect a microwave signal generator. Apply a CW signal at 1450 MHz and -3 dBm.
2. Select 40 MHz bandwidth.
3.) Adjust trimpot R39 so that the front overload indicator on the front panel of the receiver just comes on.

6.1.2. Underload Threshold Adjustment

Procedure:

1. Use the same signal generator hookup as the foregoing procedure Reduce the amplitude to -16 dBm.
2. Monitor connector P1 (the cardcage bus connector) pin B20 with a voltmeter.
3. Adjust trimpot R41 so that the voltage on pin B20 just switches from near +5V to near 0V.

6.2. Wideband Video Module Field Service Adjustments

The wideband video module provides many of the same adjustments as the standard video module, since it uses many of the same circuits. In order to have access to the adjustment components, the module must be raised above the cardcage using a cardcage bus extender and coax cable extensions.

6.2.1. Log Detector Null Adjustment

Procedure:

1. With no signal applied and the coax cable removed from J2, monitor U3 pin 6 with a voltmeter.
2. Select log detection on the front panel of the receiver. Select a bandwidth that is not wideband.
3. Adjust trimpot R22 for minimum voltage at U3 pin 6.
4. Disable log detection. Reconnect the cable to J2.

6.2.2. BFO Center Frequency Adjustment

Procedure:

1. Remove the coax cable from module connector J1 and connect a signal generator. Set the signal generator to CW at 21.4 MHz, -10 dBm.
2. Select BFO on the front panel of the receiver, with a compatible bandwidth (e.g. 1 MHz).
3. Monitor U28 Pin 6 with an oscilloscope.
4. Adjust trimpot R106 so that the beat frequency indicated on the oscilloscope with the BFO control on the receiver's front panel fully counterclockwise is the same as the beat frequency indicated with the control fully clockwise. Make sure that there is a null in between.
5. Restore the coax cable connection to J1.

6.2.3. Video Amplifier Offset Adjustments

Procedure:

1. With no signal applied, set the receiver gain control to minimum.
2. Select a DCIF bandwidth (e.g. 20 kHz) on the front panel of the receiver.
3. Monitor J8 with a voltmeter.
4. Adjust trimpot R65 for minimum output WITHOUT EVER LETTING THE VOLTAGE AT J8 GO NEGATIVE.
5. Select a wide bandwidth (e.g. 100 MHz) on the front panel of the receiver.
6. Adjust trimpot R64 for minimum output at J8 WITHOUT EVER LETTING THE VOLTAGE AT J8 GO NEGATIVE.

6.2.4. Z Axis Amplifier Offset Adjustment

Procedure:

1. With no signal applied, set the receiver gain to minimum.
2. Select a wide bandwidth (e.g. 100 MHz) and enable the Z axis function, no inversion, on the front panel of the receiver.
3. Monitor J10 with a voltmeter.
4. Adjust trimpot R154 for minimum output WITHOUT EVER LETTING THE VOLTAGE AT J10 GO NEGATIVE.

6.2.5. Z Axis Amplifier Multiplier Null Adjustment

This adjustment is occasionally necessary, but requires a fairly complicated test setup. If this adjustment must be performed, contact the factory for a suggested procedure with available test equipment.

6.2.6. Overload Threshold Adjustment

Procedure:

1. Remove the coax cable from module connector J3 and apply 5.25 VDC.
2. Select a bandwidth of 20 kHz to select J3 as the module input.
3. Adjust trimpot R96 so that the back overload indicator on the front panel of the receiver just comes on.

7. CONTROL INTERFACE

The control interface for the wideband module consists of six contiguous write-only ports mapped into the microcontroller's external read/write memory space. The first four addresses are for the gain control DACs, the fifth is a strobe to load the DAC, and the sixth loads a control latch.

Address 60H = DAC A low byte:

Bits 0 - 7 = DAC A bits 0 - 7

Address 61H = DAC A high nibble:

Bits 0 - 3 = DAC A bits 8 - 11

Bits 4 - 7 = spare

Address 62H = DAC B low byte:

Bits 0 - 7 = DAC B bits 0 - 7

Address 63H = DAC B high nibble:

Bits 0 - 3 = DAC B bits 8 - 11

Bits 4 - 7 = spare

Address 64H = DAC load strobe

Bits 0 - 7 = unused

Address 65H = control latch:

Bit 0 = BW #1 enable (the narrowest)

Bit 1 = BW #2 enable (the middle one)

Bit 2 = BW #3 enable (the widest)

Bits 3 - 5 = spare

Bit 6 = wideband AGC enable

Bit 7 = wideband module enable

The control interface for the wideband video module is very similar to that for the standard video module, consisting of two control latches mapped into two contiguous microcontroller external read/write memory addresses.

Address 7E = control latch #1:

Bit 0 = 4 MHz video filter enable

Bit 1 = 400 kHz video filter enable

Bit 2 = unused

Bit 3 = 4 kHz video filter enable

Bit 4 = DCIF / 21.4 MHz IF log detector input select:

0 = DCIF

1 = 21.4 MHz IF

Bit 5 = Log / Lin select:

0 = linear detection

1 = log detection

Bit 6 = medium bandwidth / narrow bandwidth video select:

0 = medium bandwidth

1 = narrow bandwidth

Bit 7 = spare

Address 7F = control latch #2:

Bit 0 = BFO enable

Bit 1 = Z axis enable

Bit 2 = Z axis invert

Bit 3 = wideband enable

0 = 21.4 MHz IF

1 = wideband

Bits 4 - 7 = spare

R-110B TECHNICAL MANUAL ADDENDUM: DVM DISPLAY OPTION

1. INTRODUCTION

The R-110B DVM display option works in conjunction with the basic DVM option to allow front panel control of the DVM options, and also to provide a front panel display of measured signal levels. While the basic DVM option is available for both the R-110 and R-110B receivers, the DVM display option is available for the R-110B only. Without the display option the basic DVM option operates in conjunction with the IEEE-488 interface only.

This document is an addendum to the R-110B technical manual covering the DVM display option only. A separate addendum is provided with the basic DVM option, covering its installation, usage with the IEEE-488 interface, and theory of operation.

2. INSTALLATION

The hardware for the DVM display option consists of a front panel pushbutton and display assembly that replaces the one normally supplied with the receiver. Note that this is the third different display assembly, since the display assembly in the non-optioned R-110B is also different from the one in the original R-110.

It is recommended that installation of the the DVM display option display assembly be done as part of the original assembly of the receiver, or that it be retrofitted only by factory field service personnel. Although the installation of this assembly is in no way different from the installation of the normal display assembly, the procedure for opening and closing the front panel assembly is somewhat complex, and it is easy for wires to become pinched in several places during re-assembly.

Once the new assembly has been installed the standard firmware configuration routine must be run to ensure that the firmware is aware of the new assembly. It is possible to autodetect the presence of the assembly, and the firmware does this on powerup, but the configuration store should be updated nevertheless.

3. USAGE

The R-110B front panel provides support for the DVM display option, whether or not the option is actually present, in the form of the "DVM" alternate keypad function. This is the alternate function of the "M" key, selected by pressing the black "Alt" key followed by pressing the "M" key. If the DVM display option is not present then the tuning display will read "Unavailable!". If it is present then a number of parameters may be set using the tuning display select pushbuttons (the three pushbuttons located directly below the tuning display).

If AM mode is selected then the DVM menu selections, obtained by means of the left and right select pushbuttons, are DVM off, DVM peak video, peak-and-hold input coupling, and peak-and-hold sample time. If FM mode is selected then there is only DVM off and FM deviation. Switching the FM demodulators in and out using the appropriate front panel pushbutton will result in both DVM hardware settings and display menu selections changing as well.

3.1. Peak-and-Hold Input Coupling

The peak-detect-and-hold circuit receives its input from the video output of the receiver. It captures peak amplitudes of that signal, including impulses as short as 5 nanoseconds, and holds the value for subsequent A/D conversion. Both the input coupling and the accumulation time of this circuit may be set. DC input coupling allows the circuit to sample both the carrier and any AM modulation present, while AC coupling will eliminate the carrier component, which is represented as a DC voltage, leaving only the modulation. With the AC/DC coupling message showing on the tuning display, the selection may be toggled by means of the center select pushbutton. Readings may take a second or two to stabilize after toggling the selection.

3.2. Peak-and-Hold Sample Time

The accumulation time in the peak-detect-and-hold circuit can be set to values between about 10 usec and 10 sec. The timebase that does this consists of a counter based on a 1.2288 MHz clock, so the accumulation time is set as a number of counts at about 814 nsec each. The firmware accepts time settings in microseconds, milliseconds, and seconds, and automatically determines the best timebase count to provide the desired setting.

With the sample time shown on the tuning display, a new value may be entered using the numeric keypad. The new value is entered in decimal, followed by the "H" key to indicate microseconds, the "K" key to indicate milliseconds, and the "M" key to indicate seconds. Any value from 10 usec to 10 sec is acceptable. The "C" key may be used during the entry to recover the old setting.

3.3. The Display

All of the foregoing selections and settings have used the tuning display. The DVM display itself, which is what is provided by the DVM display option, consists of an extra row of displays above the attenuation, gain, and bandwidth displays. Slightly smaller displays were used in this window (relative to the standard displays) in order to accommodate the new function.

Although provisions have been made for a full row of up to 16 characters, at present only the middle two sockets (8 characters) are filled, and not all of the characters are driven by the firmware. The displays for the existing functions (attenuation, gain, and bandwidth) operate normally.

3.4. Initialization and Storage of Settings

DVM settings are stored as part of the overall setting records used in initialization, temporary, and permanent storage. This means that, firstly, the DVM and display options will be initialized on powerup and reset to the settings held in the initialization store. This store may be modified by the user. Likewise, when using the temporary and permanent stores, DVM settings are stored and recalled along with many other receiver parameters.

3.5. Usage in AM

When AM demodulation is selected (the default in the absence of FM), the peak-detect-and-hold circuit is in use and both of its settings become significant. To set up the DVM display in this mode first press the black "Alt" key so that its LED is illuminated, and then press the keypad "M" key to bring the DVM setup indications to the tuning display. The parameter to be displayed is selected by pressing the left or right select pushbutton repeatedly until the desired message appears.

With "DVM Off" displayed, the DVM display may be enabled by pressing any of the three select pushbuttons. The center button is in fact a "default select" button for most menu selections. Here the default is "enabled".

With "Peak Video" displayed, normal DVM AM operation is in progress.

With "AC coupling" or "DC coupling" displayed, the selection may be toggled by pressing the center select pushbutton. This is an exception to the normal "select default" function of the center button.

With the sample time displayed, the sample time may be changed by entering it on the keypad in decimal, followed by the "H" key to indicate microseconds, the "K" key to indicate milliseconds, or the "M" key to indicate seconds. If the entry is out of range then the nearest legal value will be substituted.

AM video is 0 - 4 Volts in a standard receiver and 0 - 3 Volts in a receiver equipped with the wideband option. This is conditioned by the peak-detect-and-hold circuit to the 0 - 5 Volt range of the A/D converter itself. The firmware then displays the A/D count as a decimal range of 0 - 9.99

3.6. Usage in FM

When the FM option is present and the FM demodulator is selected the function of the DVM display changes from an indication of video amplitude to an indication of FM deviation. The FM option hardware contains a special circuit to generate this signal. The A/D converter accepts its 0 - 5 Volt range and converts it, whereupon the firmware displays the results as a signed decimal number from -9.99 to +9.99. An indication of 0 represents perfect tuning to the received signal, while a negative indication represents tuning too low and a positive indication represents tuning too high.

When FM demodulation is selected the DVM selections on the tuning display are limited to two: on and off. Any of the three select pushbuttons can be used to enable the DVM display, while either the left or right pushbuttion may be used to disable it.

3.7. Usage in Remote

In remote mode the DVM display continues to indicate AM video or FM deviation, except that instead of controlling sampling and conversion automatically, in remote mode the receiver will sample and convert only when commanded to do so by the IEEE-488 interface, and will therefore not display new data until the receiver is commanded to take it. A free-run command is available over the IEEE-488 interface as well.

4. THEORY OF OPERATION

The new pushbutton and display assembly that comprises the DVM display option hardware is very similar to the assembly used in the standard R-110B. The only major difference is that the three four-character displays used by the standard R-110B assembly are replaced by sockets for up to seven smaller four-character displays. The new displays have a different interface characteristic than the old displays, which allows them to be identified automatically by the firmware on powerup. Basically, the older displays are more elaborate, featuring a read/write interface allowing the characters loaded into them to be read back for verification. The new displays are write-only. This means that if an attempt to read back a character from an address allocated to an older display fails, then the new displays must be present. This characteristic is used for autodetection on powerup.

Another difference between the displays is that the older displays have internal blinking and brightness controls. Four levels of brightness are supported. The new displays require that brightness control be provided externally, via an enable pin that requires pulse-width modulation. Added circuitry has been provided in the form of an oscillator and a monostable multivibrator with a controllable pulse width. A control latch is used to set the oscillator on and off and set the pulse width to 25%, 50%, or 100%. None of the seven new displays are required to blink in the current revision of firmware, so a blinking control is not provided.

Note that more addresses are needed for the seven new displays versus the three old ones, even though the old displays required eight addresses apiece whereas the new ones only require four. Extra decoded chip selects are brought onto the new assembly from the front panel interface assembly to support the new displays.

Although sockets have been provided for seven four-character displays, only five are currently in use. The sockets in the upper corners are left vacant.

5. SERVICE INFORMATION

Removal and replacement of the DVM display assembly uses the same procedure as that for the standard display assembly, as described in the R-110B technical manual. As stated above, it is recommended that only the factory or factory field service personnel perform this operation.

There are no adjustments on the DVM display assembly.

6. INTERFACE SUMMARY

The interface to the front panel display assembly containing the DVM display is the same as for the normal display assembly except for the attenuation, bandwidth, and gain displays, the DVM display itself, and the brightness control latch. Pushbuttons, lightbars, the tuning display, the shaft encoders, and the panel beeper are all identical for both assemblies (in fact, all except the tuning displays have their data bus interfaces on the interface assembly, anyway). Only the new addressing will be given here. A complete list of the old addressing may be found in the R-110B technical manual.

Address D8:	Attenuation display	character 0 (righthand)
Address D9:		character 1
Address DA:		character 2
Address DB:		character 3 (lefthand)
Address E0:	Gain display	character 0 (righthand)
Address E1:		character 1
Address E2:		character 2
Address E3:		character 3 (lefthand)
Address E8:	Bandwidth display	character 0 (righthand)
Address E9:		character 1
Address EA:		character 2
Address EB:		character 3 (lefthand)

Address F0:	DVM display	character 0 (vacant) (righthand)
Address F1:		character 1 (vacant)
Address F2:		character 2 (vacant)
Address F3:		character 3 (vacant)
Address F8:		character 4
Address F9:		character 5
Address FA:		character 6
Address FB:		character 7
Address A0:		character 8
Address A1:		character 9
Address A2:		character 10
Address A3:		character 11
Address A8:		character 12 (vacant)
Address A9:		character 13 (vacant)
Address AA:		character 14 (vacant)
Address AB:		character 15 (vacant) (leftmost)

Address BE: Brightness latch:

Bits 0 - 2 = Brightness code:

000 = off

001 = off

010 = full

011 = 25%

100 = off

101 = off

110 = full

111 = 50%

Bits 3 - 7 = (unused)

R-110B RECEIVER TECHNICAL MANUAL ADDENDUM -- PULSE STRETCH AND SLIDEBACK OPTIONS

1. INTRODUCTION

The R-110 and R-110B receivers support a pulse stretch and slideback option in which the receiver's AM video output is processed to extend short pulses and is also gated at a settable reference for signal strength measurements and noise removal. The option physically shares space on a cardcage plug-in module with the DVM option, and shares its cardcage bus interface.

The slideback option supplements the DVM option in that while the DVM option provides a continuous relative indication of signal strength, the slideback option can be used with an external signal generator to provide, with somewhat more effort, an accurate absolute indication of signal strength. Use of the DVM option with an external host computer containing calibration tables, such as is provided in the DSI-110 system, can provide the function of the slideback option in an automated and much more elaborate form.

2. INSTALLATION

Installation of the pulse stretch and slideback option is normally performed at the factory as part of the configuration of a new receiver. It may in some cases also be retrofitted by field service personnel at the costomer's site. Installations requiring a firmware upgrade are more complicated, since the front panel assembly of the receiver must be opened up and the processor assembly removed to gain access to the firmware EPROM.

Once installed, the receiver must be informed that the option is present via the standard configuration routine in firmware.

Retrofitting of a receiver by the factory or by authorized field service personnel is highly recommended.

3. USAGE

The pulse stretch and slideback functions are each provided with separate selection switches and adjustment controls on the front panel of the receiver. In addition, the slideback function is provided with a lightbar indicator in the tuning display. The video output of the circuit is taken to the front panel as the auxiliary output. In the R-110 receiver it replaces the X axis output.

The pulse stretch function acts to extend the decay of narrow pulses without affecting their peak amplitudes. The minimum pulse width that can be captured by the circuit is about 5 nanoseconds, while the stretch range is about 12 nanoseconds to 1.5 milliseconds. The enable switch contains an internal LED which illuminates when the function is enabled.

Typical usage of the pulse stretch function is to enable it and adjust the control so that narrow, wide-spaced pulses can be seen on an oscilloscope connected to the auxiliary video output, without extending them so much that they overlap.

The slideback function provides a settable DC level which is used as a thresold for the receiver's AM video signal. In effect the video output has this DC level subtracted from it, without ever going below zero. The enable switch contains an internal LED which illuminates when the function is enabled. The level is set with the front panel control. When the signal strength is greater than the set level, the "THRESH" lightbar in the front panel tuning display illuminates.

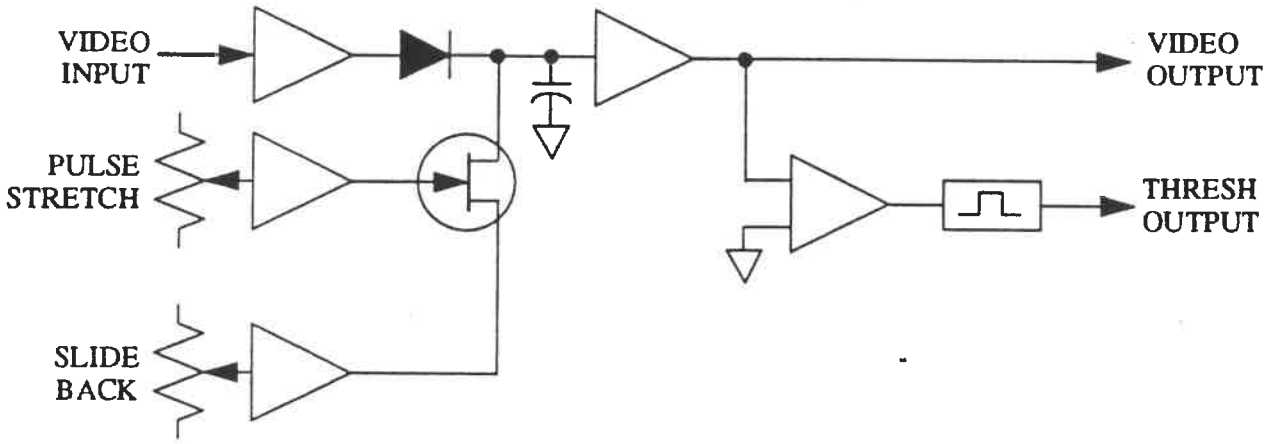
Typical usage of the slideback function for signal strength measurements consists of the following steps:

- Connect a signal of interest to the receiver's input #1
- Connect a signal generator to input #2

- Tune the receiver to the signal of interest and set the attenuation, gain, and bandwidth for optimum reception
- Enable slideback and adjust the slideback control so that the "THRESH" lightbar just barely illuminates
- Switch the receiver's input to the signal generator, set the signal generator's frequency to the tuned frequency of the receiver, and adjust the signal generator's output amplitude so that the "THRESH" lightbar again just barely illuminates
- Read the signal strength from the signal generators output meter or dial.

As mentioned previously, the DSI-110 automated receiving system automates this function using an A/D converter and a host computer with stored calibration tables.

Both pulse stretch and slideback are intended to be manual functions only. Both are disabled when the receiver is in remote (IEEE-488 control) mode.



4. THEORY OF OPERATION

The pulse stretch and slideback functions are combined in a single circuit block. In addition there is a supplementary video amplifier and a cardcage bus interface that is shared with the DVM option. The following description is based on schematic 493741, Rev X3.

The cardcage bus interface consists of a data bus buffer U17, address decoders U18 and U19, data latch U9, and status line driver U20A. Although all eight data bus lines are latched by U9, only bits 6 and 7 are used by the pulse stretch and slideback functions. Bit 6 enables pulse stretch and bit 7 enables slideback. The latch is cleared on powerup and reset so that the functions always initialize disabled. Then, when the processor initializes, it reads the initialization record in EEPROM and sets all of the hardware, including the pulse stretch and slideback enables if the initialization record indicates that they should be enabled.

The address decoders provide several address strobes to the module, but only one is used by the pulse stretch and slideback option, that being address 6D for the latch. Note that the other latch bits (bits 0 - 5) are used by the DVM option. The pulse stretch and slideback enables are inverted to the proper logic state by a pair of analog switches (U42C and U42D) that would have been spare otherwise.

The pulse stretch control is located on the front panel, and is connected to the module via coax cable, arriving on connector J8. The value of the front panel control and the feed resistor (R69) are carefully selected to provide a nonlinear output characteristic which acts to linearize the pulse stretch control FET (Q2). This voltage from the wiper is amplified, level-shifted, and buffered by amplifier U40B and connected to the rest of the circuit through enable switch U42B, which is an analog switch controlled by bit 6 of the control latch. The control voltage splits into two paths here. One path, through adjustment potentiometer R62 and an adjustable current source consisting of amplifier U41A and transistor Q4, controls the pulse stretch FET by generating a voltage across resistor R45. Since this node floats with changes in slideback level, a current source is required to control it. The other path, through diode string CR11 - CR14 and amplifier U40A, serves to reduce bias on diode CR8 for large amounts of stretching. The actual stretching is produced by the video signal, buffered by amplifier U34, charging capacitor C111 through diode CR8. The capacitor discharges through FET Q2, at a rate controlled by the aforementioned circuitry. It discharges into the slideback circuitry, which acts as a threshold gate. The greater the amount of pulse stretching, the less Q2 conducts, so that for lots of stretching Q2 is almost turned off, so that bias on diode CR8 must be reduced to keep the DC baseline from shifting, as mentioned above. The voltage on the capacitor is buffered by U35 and sent to the slideback indicator control circuit and also to the auxiliary video output on the front panel through connector J7. The signal path to the front panel is capable of passing the full 100 MHz bandwidth of the wideband option.

The slideback control on the front panel is log taper potentiometer, brought back to the module on coax through connector J9. Since only two wires are provided, a constant current source is provided by Q3 to generate the proper log characteristic output. Zener diode CR15 is provided to keep the output from rising to the positive supply rail when the front panel control is disconnected, as this would damage the output buffer. The voltage from the control is passed through enable switch U42A, which is an analog switch controlled by bit 7 of the control latch. The voltage is buffered by U41B and applied to the low side of pulse stretch FET U2. The result of this is that diode CR8 doesn't forward bias until it exceeds the slideback level, effectively subtracting all signal levels below this threshold from the output. The level can be adjusted from 0 to about 2.8 Volts to match a video range of 0 to 3 Volts.

The processed video signal is buffered by U35 and sent to the front panel auxiliary video connector, as mentioned above. Note that the slideback level appears as a DC offset on the output. The signal also feeds the indicator circuit. This consists of amplifier U38, followed by comparator U45, followed by pulse generator U20A. The signal is AC-coupled by capacitors C122 and C128, so that the comparator is set to always look for signal levels above zero Volts. The pulse generator produces a positive pulse with a minimum of several milliseconds duration every time the signal level exceeds the slideback level, to ensure that the condition will be visible on the front panel indicator. This is the "THRESH" indicator, located in the top right of the tuning display. Note that this indicator is the only one whose operation is totally independent of the control processor (except insofar as the control processor can disable the slideback function entirely).

The supplementary video amplifier, consisting of U30, U31, and related components, is provided to make up for the additional loading required by the option circuits. Gain of U30 is two so that U31 can drive a source resistance of 50 Ohms and have the output still come out unity. Note that this amplifier is compatible with the wideband option and can accept signals of up to 3 Volts and 100 MHz.

5. SERVICE AND ADJUSTMENTS

There are four adjustments in the pulse stretch, slideback, and supplementary video amplifier circuitry. None need to be readjusted frequently, but may perhaps need to be verified at intervals of several years. Making the adjustments requires the use of a signal generator, a pulse generator, a voltmeter, and an oscilloscope, plus familiarity with the procedure for removing the outer case from the receiver. The procedure for removing the case is given in the R-110 and R-110B technical manuals.

5.1. Maximum Pulse Stretch Adjustment

This adjustment is provided by trimpot R62. Connect a pulse generator to the input of the receiver and set it up so that it produces narrow pulses (1 usec or less) at a repetition rate of about 100 Hz. Then tune the receiver so that the pulses appear on the video output. Monitor the auxiliary video output with an oscilloscope, enable pulse stretch and rotate the front panel control fully clockwise, and adjust R62 so that the pulses are 1.5 milliseconds long at the point at which they decay to 10% of their peak value.

5.2. Maximum Slideback Adjustment

This adjustment is provided by trimpot R63. Connect a voltmeter to the auxiliary video output along with a 50 Ohm termination. With no signal applied to the input of the receiver, enable slideback, rotate the front panel control fully clockwise, and adjust R63 for a DC output of about 2.8 Volts.

5.3. Slideback Indicator Threshold Adjustment

This adjustment is provided by trimpot R61. Connect an impulse generator to the input of the receiver and apply a signal. Set the receiver for its widest bandwidth. Set the amplitude of the generator and the gain of the receiver to produce about 2.5 Volts at the video output. Now enable slideback and adjust the front panel control so that the indicator just barely illuminates. Now reduce the signal generator level to about 100 mV and repeat.

5.4. Supplementary Video Amplifier Offset Adjustment

This adjustment is provided by trimpot R38. With the coax cable unplugged from the module video input at J5 and J5 terminated in 50 Ohms, adjust R38 for about 1 milliVolt of positive offset into a 50 Ohm load at the video output at J6.

6. CARDCAGE INTERFACE SUMMARY

Address 6D: Control latch:

Bits 0 - 5: reserved for DVM option

Bit 6: pulse stretch enable (1 = enable)

Bit 7: slideback enable (1 = enable)

R-110 RECEIVER MANUAL ADDENDUM: WIDEBAND OPTION

1. INTRODUCTION

The wideband option adds three extra bandwidths to the standard selection of the R-110B receiver. To do so it adds a new signal path in a separate cardcage plug-in module and replaces the video module as well.

There are currently two sets of wide bandwidths available: 20 - 40 - 100 MHz, and 40 - 100 - 200 MHz. One or the other may be chosen, but not both.

The wideband option is available for both the R-110 and the R-110B receivers. This document is an addendum to their technical manuals. Excerpts may be added to the user's manuals as applicable.

2. INSTALLATION

Physically, the wideband option consists of a new plug-in module for the receiver's cardcage, plus a replacement for the video module, plus modifications to the cardcage coax cable harness. While installation is not especially complicated, it is normally done at the factory during the original construction of the receiver. Retrofitting of the option in the field is possible, but it is recommended that this only be done by authorized factory field service personnel. In addition to installing the modules, configuration storage in the firmware must be modified, using a controlled-access procedure.

3. USAGE IN MANUAL MODE

The three new bandwidths are added to the selections accessed via the bandwidth up/down pushbuttons on the front panel of the receiver. When the widest standard bandwidth (15 MHz in most receiver configurations) is selected, pressing the "bandwidth up" button will select the first of the wideband filters, and so on. Pressing the "bandwidth down" button will select narrower bandwidths until the standard bandwidths are again selected. The buttons have an "auto-increment" mode, in which a new selection is performed every half second or so if a button is held down.

The wideband option uses a signal path that is separate from most of the receiver circuitry. The signal is taken from the wideband (1450 MHz) IF, and amplified and filtered. The signal returns to the normal signal path at the video detector, which has been upgraded as part of the wideband option to afford a wider bandwidth output. The separate wideband signal path places restrictions on the use of the wideband option, due to the fact that the 21.4 MHz IF is bypassed. This means that:

- Only the first conversion is available for tuning. This means that tuning is in increments of 5 MHz.
- The Band 1 and Band 2 signal paths are unavailable. This means that the minimum legal tuned frequency in wideband mode is 20 MHz.

The receiver protects against illegal conditions by refusing to tune below 20 MHz when wideband is selected, and refusing to select a wide bandwidth when tuned below 20 MHz. When in wideband mode only the tuned frequency of the first conversion is displayed, i.e. a multiple of 5 MHz.

The wideband signal path provides its own, separate programmable gain circuits. Although there are only two of these, as opposed to four in the normal signal path, the manual adjustment range of 50 dB is maintained, and is still set via the front panel gain control knob and display.

AGC is also provided for. Usage is the same as for the narrower bandwidths. The function is selected via the appropriate keypad alternate function.

Front end overload and underload detection circuits are provided, and drive the same cardcage status lines as the detectors in the normal signal path. They are used when auto-attenuation is enabled. With auto-attenuation disabled, a front end overload indication when wideband is enabled may be alleviated by increasing the input attenuation, using the appropriate front panel pushbutton.

A new video circuit is provided with the wideband option that is used for both wide and normal bandwidths. This video circuit accepts inputs from the wideband module, the 21.4 MHz IF module, and the DCIF. While the wideband signal path contains a separate detector, the video module provides an output buffer that is capable of delivering the widest available (200 MHz IF) bandwidth into 50 Ohms. In doing so a compromise was settled upon, in that the maximum video output is 3 Volts, as opposed to the 4 Volts available from the standard video module.

Log detection and BFO are unavailable in wideband. If one of these functions is selected at the same time that a wide bandwidth is selected, then the indicator associated with that function will blink. The Z axis output is available. The pulse stretch and slideback options, if present, are operational in wideband mode as well.

In summary, significant effort has been made to make manual control and monitoring of the wideband signal path as similar as possible to that of the normal signal path. The main differences, as mentioned above, are the restricted tuning range and resolution, the reduced maximum video output amplitude, and the lack of some video functions.

4. USAGE WITH IEEE-488 AND PROPRIETARY EXTERNAL INTERFACES

The IEEE-488 interface allows an external host computer to command and monitor the receiver's operation. The proprietary external interface allows receiver cardcage status plus the output of the DVM option to be transmitted to the host computer more quickly than is possible over the IEEE-488 interface. It nevertheless must operate in conjunction with the IEEE-488 interface since it is unidirectional (transmit only).

The IEEE-488 interface in the R-110 receiver has been designed to be compliant with the requirements of IEEE-488.2, which describes communications protocol, defines a number of "standard" commands and queries, and requires that many features that were options in IEEE-488.1 be present.

The standard and proprietary commands and queries supported by the basic R-110 receiver, and the R-110B, are given in their respective technical manuals. Those pertaining to the wideband option will be reviewed here.

The normal bandwidth commands and queries are extended when the wideband option is present. Wide bandwidths may be commanded in the same manner as normal bandwidths, e.g. <BW 100E6>. If the standard query is issued when a wide bandwidth is selected, the response will be in the standard format, e.g. <100E6>. The wide bandwidths are added to the list returned in reponse to the <BW? ALL> query.

The same restrictions apply here as in manual tuning: the tuning range is limited to 20 MHz on the low side, and tuning is limited to multiples of 5 MHz. A tuning command containing a frequency that is not a multiple of 5 MHz will be rounded to the nearest legal value. A tuning command containing a frequency below 20 MHz will be rejected.

The proprietary interface outputs buffered overload, underload, and lock status signals, along with DVM data if that option is present. The front end overload and underload signals are taken from the wideband signal path when a wide bandwidth is selected, and from the 21.4 MHz IF otherwise.

5. THEORY OF OPERATION

The hardware that is unique to the wideband option consists of the wideband filter module and the wideband video module. The operation of those two modules will be described here. Descriptions of the rest of the signal path and the supporting hardware, such as synthesizers, the controller, and the power supply, are described in the R-110 and R-110B technical manuals.

The signal feeding the wideband filter module is taken from the microwave module at the output of the first mixer, using a solid state switch. Only one stage of amplification has been provided in front of the mixer, so the signal level at this point is typically very low. The result of the first conversion is an IF frequency of 1450 MHz. No filtering is performed on the signal from the mixer output before passing it to the wideband filter module.

5.1. Wideband Filter Module Operation

The input signal from the microwave module is first given three stages of amplification, increasing the signal level by about 23 dB. Overload / underload conditions are sensed here, using a coupling consisting of a PCB trace laying parallel to the trace containing the main signal. Overload and underload conditioning will be described later. The main signal is then distributed to one of three IF filters, using solid state switches. Unlike the 21.4 MHz IF filters, these are not daisy-chained. Instead, only one filter is selected at a time. Depending on which option has been ordered, these filters can be 20, 40, and 100 MHz, or 40, 100, and 200 MHz. The outputs of the two wider filters are padded to reduce their amplitude, in accordance with the gain scheme that maintains noise amplitude constant over all bandwidths. This means that the amplitude of a given filter output must be reduced by the square root of its ratio to the bandwidth of the next narrower filter. These filters not only set the IF bandwidth, they also act to isolate the 1450 MHz IF signal from the variety of signals produced by the mixer in the microwave module.

Just as the signal was sent to a particular filter using solid state switches, the output of the selected filter is obtained by a second set of switches. The signal from the selected filter is passed through a voltage controlled attenuator, and from there is delivered to a set of four more gain stages. The control for the variable attenuator is supplied by a D/A converter, described later. The attenuator has a range of about 25 dB.

The output of the second set of gain stages is passed through a filter with a bandwidth of 200 MHz, to reduce out-of-band noise. The signal is then passed through a second variable attenuator, also controlled by a D/A converter. The output of the attenuator feeds four more gain stages through a coupling that again consists of a trace laying parallel to the signal trace. The tap signal from the coupling is sent to the IF output when wideband is enabled, using a solid state switch to select between it and the 21.4 MHz IF output. The signal level delivered to the IF output is a function of input signal level the input attenuation setting, selected bandwidth, and the IF gain setting. The maximum gain is about 15 dB.

The output of the set of four gain stages is padded lightly to set the signal level to approximately +6 dBm with -52 dBm at the module input. This signal feeds the wideband detector, which consists of two more gain stages driving a pair of diodes, followed by a buffer amplifier to ensure sufficiently high impedance at the diodes. The gain of this amplifier is less than unity because it is limited to about 1 Volt output at the necessary bandwidth, while the diodes need to be driven as strongly as possible in order to maximize the instantaneous dynamic range. The output of the buffer amplifier is sent to the wideband video module.

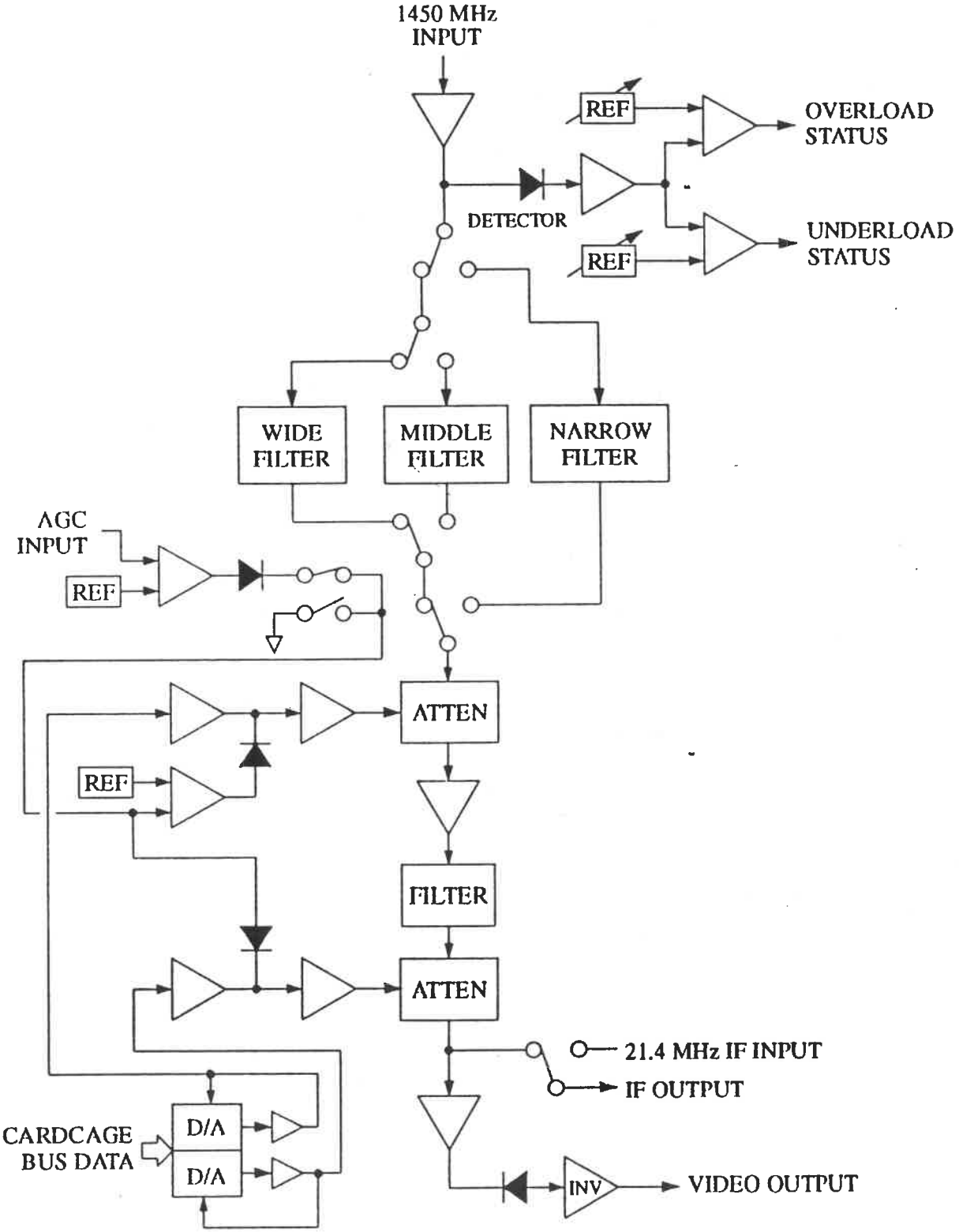


Figure 1: Wideband Filter Module Block Diagram

An FM deviation signal is produced by passing the DC offset of the discriminator outputs through an amplifier (U24A). The appropriate input (selected 21.4 MHz discriminator or selected 455 kHz discriminator) is chosen by switch U26A. Trimming adjustments are provided individually for each discriminator (R83 for 15 MHz, R81 for 1 MHz, R79 for 100 kHz, R82 for 20 kHz, R80 for 3 kHz), selected by switches (U26B, U27) controlled by the cardcage bus interface. The output is set so as to be midrange (2.5 Volts) for center-frequency tuning. The amplifier output feeds a connector (J6), and is routed from there to the DVM option cardcage module, if present.

The cardcage interface consists of address decoding (U3, U4) a data latch (U2), and a switch and relay driver (U1). The latch is reset on power-up and is accessed through cardcage bus address 72(hex), as determined by the address decoder. The buffered latch bits control relays K1 - K3 and selection switches for the various discriminators and deviation trimmers. A pair of local voltage regulators (U5, U6) generate the +10.6 Volt power required by the discriminator chips from the cardcage +15 Volt power line. In addition, a switch (U25C) controls power applied to the local oscillator. The oscillator is powered down when a 21.4 MHz discriminator is selected.

Besides the latch bits for AM/FM selection and discriminator selection, there is a narrowband selection bit that must be asserted when one of the 455 MHz discriminators is selected.

7. FIELD SERVICE ADJUSTMENTS

The FM option cardcage module contains a number of adjustments which may be performed in the field. All of these require that the outside case of the receiver be removed for access. In addition, most adjustments require that the cardcage module be placed on extender card, to afford access to the adjustments.

7.1. 21.4 MHz Discriminator Quadrature Coils

The 15 MHz discriminator consists of U17, L7, and surrounding components. The 1 MHz discriminator consists of U16, L6, and surrounding components. Both may be adjusted using the same procedure.

1. Apply a 21.4 MHz signal at -30 dBm to module input J1.
2. Select FM mode and select the desired bandwidth to be adjusted (15 MHz or 1 MHz).
3. Monitor pin 1 of the appropriate discriminator (U17 for 15 MHz, U16 for 1 MHz) and adjust the appropriate coil tuning slug (L7 for 15 MHz, L6 for 1 MHz) for 5.0 Volts at pin 1 of the IC.

7.2. Local Oscillator Adjustment

The local oscillator consists of crystal Y1, transistor Q1, and amplifier U7, plus surrounding components. One of these, C17, allows the frequency of the oscillator to be trimmed.

1. Connect a frequency counter to U7 pin 6 and monitor the frequency there.
2. Adjust C17 for a reading of 20.945 MHz.

7.3. 455 kHz Discriminator Outputs

Each of the three 455 kHz discriminators has a trimpot connected to its output. The purpose of this is to equalize the gains. R45 is for the 100 kHz discriminator, R48 is for the 20 kHz discriminator, and R50 is for the 3 kHz discriminator.

1. Monitor the signal at the signal at the module output (J4).
2. Apply a 21.4 MHz signal modulated at 1 kHz with 75% deviation at -30 dBm at module input J1.

3. Select FM mode and 1 MHz bandwidth. Measure the signal amplitude at the output.
4. Select 100 kHz bandwidth. Adjust R45 for the same amplitude.
5. Select 20 kHz bandwidth. Adjust R48 for the same amplitude.
6. Select 3 kHz bandwidth. Adjust R50 for the same amplitude.

7.4. FM Deviation Null Level

Each of the five discriminators has a separate trimmer to set its FM deviation null level.

1. Connect a signal at 21.4 MHz and -30 dBm to the module input at J1.
2. Monitor the signal at the carrier deviation output (J6).
3. Select FM mode and 15 MHz bandwidth, and adjust R83 for 2.5 Volts at the output.
4. Select 1 MHz bandwidth and adjust R81 for 2.5 Volts at the output.
5. Select 100 kHz bandwidth and adjust R79 for 2.5 Volts at the output.
6. Select 20 kHz bandwidth and adjust R82 for 2.5 Volts at the output.
7. Select 3 kHz bandwidth and adjust R80 for 2.5 Volts at the output.

8. CARDCAGE BUS INTERFACE SUMMARY

The control latch is at address 72(hex):

Bit 0 = AM/FM select:

0 = AM

1 = FM

Bit 1 = narrowband select:

0 = 21.4 MHz discriminators

1 = 455 kHz discriminators

Bit 2 = 15 MHz discriminator select (1 = select)

Bit 3 = 1 MHz discriminator select (1 = select)

Bit 4 = 100 kHz discriminator select (1 = select)

Bit 5 = 20 kHz discriminator select (1 = select)

Bit 6 = 4 kHz discriminator select (1 = select)

Bit 7 = (unused)

The overload / underload pickoff is peak detected with a diode and a low-pass filter, and is then buffered by an opamp. The amplifier output is fed to individual comparators for overload and underload, the references for which are set by trimpots, based on a reference that provides temperature correction by means of a diode and an opamp buffer. The comparator outputs are gated with an enable signal, and finally control individual drivers that are set up to provide a high-impedance output to the cardcage status lines (which are supplied with pullup resistors) when status is "good", and to provide a low-driven output when status is "bad". Overload status is applied to cardcage bus STAT1, and underload status is applied to cardcage bus STAT3, both of which are shared with similar status signals supplied by the 21.4 MHz IF. The 21.4 MHz IF will not be enabled when the wideband option is in use, and vice versa.

Intelligent gain control is provided by a double 12 bit D/A converter IC, which is connected to the cardcage control bus. Since this is an 8 bit bus, four addresses are used to load data into holding registers in the IC, plus a fifth address to apply all of it to the outputs simultaneously. The D/A converter IC outputs are current mode, so a pair of opamps are used to convert to voltage mode, as required by the attenuators. Note that the attenuators are not perfectly linear, so that the firmware maintains individual and unique calibration tables for each of them. One of the procedures required when initially configuring a receiver or when replacing the wideband filter module is to connect the receiver to an IEEE-488 interface-based system and run an automated calibration program on the host computer. This updates the calibration tables for the attenuators and provides gain control accuracy that is nominally within 1 dB of the front panel display for "regular" signals. A +10V precision reference is inverted by an opamp to provide a stable reference voltage for the D/A converters.

Automatic gain control (AGC) is provided by a circuit that takes its input from the video signal, buffers and peak-detects it, and combines it into the signals from the D/A converter outputs. This is somewhat complicated, involving several stages of selectable gain and offset tweaking, depending upon whether or not AGC is enabled. Diodes couple the AGC voltage into the gain control signals, so that the AGC is only effective when the attenuation required is greater than that set by the D/A converters. When operating with AGC enabled, the front panel gain control is normally left set to maximum, to give the AGC circuit its maximum control range. The AGC signal to the first attenuator is delayed from that to the second, to avoid degrading the noise figure.

As described above, filter selection is performed by solid state switches, with only one filter selected at a time. Control of these switches is provided by a latch connected to the cardcage control bus. Latched control bits drive comparators, which output the required (non-TTL) control voltages for the switches. The same latch also supplies control bits for wideband and overall module enable.

5.2. Wideband Video Module Operation

The wideband video module performs the same functions as the standard video module, with increased bandwidth for those functions that involve the wideband signal path. The log detector, 21.4 MHz linear detector, and BFO are essentially duplicates of the circuitry on the standard module. The video and Z axis amplifiers are different. Additional connectors are provided for wideband inputs and outputs.

There are four signal inputs to the wideband video module: one from the wideband filter module, two from the 21.4 MHz IF, and one from the DCIF module. The 21.4 MHz IF is tapped in two different places, once for AM and BFO detection and once for log detection, so that the gain distribution will work out correctly in each case. The requirements for each are different because the log detector has over 70 dB of dynamic range while the linear detector has only a little more than 30 dB. The BFO uses the same input as the AM detector because here the available dynamic range is not a consideration.

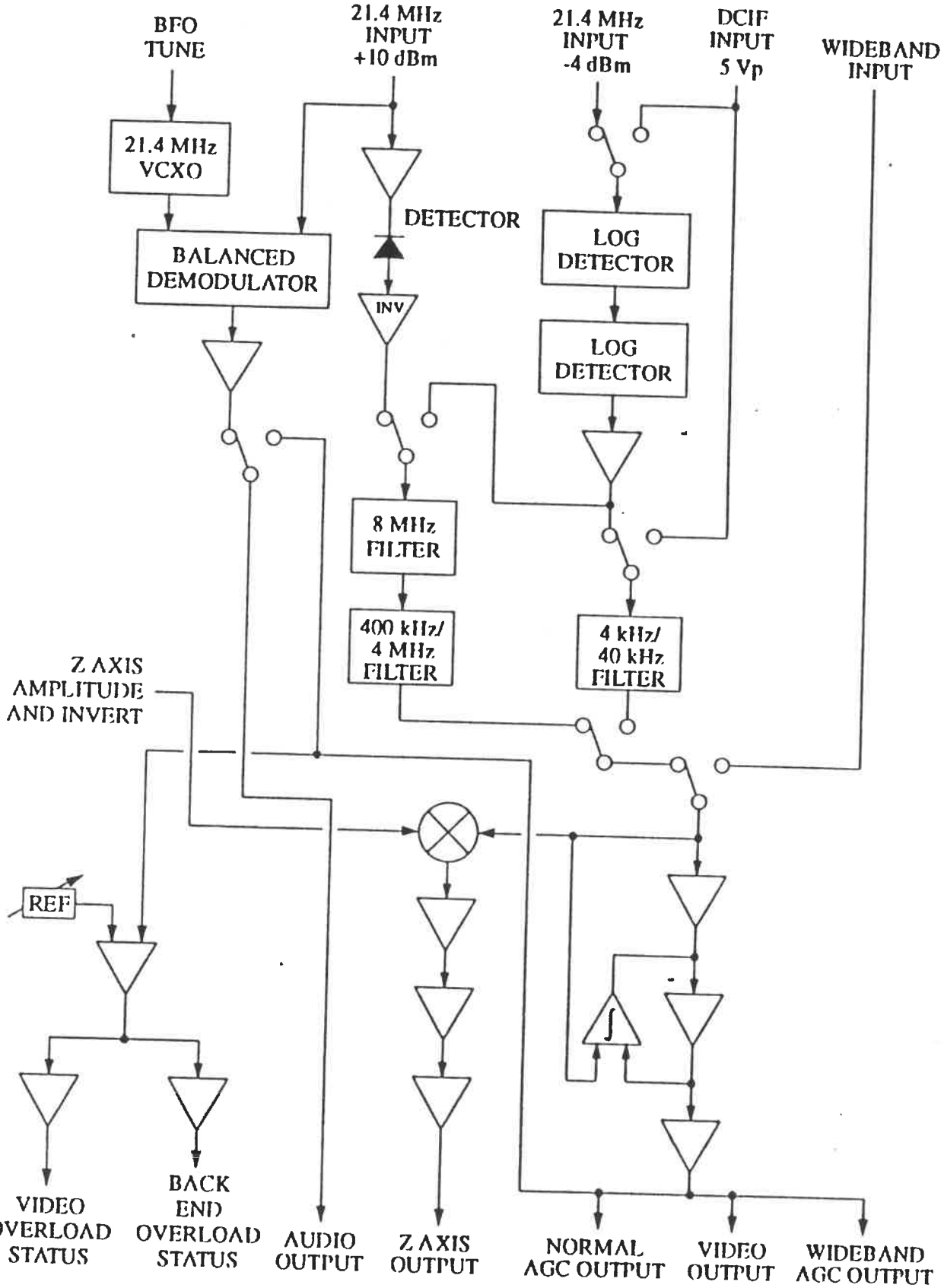


Figure 1: Wideband Video Module Block Diagram

The 21.4 MHz IF input destined for wideband AM detection arrives at at a maximum level of +10 dBm and is routed to the detector circuit throught a pad and an AC coupling. The pad is selected to place the full-scale value of the input at the detector overload threshold. While the detector itself is basically a diode, dynamic range is maximized by placing the diode behind a tuned amplifier which steps the signal level up to a point where the effect of the turn-on characteristic of the diode is minimized. The tuned amplifier is based on a transistor and a low-Q tuned network. The diode is followed by an opamp, to maintain the impedance at the detector diode and to provide thermal compensation. The gain of the opamp is trimmed during test to establish end-to-end gain. A second transistor acts as a switch to disable the detector when it is not in use. The detector is followed by a carrier-removal filter that consists of a series of L-C low-pass filters, totalling 8 poles with a corner at 8 MHz. This filter is also used by the log detector.

End-to-end gain of the 21.4 MHz AM detector is 10 dB, so that a +10 dBm input will produce a full-scale output of 0 - 3 Volts peak. Dynamic range at full scale output is at least 30 dB.

The output of the filter provides the input for a second, selectable video noise filter. This filter is a one-pole low-pass R-C configuration, in which any combination of two capacitors may be selected by the firmware. In actual usage only one (or none) of these is selected at a time, however. The corners are at 400 kHz and 4 MHz. Selection is based on the selected 21.4 MHz IF bandwidth. Table I shows the correlation between IF bandwidth and the selected video filter, including the filters in the DCIF video signal path (described below).

The input for the log detector can come from one of two places, either from the other 21.4 MHz IF input (the one that doesn't supply the AM detector) or from the DCIF. Selection is made by a relay under the control of the firmware. A termination resistor is switched onto the 21.4 MHz IF input when it is not in use. Furthermore, the input from the DCIF may be switched around the log detector, bypassing it, when a linear characteristic is desired. When routed through the log detector, the DCIF signal, even through it arrives already detected and carrier-filtered, is given the same log-compression gain characteristic as the detected signal from the 21.4 MHz IF.

The log detector consists of a pair of log amplifier/detectors, which output in current mode, followed by a linear amplifier, which provides a voltage output. The IF signal from the input is fed in series from the first log amp to the second, while their detected video outputs are summed at the voltage amplifier. An input offset adjustment is provided to null the output of the log amps. A resistor is selected during module test to set the full scale output level at the output of the voltage amplifier. The voltage amplifer output is sent along two paths. One path is to the same 8-pole carrier removal filter used by the 21.4 MHz AM detector, selected by a relay under firmware control. The other path is through another relay that selects between this and the raw DCIF input, again under firmware control. The signal that is selected by the relay is passed through another video filter, which provides a fixed corner at 40 kHz and a selectable corner at 4 kHz. The outputs of this and the other video filter are now recombined into a single path, using another relay, again under firmware control. This signal is padded and delivered to yet another relay, that selects between it and the input from the wideband filter module. This signal, then, is delivered to the video and Z axis amplifiers.

Gain of the log detector is such that at full scale, every 10 dB coming in will produce 375 mV at the video output. Dynamic range at full scale is in excess of 70 dB. The front end of the log detector has a bandwidth of 120 MHz, much greater than the 8 MHz maximum bandwidth of the carrier removal and video filters that follow.

The BFO detector consists of a 21.4 MHz Clapp oscillator based on a crystal and driven by a transistor, fine-tuned by a varactor diode. An on/off switch is provided by a FET switch, which disables the oscillator by removing power from it. Tuning frequency control is provided by a potentiometer on the receiver front panel. A constant current source based on a FET drives the front panel control, developing a voltage which varies linearly with its setting while requiring only one "hot" line and a return running off of the module. The voltage derived from the control setting is used to tune the varactor. A trimmer on the module is used to set the center frequency, while a variable inductor is used to set the adjustment range.

The oscillator drives a mixer, the other input of which is the same tap of the 21.4 MHz IF used by the AM detector. The difference output generated by the mixer is offset from baseband by an amount determined by the front panel control setting, whthin a range of +/- 4 kHz. The output of the mixer is filtered to remove unmixed and summed products, and is amplified by an opamp. The output of this amplifier is sent to the audio output when enabled, routed by a FET switch under firmware control. For a full-scale input of +10 dBm, the output will be 1.6 Volts peak-to-peak. Dynamic range is not a consideration because the BFO is used for detection of CW signals

Table 1: Video Noise Filter Selection

Bandwidth Range	Filter Corner
200 Hz - 2 kHz	4 kHz
2.5 kHz - 20 kHz	40 kHz
50 kHz - 200 kHz	400 kHz
300 kHz - 2 MHz	4 MHz
4 MHz - 15 MHz	None

The video amplifier is upgraded in the wideband video module. It consists of three stages, plus a DC servo amplifier. The first two stages provide gain, with the first stage providing most of it because the second, while it can provide high output levels, is limited in its maximum gain capability. The final stage is a unity gain buffer that drives the video output on the front panel of the receiver through a resistor that sets the source impedance to 50 Ohms. It also feeds the 21.4 MHz IF and wideband filter module AGC inputs, the audio output (through a FET switch that selects between the video output and the BFO output), and the video overload detector. The maximum available output is 3 Volts peak, and the maximum bandwidth is about 100 MHz. The DC servo amplifier is looped around the second stage amplifier, acting as an integrator that compares the input to the output and generates a correction voltage to yield zero DC output. Trimpots are provided to pre-correct the offset for both the wideband and 21.4 MHz IF / DCIF inputs. The appropriate trimpot voltage is selected by means of FET switches.

The Z axis amplifier is also upgraded in the wideband video module. It consists of an analog multiplier followed by a current-to-voltage converter, followed by an amplifier stage and an output buffer stage. The analog multiplier is used for gain control and signal inversion. A constant current source based on a FET drives a potentiometer on the front panel of the receiver. The pot setting therefore establishes the voltage drop across it, requiring only a hot line and a return, which can be configured as a coax cable to minimize noise pickup. The voltage is buffered by an opamp and selectively inverted by a FET switch in conjunction with another amplifier, under firmware control. The FET switch sets the gain of the amplifier to +/-1 by supplying signal to both differential inputs (gain = +1) or grounding the positive input (gain = -1). The output of this amplifier provides the control voltage for a four-quadrant multiplier that processes the video signal accordingly. The output of the multiplier is in differential current mode, and is converted to single-ended voltage mode by an opamp. The next stage adds gain and generates a large output signal range. The final stage is a unity-gain buffer followed by a resistor that sets the source impedance to 50 Ohms. The output capability of this circuit is again 3 Volts peak at 100 MHz bandwidth.

The overload detector consists of a high-speed comparator that measures the video output against a reference set by a trimpot. The output is inverted by a transistor that provides a faster slew rate and also extends narrow pulses. The transistor output controls a pair of drivers that drive two of the cardcage bus status lines. The drivers are configured to have high-impedance outputs when status is "good" (the cardcage bus status lines are supplied with pullup resistors to make this state float high), and low-driven outputs when status is "bad". This allows multiple drivers to be connected to a single status line, with any one of them able to report "bad" status. The two cardcage bus status lines used here are STAT2 (back end overload) and STAT7 (video module overload). Currently each of these two lines is used only by the video module.

The cardcage bus control interface consists of address decoding and a pair of latches. The latches provide control for video filter selection, DCIF / 21.4 MHz IF / wideband input selection, log detector selection, BFO selection, and Z axis selection and inversion control.

6. MAINTENANCE AND FIELD SERVICE ADJUSTMENTS

Preventative maintenance for the wideband option hardware is the same as for the rest of the receiver. Hardware calibration may be required periodically, or when a module is replaced. Field service adjustments are described in the following paragraphs.

6.1. Wideband Filter Module Field Service Adjustments

The wideband filter module provides just two field service adjustments, these being the overload and underload thresholds. In order to have access to the adjustment components, the module must be raised above the cardcage using a cardcage bus extender and coax cable extensions.

6.1.1. Overload Threshold Adjustment

Procedure:

1. Remove the coax cable from module connector J1 and connect a microwave signal generator. Apply a CW signal at 1450 MHz and -3 dBm.
2. Select 40 MHz bandwidth.
3.) Adjust trimpot R39 so that the front overload indicator on the front panel of the receiver just comes on.

6.1.2. Underload Threshold Adjustment

Procedure:

1. Use the same signal generator hookup as the foregoing procedure Reduce the amplitude to -16 dBm.
2. Monitor connector P1 (the cardcage bus connector) pin B20 with a voltmeter.
3. Adjust trimpot R41 so that the voltage on pin B20 just switches from near +5V to near 0V.

6.2. Wideband Video Module Field Service Adjustments

The wideband video module provides many of the same adjustments as the standard video module, since it uses many of the same circuits. In order to have access to the adjustment components, the module must be raised above the cardcage using a cardcage bus extender and coax cable extensions.

6.2.1. Log Detector Null Adjustment

Procedure:

1. With no signal applied and the coax cable removed from J2, monitor U3 pin 6 with a voltmeter.
2. Select log detection on the front panel of the receiver. Select a bandwidth that is not wideband.
3. Adjust trimpot R22 for minimum voltage at U3 pin 6.
4. Disable log detection. Reconnect the cable to J2.

6.2.2. BFO Center Frequency Adjustment

Procedure:

1. Remove the coax cable from module connector J1 and connect a signal generator. Set the signal generator to CW at 21.4 MHz, -10 dBm.
2. Select BFO on the front panel of the receiver, with a compatible bandwidth (e.g. 1 MHz).
3. Monitor U28 Pin 6 with an oscilloscope.
4. Adjust trimpot R106 so that the beat frequency indicated on the oscilloscope with the BFO control on the receiver's front panel fully counterclockwise is the same as the beat frequency indicated with the control fully clockwise. Make sure that there is a null in between.
5. Restore the coax cable connection to J1.

6.2.3. Video Amplifier Offset Adjustments

Procedure:

1. With no signal applied, set the receiver gain control to minimum.
2. Select a DCIF bandwidth (e.g. 20 kHz) on the front panel of the receiver.
3. Monitor J8 with a voltmeter.
4. Adjust trimpot R65 for minimum output WITHOUT EVER LETTING THE VOLTAGE AT J8 GO NEGATIVE.
5. Select a wide bandwidth (e.g. 100 MHz) on the front panel of the receiver.
6. Adjust trimpot R64 for minimum output at J8 WITHOUT EVER LETTING THE VOLTAGE AT J8 GO NEGATIVE.

6.2.4. Z Axis Amplifier Offset Adjustment

Procedure:

1. With no signal applied, set the receiver gain to minimum.
2. Select a wide bandwidth (e.g. 100 MHz) and enable the Z axis function, no inversion, on the front panel of the receiver.
3. Monitor J10 with a voltmeter.
4. Adjust trimpot R154 for minimum output WITHOUT EVER LETTING THE VOLTAGE AT J10 GO NEGATIVE.

6.2.5. Z Axis Amplifier Multiplier Null Adjustment

This adjustment is occasionally necessary, but requires a fairly complicated test setup. If this adjustment must be performed, contact the factory for a suggested procedure with available test equipment.

6.2.6. Overload Threshold Adjustment

Procedure:

1. Remove the coax cable from module connector J3 and apply 5.25 VDC.
2. Select a bandwidth of 20 kHz to select J3 as the module input.
3. Adjust trimpot R96 so that the back overload indicator on the front panel of the receiver just comes on.

7. CONTROL INTERFACE

The control interface for the wideband module consists of six contiguous write-only ports mapped into the microcontroller's external read/write memory space. The first four addresses are for the gain control DACs, the fifth is a strobe to load the DAC, and the sixth loads a control latch.

Address 60H = DAC A low byte:

Bits 0 - 7 = DAC A bits 0 - 7

Address 61H = DAC A high nibble:

Bits 0 - 3 = DAC A bits 8 - 11

Bits 4 - 7 = spare

Address 62H = DAC B low byte:

Bits 0 - 7 = DAC B bits 0 - 7

Address 63H = DAC B high nibble:

Bits 0 - 3 = DAC B bits 8 - 11

Bits 4 - 7 = spare

Address 64H = DAC load strobe

Bits 0 - 7 = unused

Address 65H = control latch:

Bit 0 = BW #1 enable (the narrowest)

Bit 1 = BW #2 enable (the middle one)

Bit 2 = BW #3 enable (the widest)

Bits 3 - 5 = spare

Bit 6 = wideband AGC enable

Bit 7 = wideband module enable

The control interface for the wideband video module is very similar to that for the standard video module, consisting of two control latches mapped into two contiguous microcontroller external read/write memory addresses.

Address 7E = control latch #1:

Bit 0 = 4 MHz video filter enable

Bit 1 = 400 kHz video filter enable

Bit 2 = unused

Bit 3 = 4 kHz video filter enable

Bit 4 = DCIF / 21.4 MHz IF log detector input select:

0 = DCIF

1 = 21.4 MHz IF

Bit 5 = Log / Lin select:

0 = linear detection

1 = log detection

Bit 6 = medium bandwidth / narrow bandwidth video select:

0 = medium bandwidth

1 = narrow bandwidth

Bit 7 = spare

Address 7F = control latch #2:

Bit 0 = BFO enable

Bit 1 = Z axis enable

Bit 2 = Z axis invert

Bit 3 = wideband enable

0 = 21.4 MHz IF

1 = wideband

Bits 4 - 7 = spare

SECTION 6. PARTS LISTS AND SCHEMATICS

6.1 Introduction

Hardware documentation for the R-110 is structured as an "indentured drawing list" (IDL). In this format the receiver top assembly is broken into major assemblies, which in turn are broken into subassemblies, in the form of a tree. Included are assembly drawings, de ail drawings, specifications for individual parts, parts lists, test procedures, and schematics.

This section contains a complete copy of the indentured drawing list, plus copies of the pertinent assembly drawings, parts lists, and schematics. Note tha some assemblies lack schematics, or share a schematic with other assemblies, or may be indicated at different levels of detail on different schematics.

6.2 Indentured Drawing List

The complete indentured drawing list is shown in table 6-1. The list contains details, assemblies, schematics, test procedures, and parts specifications for the radio.

Table 6-1: Indentured Drawing List

Indent Level	Part Number	Type	Title
0	493000	Assy	R-110 Receiver
1	493000TP	TP	R-110 Receiver
1	493001	Sch	R-110 Receiver
1	493050	Assy	Cardcage
2	493051	Sch	Cardcage
2	493055	Assy	Cardcage/Front Panel Cable Set
2	493057	Assy	Cardcage Cable Harness
2	493060	Assy	Cardcage Backplane
3	493061	Sch	Cardcage Backplane
3	493062	Det	Cardcage Backplane
2	493065	Assy	Microwave RF Module Power Cable

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
2	493100	Assy	Microwave RF Module
3	167082	Spec	1447.5 MHz Bandpass Filter
3	167084	Spec	550 MHz Bandpass Filter
3	493100TP	TP	Microwave RF Module
3	493101	Sch	Microwave RF Module
3	493107	Det	Microwave RF Module PCB
3	493112	Det	Microwave RF Module Housing
3	493113	Det	Microwave RF Module Holder
3	493114	Det	Microwave RF Module Cover #1
3	493115	Det	Microwave RF Module Cover #2
3	493116	Det	Microwave RF Module Cover #3
3	493117	Det	Microwave RF Module Cover #4
3	493118	Det	Microwave RF Module Cover #5
3	493119	Det	Microwave RF Module Cover #6
3	493120	Det	Microwave RF Module Holder #1
3	493121	Det	Microwave RF Module Holder #2
3	493122	Det	Microwave RF Module Holder #3
3	493123	Det	Microwave RF Module Holder #4
3	493124	Det	Microwave RF Module Holder #5
3	493128-1	Det	Microwave RF Module Short Septum Block
3	493128-2	Det	Microwave RF Module Long Septum Block

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
3	493130	Assy	RF Input Converter PCB
4	493132	Det	RF Input Converter PCB
4	493175-1	Assy	75 nH Inductor
3	493135	Assy	RF Input Limiter PCB
4	493137	Det	RF Input Limiter PCB
3	493140	Assy	1450 MHz Prefilter PCB
4	493142	Det	1450 MHz Prefilter PCB
4	493175-1	Assy	75 nH Inductor
3	493150	Assy	1450 - 550 Converter PCB
4	493152	Det	1450 - 550 Converter PCB
4	493175-1	Assy	75 nH Inductor
3	493170	Assy	550 - 21.4 MHz Converter PCB
4	493172	Det	550 - 21.4 MHz Converter PCB
4	493175-2	Assy	150 nH Inductor
2	493180	Assy	Low Frequency RF Module
3	469078-047	Assy	RF Transformer
3	493900-109	Assy	700 nH Variable Inductor
3	493900-110	Assy	1.6 uH Variable Inductor
3	493900-112	Assy	32 uH Variable Inductor
3	493900-122	Assy	139 nH Variable Inductor
3	493900-123	Assy	2 uH Variable Inductor
3	493180TP	TP	Low Frequency RF Module
3	493181	Sch	Low Frequency RF Module
3	493182	Det	Low Frequency RF Module PCB
3	493860-5	Det	Low Frequency RF Module Shield
3	493862	Det	Module Insulator

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
2	493190	Assy	Preselector Module
3	469386	Spec	1100 MHz Lowpass Filter
3	493190TP	TP	Preselector Module
3	493191	Sch	Preselector Module
3	493192	Det	Preselector Module PCB
3	493193	Assy	530 MHz PLL Subassembly
4	493194	Det	530 MHz PLL Subassembly PCB
4	493195	Det	530 MHz PLL Subassembly Can
4	493196	Det	530 MHz PLL Subassembly Cover
3	493198	Mod	Filter Mounting Clamp
3	493860-2	Det	Preselector Module Shield
3	493862	Det	Module Insulator
2	493200	Assy	21.4 MHz IF Amplifier Module
3	469078-022	Assy	0.427 uH Variable Inductor
3	493200TP	TP	21.4 MHz IF Amplifier Module
3	493201	Sch	21.4 MHz IF Amplifier Module
3	493202	Det	21.4 MHz IF Amplifier Module PCB
3	493860-6	Det	21.4 MHz IF Amplifier Module Shield
3	493862	Det	Module Insulator

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
2	493250	Assy	21.4 MHz IF Filter Module
3	167085	Spec	21.4 MHz / 80 kHz Crystal Filter
3	493900-016	Assy	0.29 uH Variable Inductor
3	493900-116	Assy	312 nH Inductor
3	493900-117	Assy	0.13 uH Variable Inductor
3	493900-118	Assy	0.23 uH Variable Inductor
3	493900-119	Assy	0.91 uH Variable Inductor
3	493900-120	Assy	0.96 uH Variable Inductor
3	493900-121	Assy	1.3 uH Variable Inductor
3	493250TP	TP	21.4 MHz IF Filter Module
3	493251	Sch	21.4 MHz IF Filter Module
3	493252	Det	21.4 MHz IF Filter Module PCB
3	493860-8	Det	21.4 MHz IF Filter Module Shield
3	493862	Det	Module Insulator
2	493300	Assy	Microwave Synthesizer Module
3	168007	Spec	100 MHz Crystal Oscillator
3	493900-107	Assy	210 uH Variable Inductor
3	493300TP	TP	Microwave Synthesizer Module
3	493301	Sch	Microwave Synthesizer Module
3	493302	Det	Microwave Synthesizer Module PCB
3	493310	Assy	Microwave Synthesizer PROM
3	493860-17	Det	Microwave Synthesizer Module Shield
3	493863	Det	Microwave Synthesizer Module Insulator

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
2	493330	Assy	Fixed LO Synthesizer Module
3	469078-006	Assy	1 mH Variable Inductor
3	493330TP	TP	Fixed LO Synthesizer Module
3	493331	Sch	Fixed LO Synthesizer Module
3	493332	Det	Fixed LO Synthesizer Module PCB
3	493335	Assy	21.4 MHz VCO Subassembly
4	493335TP	TP	21.4 MHz VCO Subassembly
4	493337	Det	21.4 MHz VCO Subassembly PCB
4	493338	Det	21.4 MHz VCO Subassembly Can
4	493339	Det	21.4 MHz VCO Subassembly Cover
3	493860-15	Det	Fixed LO Synthesizer Module Shield
3	493862	Det	Module Insulator
2	493350	Assy	Low Frequency Synthesizer Module
3	469078-006	Assy	1 mH Variable Inductor
3	493900-107	Assy	210 uH Variable Inductor
3	493350TP	TP	Low Frequency Synthesizer Module
3	493351	Sch	Low Frequency Synthesizer Module
3	493352	Det	Low Frequency Synthesizer Module PCB
3	493355	Assy	21 - 38 MHz VCO Subassembly
4	493355TP	TP	21 - 38 MHz VCO Subassembly
4	493356	Sch	21 - 38 MHz VCO Subassembly
4	493357	Det	21 - 38 MHz VCO Subassembly PCB
4	493358	Det	21 - 38 MHz VCO Subassembly Can
4	493359	Det	21 - 38 MHz VCO/DDS Filter Cover

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
3	493360	Assy	DDS Filter Subassembly
4	493360TP	TP	DDS Filter Subassembly
4	493362	Det	DDS Filter Subassembly PCB
4	493363	Det	DDS Filter Subassembly Can
4	493359	Det	21 - 38 MHz VCO/DDS Filter Cover
3	493860-16	Det	Low Frequency Synthesizer Module Shield
3	493862	Det	Module Insulator
2	493400	Assy	Video Module
3	493900-101	Assy	4.5 uH Inductor
3	493900-102	Assy	4.2 uH Inductor
3	493900-103	Assy	6 uH Variable Inductor
3	493900-104	Assy	7 uH Variable Inductor
3	493900-105	Assy	5 uH Variable Inductor
3	493900-106	Assy	1.2 uH Variable Inductor
3	493400TP	TP	Video Module
3	493401	Sch	Video Module
3	493402	Det	Video Module PCB
3	493860-9	Det	Video Module Shield
3	493862-1	Det	Module Insulator
2	493500	Assy	DCIF Module
3	493500TP	TP	DCIF Module
3	493501	Sch	DCIF Module
3	493502	Det	DCIF Module PCB
3	493860-11	Det	DCIF Module Shield
3	493862	Det	Module Insulator

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
2	493735	Det	GPIB/Status Connector Mounting Plate
2	493850	Det	Cardcage
2	493851	Det	Long Backplane Mounting Bracket
2	493852-1	Det	Short Backplane Mounting Bracket
2	493852-2	Det	Short Backplane Mounting Bracket
2	493853	Det	Backplane Stiffener
2	493855	Det	Mu-Metal Power Supply Shield
1	493600	Assy	Front Panel
2	493600TP	TP	Front Panel
2	493601	Sch	Front Panel
2	493602	Det	Front Panel
2	493607	Assy	Front Panel Bulkhead Subassembly
3	493607TP	TP	Front Panel Bulkhead Subassembly
3	493608	Det	Front Panel Bulkhead Subassembly
3	493616	Det	RF Input Attenuator Insulator
3	493617	Det	RF Relay Insulator
3	493650	Assy	X Axis/Audio Amplifier PCB Subassembly
4	493650TP	TP	X Axis/Audio Amplifier PCB Subassembly
4	493651	Sch	X Axis/Audio Amplifier PCB Subassembly
4	493652	Det	X Axis/Audio Amplifier Subassembly PCB
3	493670	Assy	Front Panel Semi-Rigid Cables
3	493675	Assy	RF Input Attenuator Subassembly
3	493677	Assy	RF Relay Subassembly
2	474243	Assy	Tuning Control Subassembly

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
2	493610	Det	Large Bezel
2	493611	Det	Large Window
2	493612	Det	Small Bezel
2	493613	Det	Small Window
2	493620	Assy	Switch/Display PCB Subassembly
3	469078-006	Assy	1 mH Variable Inductor
3	493605	Det	Large Display Overlay
3	493606	Det	Small Display Overlay
3	493620TP	TP	Switch/Display PCB Subassembly
3	493621	Sch	Switch/Display PCB Subassembly
3	493622	Det	Switch/Display Subassembly PCB
3	493623-1	Assy	Lighted Pushbutton Switch Subassembly
3	493623-2	Assy	Lighted Pushbutton Switch Subassembly
3	493623-3	Assy	Lighted Pushbutton Switch Subassembly
3	493625	Det	Pushbutton Switch Spacer
3	493626	Assy	Pushbutton Keycap Engraving
3	493865	Det	Switch/Display Subassembly Shield
2	493630	Assy	Interface PCB Subassembly
3	469078-006	Assy	1 mH Variable Inductor
3	493630TP	TP	Interface PCB Subassembly
3	493631	Sch	Interface PCB Subassembly
3	493632	Det	Interface Subassembly PCB

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
2	493640	Assy	Processor PCB Subassembly
3	469078-006	Assy	1 mH Variable Inductor
3	469078-115	Assy	2.8 uH Inductor
3	493640TP	TP	Processor PCB Subassembly
3	493641	Sch	Processor PCB Subassembly
3	493642	Det	Processor Subasssembly PCB
3	493645	Assy	Processor EPROM Subassembly
2	493655	Assy	Power Switch Subassembly
2	493657	Assy	Audio Jack Subassembly
2	493660	Assy	Audio Volume Control Subassembly
2	493662-1	Assy	Potentiometer Subassembly
2	493662-2	Assy	Potentiometer Subassembly
2	493671	Assy	Front Panel Flex Cables
1	493700	Assy	Rear Panel
2	493700TP	TP	Rear Panel
2	493701	Sch	Rear Panel
2	493705	Assy	Fan Subassembly
3	493706	Assy	Modified Fan Subassembly
3	493707	Mod	Modified Fan Screen
3	493708	Mod	Modified Fan Standoff
2	493710	Assy	Power Supply Subassembly
3	493722	Det	Power Supply PCB Subassembly
3	493730	Spec	Power Transformer
3	493885	Det	Power Supply Subassembly Heat Sink
3	493890	Det	Power Transformer Retainer
3	493891	Det	Power Transformer Insulator

Table 6-1: Indentured Drawing List (Contd)

Indent Level	Part Number	Type	Title
2	493750	Assy	Rear Panel Flex Cables
2	493755	Assy	Rear Panel Semi-Rigid Cable
2	493880	Det	Rear Panel
2	493886	Det	Spacer/Standoff
1	493800	Det	Cover

6.3 Supplied Assembly Drawings and Parts Lists

Assembly drawings usually have assocated with them a parts list, using the same part number. An assembly document can also consist of a parts list without a drawing. A list of the document numbers provided is given in table 6-2.

Table 6-2: List of Supplied Assembly Drawings and Parts Lists

Assembly	Part Number	Title
Top	493000	Top Assembly
A1	493050	Cardcage
--	493055	Flex Cable Harness Subassembly
--	493057	Semi-Rigid Cable Harness Subassembly
A1A20	493060	Backplane Subassembly
--	493065	Microwave RF Module Power Cable Subassembly
A1A1	493100	Microwave RF Module
A1A1A2	493130	Input Converter Subassembly
A1A1A1	493135	Input Limiter Subassembly
A1A1A3	493140	1450 MHz Prefilter Subassembly
A1A1A4	493150	1450 - 550 MHz Converter Subassembly
A1A1A6	493170	550 - 21.4 MHz Converter Subassembly
A1A5	493180	Low Frequency RF Module

Table 6-2: List of Assemblies and Parts Lists (Contd)

Assembly	Part Number	Title
A1A2	493190	Preselector Module
A1A2A1	493193	530 MHz Phase Locked Loop Subassembly
A1A6	493200	21.4 MHz IF Amplifier Module
A1A8	493250	21.4 MHz IF Filter Module
A1A17	493300	Microwave Synthesizer Module
--	493310	Microwave Synthesizer PROM Subassembly
A1A15	493330	Fixed LO Synthesizer Module
A1A15A1	493335	21.4 MHz VCO Subassembly
A1A16	493350	Low Frequency Synthesizer Module
A1A16A1, A2	493355	21 - 38 MHz VCO Subassembly
A1A16A3	493360	DDS Filter Subassembly
A1A9	493400	Video Module
A1A11	493500	DCIF Module
A2	493600	Front Panel
--	474243	Tuning Control Subassembly
--	493655	Power Switch Subassembly
--	493657	Audio Jack Subassembly
--	493660	Audio Volume Control Subassembly
--	493662	Potentiometer Subassembly
--	493671	Front Panel Flex Cable Subassembly
A2A1	493620	Switch/Display PCB Subassembly
--	493623	Pushbutton Switch Subassembly
--	493626	Button Engraving Subassembly
A2A2	493630	Interface PCB Subassembly
A2A3	493640	Processor Subassembly
--	493645	Processor EPROM Subassembly

Table 6-2: List of Assemblies and Parts Lists (Contd)

Assembly	Part Number	Title
--	493607	Front Panel Bulkhead Subassembly
A2A4	493650	X Axis/Audio Amplifier PCB Subassembly
--	493675	RF Input Attenuator Subassembly
--	493677	RF Relay Subassembly
--	493670	Front Panel Semi-Rigid Cable Subassembly
A3	493700	Rear Panel
--	493705	Fan Subassembly
A3A1	493710	Power Supply Subassembly
--	493750	Rear Panel Flex Cable Subassembly
--	493755	Rear Panel Semi-Rigid Cable Subassembly

6.4 Supplied Schematics

Schematics are drawn using Schema schematic capture software, so that they follow a combination of Schema's and DSI's standards. Standard nomenclature is shown in table 6-3. A list of schematics provided is shown in table 6-4.

Table 6-3: Schematic Nomenclature

Designation	Component
C	Capacitor
CR	Diode, Rectifier
E	Terminal
FBC	Ferrite Bead Choke
J	Connector, Socket
K	Relay
L	Inductor
P	Connector, Plug
Q	Transistor
R	Resistor, Potentiometer
S	Switch
SAT	Select at Test
SP	Speaker, Piezo Transducer
T	Transformer
TM	Thermistor
U	Integrated Circuit
VR	Metal Oxide Varistor
W	Jumper
Y	Crystal

Table 6-4: List of Schematics

Assembly	Part Number	Title
Top	493001	Top Level
A1	493051	Cardcage
A1A20	493061	Backplane Subassembly
A1A1	493101	Microwave RF Module
A1A5	493181	Low Frequency RF Module
A1A2	493191	Preselector Module
A1A6	493201	21.4 MHz IF Amplifier Module
A1A8	493251	21.4 MHz IF Filter Module
A1A17	493301	Microwave Synthesizer Module
A1A15	493331	Fixed LO Synthesizer Module
A1A16	493351	Low Frequency Synthesizer Module
A1A16A1, A2	493356	21 - 38 MHz VCO Subassembly
A1A9	493401	Video Module
A1A11	493501	DCIF Module
A2	493601	Front Panel
A2A1	493621	Switch/Display PCB Subassembly
A2A2	493631	Interface PCB Subassembly
A2A3	493641	Processor PCB Subassembly
A2A4	493651	X Axis/Audio Amplifier PCB Subassembly
A3	493701	Rear Panel

APPENDIX A. IEEE-488 INTERFACE PROTOCOL

A.1 Introduction

The R-110 receiver can use its IEEE-488 interface in either of two modes. In one mode it uses the interface to control an external R-1180 microwave downconverter. In the other mode it may be remotely controlled by a host computer. These two modes are mutually exclusive -- only one mode may be operative at a time. Thus if both an MDC and a host computer are present on the interface at the same time, the host computer must then control the MDC directly, not through the receiver.

This document deals with the command codes used by the host computer to command the receiver, and the formats of any required responses. An attempt is being made to conform to the IEEE-488.2 standard, in a limited way. While all of the "mandatory" features should eventually be implemented, few of the "optional" ones are anticipated. In addition, of the many data formats supported by the spec, only a few will be recognized by the radio, typically one specific format per command.

A.2 Receiver Addressing

The address of the receiver is set by a dipswitch on the processor PCB. It may be changed either by resetting the dipswitch and cycling power or reset, or may be changed (in local mode) using the front panel controls. The default DSI-standard address setting for the receiver is 16.

A.3 General Command Formats

Two general command formats are supported: the commands relating to the radio's settings, and a list of common commands identified in the '488.2 spec. The commands in the first list have in common a header consisting of a number of purely alphabetic characters (plus digits and underscores after the first character), whereas those in the second list begin with an asterisk followed by three alphabetic characters. Not included in this list are the low-level "bus messages" of the '488.1 spec (e.g., address-to-listen). Command headers are case-insensitive.

Following the header, the setting commands will typically contain a parameter field or a question mark. A specified parameter is the setting to be applied to the receiver, while a question mark indicates a query by the host for the receiver's current value of the setting specified by the header. In response to a query the receiver will respond with its current value of the desired setting, using a more precise form of the command's data format, minus the header.

Embedded within commands there may be "whitespace", defined as non-printing and blank characters. Length of whitespace in commands is arbitrary, since it is ignored by the receiver other than where at least one whitespace character is required by the '488.2 spec.

A.4 Data Formats

Decimal numeric data can be supplied in integer, decimal, or exponential format, as specified by '488.2. Units identifiers, such as "MHz", while made optional by '488.2, are not recognized by the radio. Hexadecimal data is in hex integer format, preceded by "#H". Both upper and lower case are acceptable for A - F and H. String data is mostly "mnemonic" format, which means upper or lower case letters, numbers, and the underscore, with the first character required to be alphabetical. There is also an instance of arbitrary length ASCII data, terminated with newline in conjunction with EOI.

A.5 Whitespace

'488.2 defines whitespace as the ASCII characters in the ranges 00 - 09 and 0B - 20 hex. They may be present in groups of arbitrary length. These characters are not processed by the receiver, but rather are skipped over, except where at least one whitespace character is required in a particular place by a particular command form.

A.6 Message Separator

The semicolon (";") is specified as the message separator by '488.2. Messages containing more than one command or query use this character to separate the pieces. Response messages also use the character to delimit responses from different queries.

A.7 Data Separator

The comma (",") is specified as the data separator by '488.2. It is used to delimit individual parameters or data within a single command, query, or response. Commas can be preceded or followed by whitespace in commands, but not in responses.

A.8 Compound Command Headers

The use of multiple command header mnemonics, separated by ":" characters, is not implemented in the receiver.

A.9 Message Terminator

The EOI line may be used without ATN to indicate the end of a message. (Used with ATN it forces a parallel poll.) So can a newline character (ASCII linefeed). '488.2 requires the receiver to recognize any combination of newline and EOI as a message terminator. The terminator may be preceded by whitespace. In order to conserve bytes the receiver will simply assert EOI with the last byte of data in a response message, foregoing the newline character entirely. The exception is when the response is in "arbitrary ASCII", which requires that the string be terminated with both the newline and EOI.

A.10 Low Level Interface Functions

The IEEE-488.1 interface spec lists a number of available low-level functions and capabilities. Many of these have associated with them a "capability level" which can range from no capability to full implementation, and may in some cases provide for partial capability in which some but not all of the function is available. A description of the '488.1 functions and the R-110's implementation of them is provided in the following paragraphs.

A.10.1 Source Handshake

This allows the radio to send data on the interface. The radio is fully capable of doing this. The capability code is SH1.

A.10.2 Acceptor Handshake

This allows the radio to receive data on the interface. The radio is fully capable of doing this. The capability code is AH1.

A.10.3 Talker Function

This allows the radio to be placed in talker mode so that it may send data on the bus. Sixteen capability levels are defined by '488.1, but only four are acceptable to '488.2. The radio supports the T6 capability level, which means that it can handle serial polls and that it leaves talker mode automatically when addressed to listen. It does not support "talk only" in remote, since it must be commanded to talk by an external controller. (In MDC mode it supports "talk only" as part of the control sequence.) It does not support extended or dual primary addressing.

A.10.4 Listener Function

This allows the radio to be placed in listener mode so that it may receive data on the bus. Eight capability levels are defined by '488.1, but only four are acceptable to '488.2. The radio supports the L4 capability level, which means that it will automatically leave talker mode if addressed to listen. It does not support "listen only" in remote, since it must be commanded to listen by an external controller. (In MDC mode it supports "listen only" as part of the control sequence.) It does not support extended or dual primary addressing.

A.10.5 Service Request Function

This allows the radio to signal the host that it needs attention, using a dedicated control line on the bus which is shared by all connected devices. '488.1 requires that the host respond to a service request with a serial poll. '488.2 makes elaborate use of this interface and requires full capability, which the radio supports. The capability code is SR1.

A.10.6 Remote/Local Function

This allows the radio to be placed in remote and returned to local. There is also the option of recognizing commands to lock out either remote or local. '488.2 requires either no or full capability, including lockouts. The radio supports full capability, for which the code is RL1.

A.10.7 Parallel Poll Function

This allows several devices on the bus to respond to polling by the host simultaneously, each having been previously assigned one bus data line, with no sharing. It is not a response to the service request function. Line assignment can either be done in hardware in the responding device, or may be assigned by the host via a command. '488.2 requires either no capability or remote assignment. The radio does not support parallel polling, for which the capability code is PP0.

A.10.8 Device Clear Function

This causes the radio's interface to be cleared. Both selective and universal commands are provided by '488.1, but '488.2 requires full capability, which includes both. The capability code is DC1.

A.10.9 Device Trigger Function

This provides a synchronization signal from the host so that several devices on the bus can perform activities simultaneously. What those activities are depends on the particular device, but are expected to be associated with the devices function rather than with the interface. '488.2 does not require the capability for its basic set of operations, and so it is not implemented in the R-110. The capability code is DT0.

A.10.10 Controller Function

This allows a device to either control the bus from the outset or to have control passed to it later. Of the 28 capability levels defined by '488.1 only five are supported by '488.2. The radio is not a controller during remote operation, giving it no capability, for which the code is C0. (In MDC mode it is in control of the bus, however. This one reason why MDC mode and remote mode are mutually exclusive.)

A.10.11 Electrical Interface

Certain interface lines may be either three-state or open-collector. Both configurations are allowed by '488.2. The radio uses three-state drivers where possible, for which the capability code is E2.

A.10.12 Capability Level Summary

In summary, the radio's capability levels are:

- SH1
- AH1
- T6
- L4
- SR1
- RL1
- PP0
- DC1
- DT0
- C0
- E2

A.10.13 Interface Clear Function

The IFC signal is given a dedicated line on the bus. It is used by the system controller to gain control back from any other device which maybe temporarily in charge. Since we're not a controlling device here, it doesn't really concern us.

A.10.14 EOI Function

The EOI signal is given a dedicated line on the bus. It is used to indicate the end of a message or as part of a parallel poll. '488.2 requires that either EOI or the ASCII linefeed be acceptable as an incoming message terminator, and that both be used at the end of a response message.

A.10.15 Serial Poll

Serial polling is required by '488.1, but its use is much more explicitly defined by '488.2. It consists of polling devices on the bus one by one. When polled, a device returns a full byte of data (as opposed to parallel polling, in which all devices respond simultaneously, each being typically assigned a single bit). One bit of the return byte (bit 6) specifies if the particular device being polled is currently asserting a service request. Of the other bits, some have specific uses required by '488.2 See the status register and event status register commands and queries in the section on common commands.

A.11 Common Commands and Queries

A list of common commands is explicitly defined by the '488.2 spec. Some are required by all compliant devices, while others are optional, but if provided must still comply with the descrption given in the spec. Required commands include:

- Identification query
- Reset command
- Self-test query
- Operation complete command and query
- Wait to continue command
- Clear status command
- Standard event status enable command and query
- Standard event status query
- Service request enable command and query
- Status query

Optional common commands supported by the R-110 include:

- Save settings
- Recall settings

Command mnemonics, parameters and data, and all response data is in ASCII. In the following descriptions, strings enclosed in angle brackets (e.g. <*IDN?>) represent the string to be recognized or sent, minus the brackets. Alphabetical characters may be upper or lower case. Quote marks may be single or double as long as both starting and ending marks match. One sort may be enclosed in another sort without interference.

The '488.2 spec assumes that both commands/queries and responses may be accumulated in input and output buffers or queues, separated by semicolons. When the output buffer is emptied an ASCII linefeed, accompanied by EOI, is sent to indicate the end of the response message.

A.11.1 Identification Query

The identification query format is <*IDN?>. The response from the receiver is single string in arbitrary ASCII format, comprised of the following fields, separated by commas:

Field 1:	manufacturer
Field 2:	model
Field 3:	serial number or <0>
Field 4:	firmware level or <0>

The string is terminated with a newline character in conjunction with EOI, and the whole thing must be fewer than 72 characters in length. The string termination requires that this query be the last operation before reading the output queue, or it and everything preceding it in the buffer will be wiped out by the next query.

A.11.2 Reset Command

The format is <*RST>. The action taken is to return the receiver to its powerup settings while maintaining it in remote mode.

A.11.3 Self Test Query

The format is <*TST?>. The action taken is to perform a self-test of the receiver. The response for a successful self-test is <0>. A not-so-successful self-test response is an NR1 optionally signed integer from -32767 to 32767, excluding 0. Currently there is no self-test implemented in the receiver, so the expected response is <0>.

A.11.4 Operation Complete Command and Query

The formats are <*OPC> and <*OPC?>. The command tells the receiver to set the "operation complete" bit in its standard event status register when the actions currently in process are completed. Since the receiver only does one thing at a time this should be the case immediately after the response to each incoming command.

The query causes the receiver to respond with an ASCII <1> when all current operations in process are completed. Since we only do one thing at a time the response is immediate.

A.11.5 Wait to Continue Command

The format is <*WAI>. This command causes the receiver to finish all operations currently in process before starting on anything new. It does this anyway, so the command is accepted but ignored.

A.11.6 Clear Status Command

The format is <*CLS>. Action taken is to clear all the status bits used for service requests and serial polls.

A.11.7 Standard Event Status Enable Command and Query

The formats are <*ESE data> and <*ESE?>, where the whitespace in the command is mandatory. The command provides an enable mask for the status register. Unmasked bits contribute to the generation of a summary bit which in turn forms part of the status register which generates service requests.

The format of the standard event status register is:

Bit 0: operation complete
Bit 1: request control
Bit 2: query error
Bit 3: device dependent error
Bit 4: execution error
Bit 5: command error
Bit 6: user request
Bit 7: power on

These bits are ANDed with the mask bits specified in the command and the results ORed to produce the ESB bit (bit 5) in the status byte register. Descriptions of the individual bits is as follows:

Operation Complete: normally cleared, set in response to the operation complete command after all in-process activities are completed.

Request Control: a request for transfer of control from the host. Not used.

Query Error: an attempt has been made to read response data from the receiver when none is available or pending, or response data has been lost.

Device Dependent Error: catch all for errors other than query errors, command errors, and execution errors. An example is a step command past the end of the available tuning range.

Execution Error: command data out of range or unavailable, or some current status of the receiver prevents the command from being implemented.

Command Error: command syntax error, or an unrecognized command, or a group execute trigger received in the middle of a message.

User Request: some special control available to the user is activated to signal the host. Not used.

Power On: indicates power has been cycled.

All of the foregoing bits are cleared after being read.

The command header <*ESE> is followed by whitespace, then by a decimal format number from 0 - 255, which when converted to binary forms the mask for the event status register bits.

The response to the query is an NR1 integer from 0 - 255, representing the mask byte currently in use.

A.11.8 Standard Event Status Query

The format is <*ESR?>. The response is an NR1 integer from 0 - 255 representing the current contents of the standard event status register defined above. The register is cleared after being read. The enable mask used for generation of the ESB bit is not applied to the response data.

A.11.9 Service Request Enable Command and Query

The formats are <*SRE data> and <*SRE?>. Function and formats are similar to the event status register command and query described above except that the mask is applied to the service request status byte and is used in the generation of the service request message. The service request status byte is returned in response to a serial poll.

The bits of the status byte, given above, are repeated here:

Bit 0: power supply fault
Bit 1: lock status fault
Bit 2: front overload
Bit 3: back overload
Bit 4: message available ('488.2)
Bit 5: event status ('488.2)
Bit 6: service requested ('488.1)
Bit 7: (unassigned)

Program data is a decimal number from 0 - 255 which forms the current mask. Note that bit 6 of the enable mask is ignored, since bit 6 of the status byte is effectively the ORed combination of the other 7 bits. The response data is an NR1 integer from 0 - 63 or 128 - 191, indicating that bit 6 is always returned clear.

A.11.10 Status Query

The format is <*STB?>. The response is an NR1 integer from 0 - 255 representing the status byte defined in the preceding paragraph. The status register is not necessarily cleared after reading, and the mask used to enable service requests is not applied.

A.11.11 Store Settings Command

The format is <*SAV data>, where the whitespace is mandatory and <data> is the storage location number in decimal format. It can range from 0 - 99.

Currently the list of what is saved is as follows:

- tuned frequency
- scan start frequency
- scan stop frequency
- scan step size
- scan rate
- scan repeat mode (one-shot, unidirectional, bidirectional)
- tune step size (from selected tuning digit)
- tune mode (step or ramp)
- input attenuation
- reference input attenuation (for absolute gain calculation)
- input selection
- MDC attenuation
- MDC input selection
- input attenuation when exiting MDC mode
- input selection when exiting MDC mode
- bandwidth
- bandwidth normal/extended selection
- reference bandwidth (for absolute gain calculation)
- wideband selection
- gain
- gain distribution in BFO
- gain distribution otherwise
- gain reference (for absolute gain calculation)
- absolute gain mode select
- delta gain mode select
- AGC select
- autorange select
- log/lin select
- Z axis select
- Z axis invert select
- BFO select
- pulse stretch enable (for future implementation)
- slideback enable (for future implementation)

- tune stored step size select
- scan pause resume select (continue or revert)
- GPIB enable
- MDC enable
- limit beep enable
- error beep enable
- fault beep enable

The state is saved to temporary storage in the radio, so that it is lost when power is removed. Note that the radio treats the store and recall bus commands just like the front panel operations, using the same storage locations. This means that settings stored in local may be recalled in remote and vice versa. It also means that some settings which are always disabled in remote are nevertheless stored and recalled by the interface commands.

A.11.12 Recall Settings Command

The format is <*RCL data>, where the whitespace is mandatory and <data> is the storage location number in decimal format. It can range from 0 to 99 for accessing temporary storage and -0 to -99 for permanent storage.

What gets recalled and loaded into active storage (and hardware) is listed in the description of the store command above.

A.12 Device-Specific Commands and Queries

Commands and queries specific to the receiver include:

- tuned frequency
- tuning step size
- tuning step up/down
- signal input select
- input attenuation
- IF bandwidth
- wide bandwidth
- gain
- gain distribution
- IF attenuation
- lin/log detection
- query all settings
- gain table initialization
- end-to-end gain initialization
- DCIF fixed gain initialization

Except for "query all settings" and the step up and down commands, each item provides both a command and a query. Descriptions of each are given in the following paragraphs.

A.12.1 Frequency Tuning Command and Query

Tuned frequency can range from 1 kHz to 1 GHz. The format of the command is <FREQ data>, where the whitespace is mandatory and <data> is in decimal format with resolution as needed down to 0.1 Hz. The number specified will be interpreted as Hz.

The query has the format <FREQ?>. The response is returned in NR3 exponential format, in Hz, with no header.

Note: the minimum legal tuned frequency in wideband mode is 15 MHz.

A.12.2 Frequency Tuning Step Size Command and Query

Step size can range from 0.1 Hz to 1 GHz, although the upper bound is provided for compatibility rather than for practical use. The receiver can tune to 0.1 Hz accuracy all the way to 1 GHz although the display on its front panel loses digits on the right at higher frequencies.

The format of the command is <STEP data>, where the data is in decimal format, in Hz.

The format of the query is <STEP?>. The response is returned in NR3 exponential format, in Hz, with no header.

Note: the minimum step size in wideband mode is 5 MHz, and must be a multiple of 5 MHz. Step size commands will be accepted bearing other values, and steps will be implemented to the nearest 5 MHz value. Queries will be responded to with the value commanded.

A.12.3 Frequency Tuning Step Up and Down Commands

This command adds or subtracts the current value of tuning step size to/from the currently tuned frequency. There are two commands, <STEPUP> and <STEPDN>.

In wideband mode the lower tuning limit becomes 15 MHz and the step size granularity is 5 MHz. If a step size which is not an integer multiple of 5 MHz is used then stepping will not proceed smoothly, since the step size provided will be added to/subtracted from the current tuned frequency and stored, but will be truncated to the next lower 5 MHz value before being applied to hardware.

A.12.4 RF Input Select Command and Query

The format of the command is <INP data>, where the whitespace is mandatory and the data is in decimal format, and must evaluate to 1 or 2. The query is <INP?>. The response is <1> or <2>, with no header. Input 1 is the upper RF input connector and input 2 is the lower.

A.12.5 RF Input Attenuation Command and Query

The format of the command is <ATTN data>, where the whitespace is mandatory and the data is in decimal format, ranging from 0 to 70 in steps of 10. The query is <ATTN?>. The response is an NR1 integer 0 to 70 in steps of 10, with no header.

A.12.6 IF Bandwidth Command and Query

The format of the command is <BW data>, where the whitespace is mandatory and the data is in decimal format. The command for wideband is the specific form <BW WIDE> where the whitespace is mandatory and the string is case-insensitive. The query is <BW?>. The response is in NR3 exponential format or <WIDE>, with no header.

Command data must evaluate to one of the legal bandwidths:

15 MHz	4 MHz
1 MHz	300 kHz
80 kHz	20 kHz
16 kHz	12.5 kHz
10 kHz	8 kHz
6.4 kHz	5 kHz
4 kHz	3.2 kHz
2.5 kHz	2 kHz
1.6 kHz	1.25 kHz
1 kHz	800 Hz
640 Hz	500 Hz
400 Hz	320 Hz
250 Hz	200 Hz

A.12.7 IF Gain Command and Query

The format of the IF gain command is <GAIN data>, where the whitespace is mandatory and the data is in decimal format, representing a number of dB from 0 - 50, to 0.1 dB resolution. The command can also take the specific form <GAIN AGC> in which the whitespace is mandatory and the string is case-insensitive. The query is <GAIN?>. The response is in NR2 decimal format or <AGC>, with no header.

Note: the IF gain stages are unused in wideband mode. It is the responsibility of the host to deal with this. Gain commands will be accepted, and queries responded to, even though the signal path bypasses the stage. If a switch is then made to narrowband then the commanded gain will be applied.

A.12.8 IF Gain Distribution Command and Query

The formats of the gain distribution commmand are <DIST IMP> and <DIST CW> where the whitespace is mandatory and the strings are case-insensitive. The query is <DIST?>. The response is <IMP> or <CW>.

A.12.9 Detector Selection Command and Query

The formats of the command are <DET LIN> and <DET LOG> where the whitespace is mandatory and the strings are case-insensitive. The query is <DET?>. The response is <LIN> or <LOG>.

A.12.10 Query All Settings

The query is <INFO?>, while the response is formatted as follows, with commas between fields:

Field 1:	tuned frequency, in NR3 exponential format
Field 2:	tuning step size, in NR3 exponential format
Field 3:	input selection, <1> or <2>
Field 4:	input attenuation, NR1 integer multiple of 10 from 0 - 70
Field 5:	IF gain, NR2 decimal from 0 - 50 with 0.1 resolution, or <AGC>
Field 6:	IF gain distribution, <IMP> or <CW>
Field 7:	IF bandwidth, NR3 exponential format or <WIDE>
Field 8:	detector selection, <LIN> or <LOG>

There are no headers in the response fields.

A.12.11 IF Attenuation Command and Query

Programmable gain in the IF is normally handled by the IF gain command described above. That command includes a gain value which indexes a gain distribution table (which may be selected using the gain distribution command) which contains dB values for the first two attenuator circuits in the IF. Each of these dB values is used as an index into separate linearization tables which in turn provide the attenuator settings as binary codes. Meanwhile, the third attenuator circuit is handled separately as end-to-end gain compensation. It also passes through a linearization table, but the setting is determined by tuning band rather than gain setting. The IF attenuation command described here, in contrast to the gain command and end-to-end compensation, bypasses all of the tables and applies data passed with the command directly to the driver circuits. Note that in doing so the receiver will lose knowledge of its actual gain setting, since it bases that value on the value used to address the distribution table and the end-to-end linearization table.

The format of the command is <IATN data , data , data>, where the first whitespace is mandatory and the rest optional, and the data is 12 bits each of binary in hexadecimal format (for example <#H123,#H456,#H789>). Alphabetical characters in hexadecimal format are case-insensitive. The query is <IATN?>. The response is <data,data,data>, again in hexadecimal format. For both the command and the query the first value given is what is applied to the first attenuator in the IF signal path.

A.12.12 End-to-End Gain Command and Query

End-to-end gain is established by the last attenuator circuit in the IF. It is a fixed value for each of the three main tuning bands (1 - 250 KHz, 250 KHz - 15 MHz, 15 MHz - 1 GHz). The value is in dB to 0.1 dB resolution and can range from 0 - 17.5 dB. The intent is to establish a standard end-to-end gain for all receivers, given the same IF gain, input attenuation, bandwidth, detector, and AGC settings.

The format of the command is <EATN data1 , data2 , data3>, where the first whitespace is mandatory and the rest optional, and data is in decimal format for bands 1, 2, and 3 respectively. The query is <EATN?>. The response is <data1,data2,data3> in NR2 decimal format. Command data is stored in nonvolatile memory and becomes part of the gain calibration of the radio. The data which pertains to the current tuning band is also applied to hardware.

A.12.13 DCIF Fixed Gain Command and Query

The end-to-end gain compensation circuit described in the preceding paragraph may be bypassed when the DCIF is in use. The DCIF, in addition to its own fixed gain and bandwidth-compensating gain requirements, must also handle its own end-to-end gain compensation. The required value depends both on the current tuning band, as it did in the IF circuit, but also upon whether log or linear detection is selected. Note that the DCIF is controlled by programmable amplifiers rather than attenuators, so it uses gain values rather than attenuation.

The format of the command is <DCGNdb data , data> where the first whitespace is mandatory and the rest optional, the <d> is <LN> for linear or <LG> for log, <b> is <1>, <2>, or <3> for band, and the data is in decimal format, in dB of gain to 0.1 dB resolution, for the first and second DCIF programmable amplifiers, respectively. The values passed are for combined fixed and end-to-end compensating gain. The query is <DCGNdb?> with the same use of <d> and <b> as before. The response is <data,data> in NR2 decimal format, representing combined fixed and end-to-end gain for the first and second amplifiers respectively.

Command data is stored in nonvolatile memory and becomes part of the receiver's calibration. If the command specification matches the current tuning band and detector selection then the data is also applied to hardware.

A.12.14 IF Attenuation Linearization Table Command and Query

IF gain and end-to-end gain are set by means of PIN diode attenuator circuits. There are three of these in series, with intervening amplifiers and filters. The first is a double circuit connected to a single driving function, so the first circuit affords twice the attenuation range of either of the other two. Drive requirements for these circuits are fairly nonlinear, and vary significantly from unit to unit as well, so tables have been implemented which convert a desired attenuation in dB into a digital code which is used to drive a given attenuator circuit. The tables give values for every 0.2 dB from 0 - 35 dB for the first circuit, and every 0.1 dB from 0 - 17.5 dB for the other two. The first table value is for baseline zero attenuation, ranging up to maximum attenuation at the other end. Table values are 12 bits long each (although the prototype receivers only use the first eight).

Note that baseline zero attenuation does not necessarily need to measure zero for any particular attenuator circuit. In fact it may be preferable to give up a dB or so initially in order to avoid the very nonlinear knee at turnon, and then make up the difference in the end-to-end compensation. The eventual distribution of gain is the determined by a combination of the impulsive and CW gain distribution tables, the linearization tables, and the end-to-end compensating gains for both the IF and the DCIF. While the distribution tables are not currently modifyable, the rest must be set up by a properly written calibration algorithm and test procedure, which is not described in this document.

The command is <ATBLx index , data[, ...]>, where <x> can be <1>, <2>, or <3> to indicate which table, <index> is a decimal number from 0 - 175 indicating the table record number, and <data> is 12 bits in hexadecimal format, for example <#H123>. The alphabetical characters in hexadecimal format are case-insensitive. Data supplied after the first value will be set into subsequent consecutive entries in the table. In this manner, starting with 0, the entire table may be initialized with a single command. The query is <ATBLx? index>, where the whitespace is again mandatory and <x> and <index> are the same as for the command. The response is the same hexadecimal data. A special case of the query is <ATBLx? ALL>, where the whitespace is mandatory and the string is case-insensitive. The response to this query is the entire contents of the table starting with 0, with the entries separated by commas.

APPENDIX B. HARDWARE ADDRESS MAP

B.1 Introduction

The R-110 uses an 80C31 microprocessor. This part supports two external address spaces, one for instructions and one for data. Data addresses are read/write, while instruction addresses are read only. Each address space may be up to 64k bytes (65536 locations, each eight bits wide) in size, using sixteen address bits. The board (A2A3) which contains the processor also provides configuration jumpers which makes it possible to merge the upper half of each space for common access, or to keep them totally separate. When merged, instructions may be downloaded from an external source and written into memory as data, and then executed as instructions. As currently implemented the upper halves are merged, but when code size exceeds 32k the other configuration will be required.

This memory map shows how hardware in the radio is allocated to the two address spaces in the merged configuration. In the separated configuration everything remains the same except that the instruction address space is devoted exclusively to the EPROM.

B.2 I/O Configuration

The address decoding hardware on the processor board (A2A3) allocates a segment of 256 data addresses for I/O functions (everything else is some sort of memory). A physical I/O bus is implemented, leading to the interface board (A2A2) and from there to the displays on the display board (A2A1) and the cardcage backplane (A1A20), where the various cardcage boards can connect to it. In this appendix the allocation of the I/O bus will be indicated in the main data address map and then will be given its own map, using eight bit addresses. To determine the address the processor uses to access a particular address on the I/O bus, preface the I/O address with 7F(hex).

B.3 Hexadecimal Addressing

Addresses dealt with here are either eight or sixteen bits long. The number system which best lends itself to binary numbers of this size is hexadecimal, which is base 16. In this system numbering begins with zero through nine, and continues to the equivalent of fifteen with the first three letters of the alphabet. Either upper or lower case letters are permitted.

For example:

0(hex) = 0(decimal)
9(hex) = 10(decimal)
A(hex) = 10(decimal)
F(hex) = 15(decimal)
10(hex) = 16(decimal)
1F(hex) = 31(decimal)
20(hex) = 32(decimal)
FF(hex) = 255(decimal)
100(hex) = 256(decimal)
FFFF(hex) = 65535(decimal)

B.4 Code Address Map

Address 0000(hex) - 7FFF(hex) = EPROM (fixed instruction memory)

Address 8000(hex) - FFFF(hex) = RAM (volatile data or instruction memory)

Note: in non-merged configuration the entire code address space, 0000(hex) - FFFF(hex) is assigned to EPROM, and RAM is unavailable for execution of instructions.

B.5 Data Address Map

Address 0000(hex) - 7EFF(hex) = EEPROM (nonvolatile data memory)

Address 7F00(hex) - 7FFF(hex) = I/O bus (see separate map)

Address 8000(hex) - FFFF(hex) = RAM (volatile data or instruction memory)

Note: in non-merged configuration the RAM space is not usable as instruction memory.

B.6 I/O Bus Address Map

These are the 256 addresses identified as the I/O bus in the preceding paragraph. They are listed with eight bit addresses. The full address is the eight bit addressed prefaced by 7F(hex), for example, I/O address 80(hex) = data address 7F80(hex).

For a particular I/O address, the hardware peripheral assigned to it may allocate specific data bits for different purposes. Bit allocations will be given for those addresses which require it. As listed, bit zero is the least significant bit on the data bus, while bit 7 is the most significant.

In some instances there is redundant mapping. This means that a single hardware peripheral port was mapped into multiple (contiguous) addresses on the I/O bus. This is normally done to simplify the design of the decoding hardware. It wastes addresses, but at present there is a surplus. Peripheral ports which are redundantly mapped may be accessed through any of the assigned addresses, with no difference in effect between one and another.

In addition, some notes pertaining to the states of the bits are often provided.

Since the overall map is fairly extensive it will be presented in pieces according to the assemblies associated with it. The first half of the address space is allocated to the cardcage cards. All of these addresses are therefore write only, since no provision is made for reading from the cardcage. The upper half of the address space is allocated to the front panel assembly, and may be either written to or read from.

B.6.1 Low Frequency Synthesizer Module (A1A16)

This board uses the Qualcomm Q2334 direct digital synthesizer (DDS). It contains two separate but identical synthesizer circuits. See the manufacturer's application notes for more information.

Address 00(hex) - 1F(hex) = Q2334 direct digital synthesizer (write only)
Address 00(hex) = synthesizer #1 phase increment latch A bits 0 - 7
Address 01(hex) = synthesizer #1 phase increment latch A bits 8 - 15
Address 02(hex) = synthesizer #1 phase increment latch A bits 16 - 23
Address 03(hex) = synthesizer #1 phase increment latch A bits 24 - 31
DDS frequency in Hz = phase increment code / 214.7483648
Address 04(hex) = synthesizer #1 phase increment latch B bits 0 - 7
Address 05(hex) = synthesizer #1 phase increment latch B bits 8 - 15
Address 06(hex) = synthesizer #1 phase increment latch B bits 16 - 23
Address 07(hex) = synthesizer #1 phase increment latch B bits 24 - 31
Address 08(hex) = synthesizer #1 synchronous mode control latch
Address 09(hex) = reserved by Q2334
Address 0A(hex) = synthesizer #1 asynchronous mode control latch
Address 0B(hex) = reserved by Q2334
Address 0C(hex) = synthesizer #1 accumulator reset
Address 0D(hex) = reserved by Q2334
Address 0E(hex) = synthesizer #1 asynchronous hop clock
Address 0F(hex) = reserved by Q2334
Address 10(hex) = synthesizer #2 phase increment latch A bits 0 - 7
Address 11(hex) = synthesizer #2 phase increment latch A bits 8 - 15
Address 12(hex) = synthesizer #2 phase increment latch A bits 16 - 23
Address 13(hex) = synthesizer #2 phase increment latch A bits 24 - 31
Address 14(hex) = synthesizer #2 phase increment latch B bits 0 - 7
Address 15(hex) = synthesizer #2 phase increment latch B bits 8 - 15
Address 16(hex) = synthesizer #2 phase increment latch B bits 16 - 23
Address 17(hex) = synthesizer #2 phase increment latch B bits 24 - 31
Address 18(hex) = synthesizer #2 synchronous mode control latch
Address 19(hex) = reserved by Q2334
Address 1A(hex) = synthesizer #2 asynchronous mode control latch
Address 1B(hex) = reserved by Q2334
Address 1C(hex) = synthesizer #2 accumulator reset
Address 1D(hex) = reserved by Q2334
Address 1E(hex) = synthesizer #2 asynchronous hop clock
Address 1F(hex) = reserved by Q2334

Data to the asynchronous hop clock is unimportant, since the write strobe acts as a trigger to the IC. The control latch for the phase locked loop which operates in conjunction with the DDS is also mapped to this address, and the data written is used to set the PLL frequency. In this manner, both parts of the synthesizer can be updated at the same time.

Address 0E(hex) = back end phase locked loop control latch (write only)
Bits 0 - 5 = phase locked loop divide code
Frequency in MHz = code + 1, from 19 - 38 MHz
Bits 6 - 7 = tuning band select code
Code 0 = band 1 select
Code 1 = band 2 select
Code 2 = band 3 select
Code 3 = unused

B.6.2 DCIF Module (A1A11)

Address 40(hex) - 43(hex) = DCIF timebase counter-timer (write only)
Address 40(hex) = counter-timer circuit 0 data
Address 41(hex) = counter-timer circuit 1 data
Address 42(hex) = counter-timer circuit 2 data
Address 43(hex) = counter-timer mode

The DCIF timebase counter-timer is an 82C54, available from several manufacturers. See their application notes for more information.

Address 44(hex) = DCIF I channel gain control DAC #1 low data (write only)
Bits 0 - 7 = DCIF I channel gain control DAC #1 bits 0 - 7
Address 45(hex) = DCIF I channel gain control DAC #1 high data (write only)
Bits 0 - 3 = DCIF I channel gain control DAC #1 bits 8 - 11
Bits 4 - 7 = spare

Address 46(hex) = DCIF Q channel gain control DAC #1 low data (write only)
Bits 0 - 7 = DCIF Q channel gain control DAC #1 bits 0 - 7
Address 47(hex) = DCIF Q channel gain control DAC #1 high data (write only)
Bits 0 - 3 = DCIF Q channel gain control DAC #1 bits 8 - 11
Bits 4 - 7 = spare

Address 48(hex) = DCIF I channel gain control DAC #2 low data (write only)
Bits 0 - 7 = DCIF I channel gain control DAC #2 bits 0 - 7
Address 49(hex) = DCIF I channel gain control DAC #2 high data (write only)
Bits 0 - 3 = DCIF I channel gain control DAC #2 bits 8 - 11
Bits 4 - 7 = spare

Address 4A(hex) = DCIF Q channel gain control DAC #2 low data (write only)
Bits 0 - 7 = DCIF Q channel gain control DAC #2 bits 0 - 7
Address 4B(hex) = DCIF Q channel gain control DAC #2 high data (write only)
Bits 0 - 3 = DCIF Q channel gain control DAC #2 bits 8 - 11
Bits 4 - 7 = spare

Address 4C(hex) = DCIF control latch (write only)
Bit 0 = filter #1 and filter #3 clock ratio select
0 = 100:1
1 = 50:1
Bit 1 = filter #2 clock ratio select
0 = 150:1
1 = 75:1
Bit 2 = DCIF input select
0 = linear mode IF tap
1 = log mode IF tap
Bit 3 = clock receiver and overload status driver enable (set = enable)
Bits 4 - 7 = spare

Address 4D(hex) = DCIF gain control DAC load strobe (data unimportant) (write only)

B.6.3 21.4 MHz IF Amplifier Module (A1A6)

Address 50(hex) = IF gain control DAC #1 low data (write only)
Bits 0 - 7 = IF gain control DAC #1 bits 0 - 7
Address 51(hex) = IF gain control DAC #1 high data (write only)
Bits 0 - 3 = IF gain control DAC #1 bits 8 - 11
Bits 4 - 7 = spare

Address 52(hex) = IF gain control DAC #2 low data (write only)
Bits 0 - 7 = IF gain control DAC #2 bits 0 - 7
Address 53(hex) = IF gain control DAC #2 high data (write only)
Bits 0 - 3 = IF gain control DAC #2 bits 8 - 11
Bits 4 - 7 = spare

Address 54(hex) = IF gain control DAC #3 low data (write only)
Bits 0 - 7 = IF gain control DAC #3 bits 0 - 7
Address 55(hex) = IF gain control DAC #3 high data (write only)
Bits 0 - 3 = IF gain control DAC #3 bits 8 - 11
Bits 4 - 7 = spare

Address 56(hex) = IF gain control DAC #4 low data (write only)
Bits 0 - 7 = IF gain control DAC #4 bits 0 - 7
Address 57(hex) = IF gain control DAC #4 high data (write only)
Bits 0 - 3 = IF gain control DAC #4 bits 8 - 11
Bits 4 - 7 = spare

Address 58(hex) = gain control DAC load strobe (data unimportant) (write only)

Address 59(hex) = IF control latch (write only)
Bits 0 - 2 = bandwidth select code
Code 0 = 15 MHz bandwidth select
Code 1 = reserved for 8 MHz bandwidth select
Code 2 = 4 MHz bandwidth select
Code 3 = 1 MHz bandwidth select
Code 4 = 300 kHz bandwidth select
Code 5 = 80 kHz bandwidth select
Code 6 = spare
Code 7 = wideband select
Bit 3 = bandwidth enable (set = enable bandwidth selection)
Bit 4 = high/low band select
0 = high band
1 = low band
Bit 5 = band 1/2 select
0 = band 2
1 = band 1
Bit 6 = AGC enable (set = enable)
Bit 7 = spare

B.6.4 Fixed LO Synthesizer Module (A1A15)

Address 70(hex) = fixed oscillator and DCIF timebase control (write only)
Bit 0 = band 1 enable (set = enable)
Bit 1 = DCIF phase locked loop enable (set = enable)
Bits 2 - 7 = spare

Address 71(hex) = DCIF phase locked loop divider (write only)
Bits 0 - 7 = DCIF phase locked loop divider code
Frequency = (255 - code) * 50 kHz

B.6.5 Microwave Synthesizer Module (A1A17)

Address 78(hex) = microwave synthesizer skip counter (write only)
Bits 0 - 3 = microwave synthesizer skip counter code
Code = (frequency / 5 MHz) MOD 10
where "MOD" is the remainder from dividing by 10
Bit 4 = spare
Bit 5 = band 3 enable (clear = enable)
Bits 6 - 7 = spare

Address 79(hex) = microwave synthesizer divider (write only)
Bits 0 - 7 = microwave synthesizer divider code
Code = [(frequency / 5 MHz) DIV 10] - 1
where "DIV" is truncated integer division

B.6.6 Video Module (A1A9)

Address 7E(hex) = video control latch 0 (write only)
- Bit 0 = 4 MHz video filter enable (set = enable)
- Bit 1 = 400 kHz video filter enable (set = enable)
- Bit 2 = 40 kHz video filter enable (set = enable)
- Bit 3 = 4 kHz video filter enable (set = enable)
- Bit 4 = log detector input select
  - 0 = DCIF input
  - 1 = 21.4 MHz IF input
- Bit 5 = log/linear detector select
  - 0 = linear detector
  - 1 = log detector
- Bit 6 = video output select
  - 0 = processed 21.4 MHz IF
  - 1 = processed DCIF
- Bit 7 = spare

Address 7F(hex) = video control latch 1 (write only)
- Bit 0 = BFO enable (set = enable)
- Bit 1 = Z axis enable (set = enable)
- Bit 2 = Z axis invert (set = invert)
- Bit 3 = reserved for slideback enable
- Bit 4 = reserved for pulse stretch enable
- Bits 5 - 7 = spare

B.6.7 Processor PCB (A2A3)

Address 80(hex) - 83(hex) = dipswitch (redundant mapping) (read only)
- Bit 0 = switch #1 ("on" = 0, "off" = 1)
- Bit 1 = switch #2
- Bit 2 = switch #3
- Bit 3 = switch #4
- Bit 4 = switch #5
- Bit 5 = switch #6
- Bit 6 = switch #7
- Bit 7 = switch #8

Address 80(hex) - 83(hex) = external counter-timer interrupt request clear (redundant mapping) (write only) (data is unimportant to clearing the request, but is used by the other write function mapped here -- see below)

Address 80(hex) - 83(hex) = serial port receive data select (redundantly mapped) (write only) (this write address is also used by another write function -- see above)
- Bit 0 = data select
  - 0 = RS-232
  - 1 = serial data from cardcage
- Bits 1 = 7 = spare

Address 84(hex) - 87(hex) = external counter-timer ports
Address 84(hex) = counter-timer circuit 0 data (read/write)
Address 85(hex) = counter-timer circuit 1 data (read/write)
Address 86(hex) = counter-timer circuit 2 data (read/write)
Address 87(hex) = counter-timer status (read)
Address 87(hex) = counter-timer mode (write)

The external counter-timer is an 82C54, available from several manufacturers. See their application notes for more information.

Address 88(hex) - 8F(hex) = IEEE-488 controller ports
Address 88(hex) = interrupt request status 0 (read)
Address 88(hex) = interrupt mask 0 (write)
Address 89(hex) = interrupt request status 1 (read)
Address 89(hex) = interrupt mask 1 (write)
Address 8A(hex) = address status (read only)
Address 8B(hex) = bus status (read)
Address 8B(hex) = auxiliary command (write)
Address 8C(hex) = controller address (write only)
Address 8D(hex) = serial poll data (write only)
Address 8E(hex) = command pass-through (read)
Address 8E(hex) = parallel poll configuration (write)
Address 8F(hex) = data in (read)
Address 8F(hex) = data out (write)

The IEEE-488 controller is a Texas Instruments TMS9914A. See the manufacturer's application notes for more information.

B.6.8 Interface PCB (A2A2)

Address B0(hex) = LED latch 0 (write only)
Bit 0 = RF input indicator select
0 = RF input #1 select indicator
1 = RF input #2 select indicator
Bits 1 - 7 = spare

Address B1(hex) = LED latch 1 (write only)
Bit 0 = spare indicator (left end of attenuation display)
Bit 1 = autorange indicator
Bit 2 = AGC indicator
Bit 3 = absolute gain indicator
Bit 4 = delta gain indicator
Bit 5 = CW gain indicator
Bit 6 = wideband mode indicator
Bit 7 = spare indicator (right end of bandwidth display)

Address B2(hex) = LED latch 2 (write only)
Bits 0 - 3 = operating mode indicator code
Code 0(hex) = tune mode indicator
Code 1(hex) = start mode indicator
Code 2(hex) = stop mode indicator
Code 3(hex) = step mode indicator
Code 4(hex) = rate mode indicator
Code 5(hex) = scan mode indicator
Code 6(hex) = store mode indicator
Code 7(hex) = recall mode indicator
Code 8(hex) = GPIB mode indicator
Code 9(hex) = remote mode indicator
Codes A(hex) - F(hex) = spare
Bit 4 = select left indicator
Bit 5 = select step indicator
Bit 6 = select right indicator
Bit 7 = AC high indicator

Address B3(hex) = LED latch 3 (write only)
Bit 0 = AC low indicator
Bit 1 = DC regulation indicator
Bit 2 = unlock indicator
Bit 3 = front end overload indicator
Bit 4 = back end overload indicator
Bit 5 = bandwidth limit indicator
Bit 6 = step gap indicator
Bit 7 = downconverter mode indicator

Address B4(hex) = LED latch 4 (write only)
Bit 0 = reserved for slideback enable indicator
Bit 1 = reserved for pulse stretch enable indicator
Bit 2 = BFO enable indicator
Bit 3 = Z axis output enable indicator
Bit 4 = Z axis invert enable indicator
Bit 5 = alternate function select pending indicator
Bit 6 = reserved for alternate video detector enable indicator
Bit 7 = log video enable indicator

Address B5(hex) = rear panel status latch 0 (write only)
Bits 0 - 7 = rear panel processor status bits 0 - 7

Address B6(hex) = rear panel status latch 1 (write only)
Bits 0 - 7 = rear panel processor status bits 8 - 15

Address B7(hex) = front panel RF control latch (write only)
Bits 0 - 2 = input attenuation code
Code 0 = 0 dB
Code 1 = 10 dB
Code 2 = 20 dB
Code 3 = 30 dB
Code 4 = 40 dB
Code 5 = 50 dB
Code 6 = 60 dB
Code 7 = 70 dB
Bit 3 = reserved for GLI control
Bits 4 - 5 = RF input select code
Code 0 = no change
Code 1 = RF input #1 select
Code 2 = RF input #2 select
Code 3 = illegal
Bits 6 - 7 = high/low band select code
Code 0 = no change
Code 1 = band #1/2 select
Code 2 = band 3 select
Code 3 = illegal

Address B8(hex) = button buffer 0 (read)
Bits 0 - 3 = keypad code
Code 0(hex) = "C" key
Code 1(hex) = "M" key
Code 2(hex) = "K" key
Code 3(hex) = "H" key
Code 4(hex) = "." key
Code 5(hex) = "9" key
Code 6(hex) = "8" key
Code 7(hex) = "7" key
Code 8(hex) = "6" key
Code 9(hex) = "5" key
Code A(hex) = "4" key
Code B(hex) = "3" key
Code C(hex) = "2" key
Code D(hex) = "1" key
Code E(hex) = "0" key
Code F(hex) = no key
Bit 4 = select left key
Bit 5 = select step key
Bit 6 = select right key
Bit 7 = alternate function enable key
Address B8(hex) = X axis DAC low port and X axis DAC strobe(write)
Bits 0 - 7 = X axis DAC bits 0 - 7

Address B9(hex) = button buffer 1 (read)
- Bit 0 = RF input #1 select key
- Bit 1 = RF input #2 select key
- Bit 2 = attenuation up key
- Bit 3 = attenuation down key
- Bit 4 = bandwidth up key
- Bit 5 = bandwidht down key
- Bit 6 = tune up key
- Bit 7 = tune down key

Address B9(hex) = X axis DAC high port (write)
- Bits 0 - 3 = X axis DAC bits 8 - 11
- Bits 4 - 7 = spare

Address BA(hex) = button buffer 2 (read)
- Bit 0 = reserved for slideback enable key
- Bit 1 = reserved for pulse stretch enable key
- Bit 2 = BFO enable key
- Bit 3 = Z axis output enable key
- Bit 4 = Z axis invert enable key
- Bit 5 = reserved for alternate detector select key
- Bit 6 = log/linear detector select key
- Bit 7 = spare

Address BA(hex) = beep headphone volume DAC port (write)
- Bits 0 - 7 = beep headphone volume DAC bits 0 - 7

Address BB(hex) = shaft encoder buffer (read)
- Bit 0 = gain encoder direction (set = clockwise)
- Bit 1 = gain encoder rotation (set = new rotation detected)
- Bit 2 = tune encoder direction (set = clockwise)
- Bit 3 = tune encoder rotation (set = new rotation detected)
- Bits 4 - 7 = spare

Address BB(hex) = beep transducer volume DAC port (write)
- Bits 0 - 7 = beep transducer volume DAC bits 0 - 7

Address BC(hex) = cardcage status buffer 0 (read)
- Bit 0 = combined lock status (clear = all locked)
- Bit 1 = combined front end overload (clear = no overload)
- Bit 2 = combined back end overload (clear = no overload)
- Bit 3 = front end underload (clear = no underload)
- Bit 4 = spare
- Bit 5 = video overload (clear = no overload)
- Bit 6 = DCIF overload (clear = no overload)
- Bit 7 = IF overload (clear = no overload)

Address BC(hex) = short beep trigger (write) (data unimportant)

Address BD(hex) = cardcage status buffer 1 (read)
Bit 0 = RF overload (clear = no overload)
Bit 1 = variable MW synthesizer lock status (clear = locked)
Bit 2 = 2 GHz synthesizer lock status (clear = locked)
Bit 3 = 530 MHz synthesizer lock status (clear = locked)
Bit 4 = back end synthesizer lock status (clear = locked)
Bit 5 = mixer lock status (clear = locked)
Bit 6 = 21.4 MHz synthesizer lock status (clear = locked)
Bit 7 = DCIF timebase synthesizer lock status (clear = locked)
Address BD(hex) = long beep trigger (write) (data unimportant)

Address BE(hex) = power supply status buffer (read only)
Bit 0 = AC line high (clear = within tolerance)
Bit 1 = AC line low (clear = within tolerance)
Bit 2 = DC regulation (clear = all voltages within tolerance)
Bit 3 = spare power supply status
Bit 4 = spare cardcage status
Bit 5 = spare cardcage status
Bits 6 - 7 = spare

B.6.9 Switch/Display PCB (A2A1)

Addresses used by components on the display board are partly decoded by logic on the interface board (A2A2). The tuning displays are Siemens PD3535, 4 character alphanumeric LED displays. The other displays are Siemens PD2435, which are similar but smaller in size. See the manufacturer's application notes for more information.

Address C0(hex) - C7(hex) = tuning display 0 (the rightmost 4 characters)
Address C0(hex) - C3(hex) = control port (redundantly mapped) (read/write)
Address C4(hex) = character 0 port (rightmost of 4) (read/write)
Address C5(hex) = character 1 port (read/write)
Address C6(hex) = character 2 port (read/write)
Address C7(hex) = character 3 port (leftmost of 4) (read/write)

Address C8(hex) - CF(hex) = tuning display 1 (the middle 4 characters)
Address C8(hex) - CB(hex) = control port (redundantly mapped) (read/write)
Address CC(hex) = character 0 port (rightmost of 4) (read/write)
Address CD(hex) = character 1 port (read/write)
Address CE(hex) = character 2 port (read/write)
Address CF(hex) = character 3 port (leftmost of 4) (read/write)

Address D0(hex) - D7(hex) = tuning display 3 (the leftmost 4 characters)
Address D0(hex) - D3(hex) = control port (redundantly mapped) (read/write)
Address D4(hex) = character 0 port (rightmost of 4) (read/write)
Address D5(hex) = character 1 port (read/write)
Address D6(hex) = character 2 port (read/write)
Address D7(hex) = character 3 port (leftmost of 4) (read/write)

Address D8(hex) - DF(hex) = attenuation display (4 characters)
Address D8(hex) - DB(hex) = control port (redundantly mapped) (read/write)
Address DC(hex) = character 0 port (rightmost of 4) (read/write)
Address DD(hex) = character 1 port (read/write)
Address DE(hex) = character 2 port (read/write)
Address DF(hex) = character 3 port (leftmost of 4) (read/write)

Address E0(hex) - E7(hex) = gain display (4 characters)
Address E0(hex) - E3(hex) = control port (redundantly mapped) (read/write)
Address E4(hex) = character 0 port (rightmost of 4) (read/write)
Address E5(hex) = character 1 port (read/write)
Address E6(hex) = character 2 port (read/write)
Address E7(hex) = character 3 port (leftmost of 4) (read/write)

Address E8(hex) - EF(hex) = bandwidth display (4 characters)
Address E8(hex) - EB(hex) = control port (redundantly mapped) (read/write)
Address EC(hex) = character 0 port (rightmost of 4) (read/write)
Address ED(hex) = character 1 port (read/write)
Address EE(hex) = character 2 port (read/write)
Address EF(hex) = character 3 port (leftmost of 4) (read/write)

Address F0(hex) - FF(hex) = reserved for DVM display

B.6.10 Unused Addresses

The following segments of the I/O address space are currently unused. Note that that addresses 00(hex) - 7F(hex) are cardcage addresses, which are write-only. Some addresses, while not assigned in the memory map, are nevertheless decoded by hardware to the point where a card will be partly enabled. These addresses are omitted from this list.

Address 20(hex) - 3F(hex)

Address 60(hex) - 6F(hex)

Address 90(hex) - AF(hex)

Address B0(hex) - B7(hex) (only read is unused)

Address BE(hex) (only write is unused)

Address BF(hex)

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August 13, 1991

MAINTENANCE MANUAL
FOR THE
R-110 and R-110B RECEIVERS

THIS MANUAL IS INTENDED FOR USE WITH THE FOLLOWING SERIAL NUMBER:

_____

Dynamic Sciences International Inc.
6130 Variel Avenue
Woodland Hills, CA 91367
(818)226-6262 Fax:(818) 226-6247

SECTION 5. MAINTENANCE

5.1 Introduction

Three levels of maintenance are discussed in this section: preventive maintenance, periodic maintenance, and corrective maintenance. Periodic maintenance is part of preventive maintenance and includes a receiver performance test. Failure of a particular part of the performance test should lead to initiation of corrective maintenance, and will indicate a starting point for fault isolation. Isolation procedures are provided down to at least the module level. Disassembly procedures are also provided as an aid to service personnel.

Finally, field calibration procedures are included both for periodic maintenance and for replacement of failed assemblies. Procedures for adjustments which may be made at the factory before shipment and which should never need recalibration are not included.

5.2 Preventive Maintenance

Preventive maintenance includes correct installation and connection of the radio, periodic inspection and cleaning, and execution of the receiver performance test. See table 5-1.

The model R-110 receiver requires a minimum of periodic maintenance unless abusive conditions exist. Such conditions include improper handling, mounting, and operation, or environmental extremes.

5.2.1 Performance Test

The performance test consists of a procedure which, if followed all the way through, will demonstrate that the receiver is in good operating condition. The performance test makes no attempt to verify all specifications, as would an acceptance test procedure, but is rather intended to verify its basic operation. A full verification of the radio's specifications requires execution of the ATP.

Test equipment required by the performance test is listed in table 5-2. Receiver test points used by the performance test are indicated in figure 5-1. A sample data sheet for recording the results of the performance test is given in paragraph 5.2.1.2.15.

Field service adjustment procedures are provided at the end of this section.

Table 5-1: Preventive Maintenance

Task	Interval	Description
Inspect Cables	4 Months	Check for frayed cables and wires. Check that wires and coax cables are not crimped between structural members. Inspect connectors.
Inspect and clean air inlet filter	4 Months	Visually check for accumulated dirt; if excessive, remove dirt and other deposits with a vacuum cleaner or compressed air.
Inspect plug-in modules	12 Months	Look for discoloration of resistor and capacitor coding bands or loss of coating that would indicate abnormal operation such as extreme heat conditions.
Clean connectors	12 Months	Dissolve and wipe away any grease deposits on front and rear panel connectors. Use a cotton swab dipped in Freon TF or alcohol.
Clean chassis	12 Months	Wipe all dust and grease from the interior and exterior chassis parts.
Execute performance test and alleviate any identified faults	12 Months	Perform thorough testing of the receiver to ensure that specified performance is maintained.

Table 5-2: Test Equipment for the Performance Test

Type	Specifications	Example
Signal Generator	10 Hz - 1280 MHz AM, CW	Hewlett Packard 8662A
Spectrum Analyzer	10 kHz - 1.8 GHz	Tektronix 7L14
Oscilloscope	300 MHz Bandwidth	Tektronix 2465
Frequency Counter	10 Hz - 3 GHz	Hewlett Packard 5386A
IEEE-488 Controller (Optional)	Computer With Directly Controllable Interface	HP-85

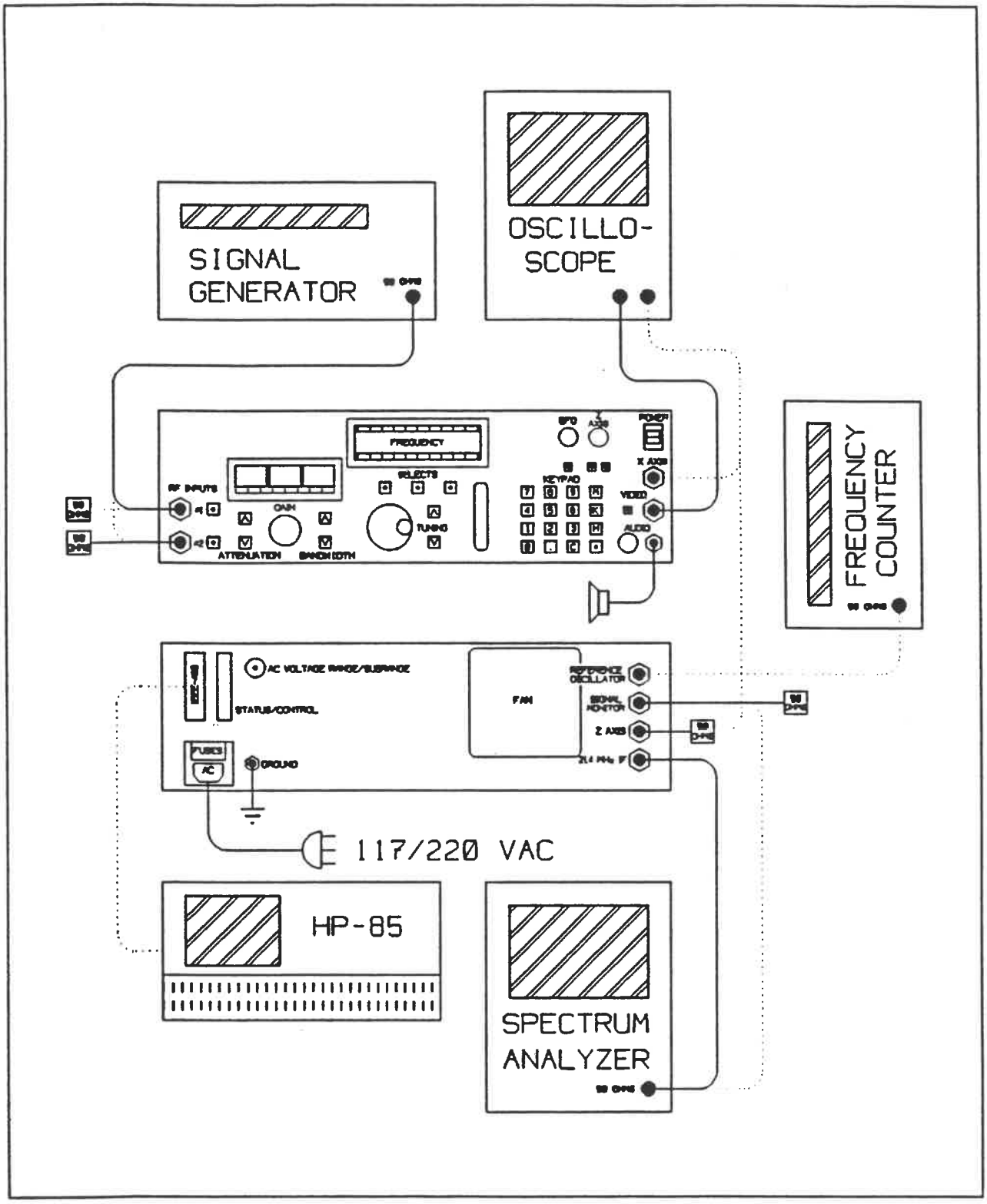

Figure 5-1: Test Points for the Performance Test

5.2.1.1 Setup

The performance test is based on a standard test setup. This is as follows:

- The radio is in its powerup condition:

  Tuned frequency = 100 MHz
  Input select = input #1
  Input attenuation = 20 dB
  Gain = 50 dB
  Bandwith = 1 MHz
  Detection = linear
  BFO, Z axis, autorange, AGC disabled
  Tune mode selected, 1 MHz tuning display digit selected for tuning

- A signal generator is connected to the radio's #1 input:

  Frequency = 100 MHz
  Amplitude = -60 dBm
  Modulation = unmodulated CW

- The radio's #2 input is terminated in 50 Ohms.

- A spectrum analyzer is connected to the radio's 21.4 MHz IF monitor jack (not the "signal monitor" jack):

  Center frequency = 21.4 MHz
  Reference = +10 dBm

- An oscilloscope is connected to the radio's video output jack through a 50 Ohm feed-through terminator:

  Sensitivity = 0.5 V/div
  Coupling = DC
  Trace position = bottom of screen

Many of the test steps will call for variations on this basic setup. These variations will be described at the point at which they are required.

5.2.1.2 Procedure

The performance test procedure is functionally divided into a number of test headings, each of which typically contains a number of steps to be performed.

5.2.1.2.1 Front Panel Operation

This test verifies the operation of those front panel controls and displays which interface with the controlling microprocessor. Note that this is a test of the controls only, not the functions associated with them. Not included are the BFO, Z axis, and audio gain control knobs. Several of the status indicators are also not included because they require special equipment, or require that a hardware fault be induced. Some of these indicators will be exercised in subsequent tests.

For this test the standard test setup is not required. An oscilloscope is required for the X axis test.

1. Press the RF input select pushbuttons one at a time. Pressing one of these buttons should cause its internal indicator LED to illuminate, and the LED in the opposite pushbutton to extinguish.

2. Press the RF input attenuation stepping pushbuttons one at a time. They should cause the value indicated on the attenuation display to step up and down.

3. Rotate the IF gain control knob in both directions. The rotation should cause the value indicated on the gain display to step up and down.

4. Press the IF bandwidth stepping pushbuttons one at a time. They should cause the value indicatated on the bandwidth display to step up and down.

5. Rotate the tuning knob in both directions. The rotation should cause the value indicated on the tuning display to step up and down, with the step size based on the selected (blinking) display digit.

6. Press the tuned frequency stepping pushbuttons one at a time. They should cause the value indicated on the tuning display to step up and down, with the step size based on the selected (blinking) display digit.

7. Enter the sequence "1234567890." on the keypad. The digits should be shown on the tuning display as they are entered. Now press the "C" key. The display should revert to its previous indication.

   Enter the sequence "1K". The display should indicate 1 kHz.

   Enter the sequence "1M". The display should indicate 1 MHz.

   Enter the sequence "1000H". The display should indicate 1 kHz.

8. Press the log detector pushbutton. Its internal indicator LED should illuminate. Press it again and the LED should extinguish.

9. Press the BFO enable pushbutton. Its internal indicator LED should illuminate. Press it again and the LED should extinguish.

10. Press the Z axis enable pushbutton. Its internal indicator LED should illuminate. Press it again and it should extinguish. With the Z axis enable pushbutton indicator LED illuminated, press the Z axis invert pushbutton. Its internal indicator LED should illuminate. Press it again and the LED should extinguish.

11. Press the STEP pushbutton below the tuning display. Its internal indicator LED should illuminate. Press it again and the LED should extinguish.

    With the STEP pushbutton indicator LED extinguished, press the←SELECT pushbutton a few times. The blinking digit selection on the tuning display should move left and then wrap around to the right end of the display.

    With the STEP pushbutton indicator LED extinguished, press the SELECT→ pushbutton a few times. The blinking digit selection on the tuning display should move right and then wrap around to the left end of the display.

12. Press the alt mode pushbutton in at the bottom right of the keypad. Its internal indicator LED should illuminate. Press it again and the LED should extinguish.

13. Enable autorange. The AUTO indicator should illuminate. Disable it and the indicator should extinguish.

    Enable AGC. The AGC indicator should illuminate. Disable it and the indicator should extinguish.

    Enable absolute gain display mode. The ABS indicator should illuminate. Disable it and the indicator should extinguish.

    Enable delta gain display mode. The DELTA indicator should illuminate. Disable it and the indicator should extinguish.

    Enable CW gain distribution mode. The CW DIST indicator should illuminate. Disable it and the indicator should extinguish.

    Enable external wideband mode. The WIDE indicator should illuminate. Disable it and the indicator should extinguish.

    Set the bandwidth to 1 MHz and the tuned frequency to 1 MHz. The BW LIM indicator should illuminate. Set the tuned frequency to 100 MHz and the indicator should extinguish.

    Set the bandwidth to 10 kHz and the tuned frequency to 100 MHz. Select the 1 MHz tuning display digit for tuning. The BW GAP indicator should illuminate. Select 1 MHz bandwidth and the indicator should extinguish.

    The AC HI, AC LO, REG, LOCK, FR OVL, BK OVL, MDC, and THRESH indicators should all be extinguished.

14. Enter tune mode. The TUNE mode indicator should illuminate. All other operating mode indicators should be extinguished.

    Enter start mode. The START mode indicator should illuminate and the TUNE mode indicator should extinguish.

    Enter stop mode. The STOP mode indicator should illuminate and the START mode indicator should extinguish.

    Enter step mode. The STEP mode indicator should illuminate and the STOP mode indicator should extinguish.

    Enter rate mode. The RATE mode indicator should illuminate and the STEP mode indicator should extinguish.

    Enter scan mode. The SCAN mode indicator should illuminate and the RATE mode indicator should extinguish.

    Enter store mode. The STORE mode indicator should illuminate and the SCAN mode indicator should extinguish.

    Enter recall mode. The RCL mode indicator should illuminate and the STORE mode indicator should extinguish.

    Enter reset mode. The RESET mode indicator should illuminate and the RCL indicator should extinguish.

15. Set up the following scan parameters:

    Start frequency = 100 MHz
    Stop frequency = 200 MHz
    Step size = 1 MHz
    Step rate = 1 step/second
    Repeat = none

    Connect an oscilloscope to the X axis output connector. Set it for continuous monitoring of DC over a 0 - 10 Volt range. The initial voltage should be zero.

    Initiate an upward scan using the SELECT→ pushbutton. The indicator LED inside the pushbutton should illuminate and the scan should commence. Time the scan to completion. It should require 100 seconds. The indicator LED inside the pushbutton should extinguish at the end of the scan. The X axis output should proceed linearly from 0 to +10 Volts during the course of the scan.

    Initiate a downward scan using the←SELECT pushbutton. The indicator LED inside the pushbutton should illuminate as the scan commences. It should extinguish at the end of the scan.

16. Select front panel beep volume adjustment mode and rotate the tuning knob back and forth. The piezo transducer should sound and the volume should vary with the tuning knob position.

    Plug a speaker or headphone into the audio jack and select audio beep volume adjustment mode. Rotating the tuning knob back and forth should produce an audible indication through the speaker at varying volume levels.

17. Select display brightness adjustment mode and verify that the LED matrix character displays may be dimmed and extinguished.

5.2.1.2.2 Power Supply Monitor

There are three power supply status monitor indicators on the front panel of the radio, for AC line high, AC line low, and DC regulation. While it is not advisable to deliberately induce a regulation fault, it should be possible to exercise one or both of the AC line monitors by adjusting the range switch on the rear panel. Note that this test does not require the test equipment used by the standard test setup.

1. It is assumed that the 120 VAC/220 VAC selection was properly made before initial use of the radio.

2. Rotate the AC subrange switch on the rear panel across its range. If the mains voltage is nominal then one extreme setting should cause the AC HI indicator on the front panel to illuminate, while the other extreme should cause the AC LO indicator to illuminate.

3. At least one setting of the AC subrange switch should cause both AC line indicators to extinguish. If more than one setting does this then choose the one which is in the middle for normal use.

5.2.1.2.3 Reference Oscillator Output

Note that this test does not require the test equipment used by the standard test setup. It does require a frequency counter, however.

1. Connect a frequency counter to the reference oscillator output jack on the rear panel of the radio. The radio must be warmed up for at least 1 hour.

2. Measure the frequency at the monitor connector. It should be 20 MHz to within a couple of Hz.

5.2.1.2.4 RF Input Selection

This test exercises the RF input select relay. It is also the first throughput test of the signal path, so that many other problems may first show up here as well.

1. Begin with the standard test setup described in paragraph 5.2.1.1. A clear signal should be present from the IF on the spectrum analyzer screen and a DC offset from the video should be indicated on the oscilloscope.

2. Select RF input #2 without moving the signal generator connection. The indications on the spectrum analyzer and the oscilloscope should fall to zero (or nearly so).

3. Now reconnect the signal generator to RF input #2 and the 50 Ohm terminator to RF input #1. The signals on the spectrum analyzer and the oscilloscope should be identical to those seen in step 1.

4. Select RF input #1 without moving the signal generator connection. The indications on the spectrum analyzer and the oscilloscope shoud again fall to zero.

5.2.1.2.5 RF Input Attenuation

1. Begin with the standard test setup described in paragraph 5.2.1.1. From the standard attenuation setting of 20 dB, increase attenuation a step at a time and observe the results on the spectrum analyzer. Each step should cause a 10 dB reduction on the screen.

2. Return to 20 dB of attenuation and set the signal generator to -80 dBm. Now step the attenuation down. The indication on the spectrum analyzer should increase at 10 dB per step.

5.2.1.2.6 IF Gain Control

1. Begin with the standard test setup described in paragraph 5.2.1.1. From the standard gain setting of 50 dB, use the gain control to decrease the gain and observe the results on the spectrum analyzer. The IF signal should attenuate smoothly and linearly through the entire 50 dB range of the control.

5.2.1.2.7 IF Bandwidth Selection

For the 21.4 MHz IF bandwidths, front end noise is used as a broadband source and the effects of the various IF bandwidth filters observed. For DCIF bandwidths a signal must be applied. This is the first test in which the DCIF module is used. Up until now it has not been in the signal path.

1. Begin with the standard test setup described in paragraph 5.2.1.1. Select RF input #2 so as to monitor front-end noise.

2. Observe the noise bandwidth on the spectrum analyzer. At the standard setup bandwidth of 1 MHz, the noise bandwidth (-6 dB points) should also be 1 MHz. Note the video output level on the oscilloscope as well.

3. Now select the other 21.4 MHz IF bandwidths (everything available down to and including 80 kHz) and observe the noise bandwidth on the spectrum analyzer. In each case the bandwidth shown on the analyzer should match the bandwidth setting. The video output should remain at the same RMS level for each selection.

4. Select RF input #1 and 20 kHz bandwidth. This switches in the DCIF. Slightly vary the signal generator frequency to find the -6 dB points of the bandwidth. They should be at 10 kHz offset from 100 MHz. Make sure that the LOCK indicator is not illuminated, since this test initiates the use of two synthesizers which were not previously enabled.

5. Select bandwidths of 10 kHz and 5 kHz. In each case check the bandwidth at the output by varying the signal generator frequency, and verify that the LOCK indicator remains extinguished. These three bandwidths exercise the range of the DCIF filter clock synthesizer. In each case the -6 dB points should be offset half the nominal bandwidth from the tuned frequency of the radio.

5.2.1.2.8 Tuning Bands and Synthesizer Range

This test checks the signal paths of the three tuning bands. In doing so a few extra tuned frequencies will be included to run the programmable microwave and low frequency synthesizers through their ranges. This involves taking advantage of the band switching hysteresis available when using the tuning knob and pushbuttons. Note that this test is the first point in the procedure at which the low frequency RF module is used.

1. Begin with the standard test setup described in paragraph 5.2.1.1. Note the signal level indicated on the spectrum analyzer.

2. Tune the radio to 1 GHz and set the signal generator to this frequency as well. The spectrum analyzer should show the same signal level as before and the LOCK indicator should still be extinguished.

3. Tune the radio to 20 MHz. Now, using the tuning knob and pushbuttons BUT NOT THE KEYPAD, step the tuned frequency down to 13.5 MHz WITHOUT OVERSHOOTING. Set the signal generator to this frequency as well. The spectrum analyzer should show the same signal level as before and the LOCK indicator should still be extinguished.

4. Tune the radio to 7.5 MHz and set the signal generator to this frequency as well. The spectrum analyzer should show the same signal level as before and the LOCK indicator should still be extinguished.

5. Step the bandwidth down to 80 kHz and reduce gain to return the signal level on the spectrum analyzer to where it was before. Now, using the tuning knob and pusbuttons BUT NOT THE KEYPAD, step the tuned frequency up to 16.499999 MHz WITHOUT OVERSHOOTING. Set the signal generator to this frequency as well. The spectrum analyzer should show the same signal level as before and the LOCK indicator should still be extinguished.

6. Set the tuned frequency to 300 kHz. Now, using the tuning knob and pushbuttons BUT NOT THE KEYPAD, step the tuned frequency down to 225.0000 kHz WITHOUT OVERSHOOTING. Set the signal generator to this frequency as well. The spectrum analyzer should show the same signal level as before and the LOCK indicator should still be extinguished.

7. Set the tuned frequency to 200 kHz and set the signal generator to this frequency as well. The spectrum analzyer should show the same signal level as before and the LOCK indicator should still be extinguished.

8. Step the bandwidth down to 500 Hz and reduce gain to return the signal level on the spectrum analyzer to where it was before. Now, using the tuning knob and pushbuttons BUT NOT THE KEYPAD, step the tuned frequency up to 264.9999 kHz WITHOUT OVERSHOOTING. Set the signal generator to this frequency as well. The spectrum analyzer should show the same signal level as before and the LOCK indicator should still be extinguished.

9. Tune the radio to 1 kHz and set the signal generator to this frequency as well. The spectrum analyzer should show the same signal level as before and the LOCK indicator should still be extinguished.

5.2.1.2.9 Log Detector

The log detector and the linear detector use different signal pickoff points in the 21.4 MHz IF. In addition the DCIF performs its own detection and bypasses the linear detector when it is used in linear mode. This test checks the log detector both with and without the DCIF.

1. Begin with the standard test setup described in paragraph 5.2.1.1. Enable log detection.

2. Set the signal generator amplitude to produce 3.0 Volts of video as indicated on the oscilloscope. Now step the radio's RF input attenuation up and down and verify that each 10 dB step produces 0.5 Volts of change at the video output.

3. Set the bandwidth to 20 kHz. Adjust the signal generator for 3.0 Volts at the video output. Stepping the input attenuator should again cause the video output to change 0.5 Volts for each 10 dB step.

5.2.1.2.10 Overload Detectors

There is only one front end overload detector, but there are three for the back end: one for the 21.4 MHz IF, one for the DCIF, and one for the video. It is possible to test each one separately, using different combinations of radio settings.

1. Begin with the standard test setup described in paragraph 5.2.1.1. Then set the RF input attenuation to zero and gradually increase the signal generator level. The FR OVL indicator should illuminate when the signal generator is set somewhere between -30 dBm and -20 dBm.

2. Return to the standard test setup. Then gradually increase the signal generator level. The BK OVL indicator should illuminate at a signal generator level of around -50 dBm. This is a video overload.

3. Return to the standard test setup. Set the bandwidth to 1 kHz and gradually increase the signal generator level. The BK OVL indicator should illuminate when the 21.4 MHz IF level, as seen on the spectrum analyzer, reaches about +6 dBm. This is a DCIF overload.

4. Return to the standard test setup. Set bandwidth to 15 MHz, enable log detection, and gradually increase the signal generator level. The BK OVL indicator should illuminate when the video level, as seen on the oscilloscope, reaches about 3.5 Volts. This is a back end IF overload.

5.2.1.2.11 Signal Monitor and Z Axis Outputs

The signal monitor and Z axis outputs are both sent to connectors on the rear panel. Signal monitor is taken from the front end of the 21.4 MHz IF while Z axis is taken from the video. The Z axis output is provided with controls which must be exercised.

1. Begin with the standard test setup described in paragraph 5.2.1.1. Reconnect the spectrum analyzer to the signal monitor output jack on the rear panel of the radio and verify the presence of the 21.4 MHz IF signal. Then return the analyzer connection to the 21.4 MHz IF monitor jack.

2. While maintaining the existing oscilloscope connection to the video output, connect the other oscilloscope input to the Z axis output on the rear panel of the radio, using a 50 Ohm feed-through terminator. Set the oscilloscope to monitor both outputs simultaneously. Set the signal generator for 1 kHz AM modulation. In the standard test setup the Z axis output is disabled, so there should be no output visible on the oscilloscope.

3. Enable the Z axis output and set the level control fully clockwise. The Z axis output should show the AM modulation but no DC offset. The displayed modulation level should be about 1.5 times that present at the video output.

4. Rotate the Z axis level control counterclockwise. The Z axis output should reduce to zero. Now return the control to the fully clockwise position and press the invert pushbutton. The phase of the Z axis output should reverse relative to the video output.

5.2.1.2.12 Audio Output and BFO Detector

The output of the BFO detector, when enabled, replaces the output of the other detectors in the audio output only. Tests of the BFO and the audio output are grouped together for convenience.

1. Begin with the standard test setup described in paragraph 5.2.1.1. Plug a speaker or headphone into the audio output jack on the front panel of the radio. Select 1 kHz AM modulation on the signal generator and verify that the modulation appears at the audio output. Rotate the audio volume control back and forth and verify its operation.

2. Return the signal generator to unmodulated CW and enable BFO detection. Rotate the BFO control back and forth and verify a zero beat near the midrange position of the control, with increasing beat frequency on either side.

5.2.1.2.13 Autorange and AGC

Although these functions are implemented very differently, they perform a similar function. They are also grouped together in a single keypad operating mode.

1. Begin with the standard test setup described in paragraph 5.2.1.1. Enable the autorange function. Now vary the signal generator level and observe the input attenuation of the radio. It should step up and down to track the signal generator level loosely, with about 13 dB of hysteresis.

2. Return to the standard test setup and enable AGC. Reduce the signal generator level to minimum and gradually increase it. The video output level, as seen on the oscilloscope display, should level off as signal generator level increases, approaching about 3 Volts as a limit.

5.2.1.2.14 IEEE-488 Interface

The radio makes use of the IEEE-488 interface in two ways: to control an external microwave downconverter and to accept commands from an external host. The two are mutually exclusive, so that the interface may only be used for one purpose in any particular application. If the interface of the radio under test is not being used then the test is unnecessary. If the radio is used with an MDC then demonstrated control of the MDC is a sufficient test of the interface. If the radio is remotely controlled by a host then demonstration of that control is a sufficient test of the interface. A desktop computer with direct control of its IEEE-488 interface is listed in the test equipment table, for use when the equipment which is normally connected to the interface is unavailable. When using this computer it is sufficient to take control of the radio, issue a setting command to it, and read back the setting.

Factory-set interface address = 16
Example command = "FREQ 12345"
Example setting request = "FREQ?"

The return data in this case should be "1.2345E+4".

5.2.1.2.15 Sample Data Sheet

R-110 RECEIVER PERFORMANCE TEST

SAMPLE DATA SHEET

Serial Number: _____ **Rev Level:** _____ **Date:** _____

Front Panel Operation:	_____ (✓)	Comments: _____
Power Supply Monitor:	_____ (✓)	Comments: _____
20 MHz Monitor:	_____ (✓)	Comments: _____
RF Input Selection:	_____ (✓)	Comments: _____
RF Input Attenuator:	_____ (✓)	Comments: _____
Gain Control:	_____ (✓)	Comments: _____
Bandwidth Selection:	_____ (✓)	Comments: _____
Tuning Bands:	_____ (✓)	Comments: _____
Synthesizer Range:	_____ (✓)	Comments: _____
Log Detector:	_____ (✓)	Comments: _____
Overload Detectors:	_____ (✓)	Comments: _____
Signal Monitor:	_____ (✓)	Comments: _____
Audio Output:	_____ (✓)	Comments: _____
BFO Detector:	_____ (✓)	Comments: _____
Autorange:	_____ (✓)	Comments: _____
AGC:	_____ (✓)	Comments: _____
IEEE-488 Interface:	_____ (✓)	Comments: _____ (Optional)

Test Operator: _____

5.2.2 Fault Isolation

The R-110 is designed so that failures in the performance test, or other detected faults, may in most cases be easily isolated to a single failing assembly. If a failure is detected in normal use then the performance test may be of assistance in the first level of isolation, but in most cases the appropriate fault isolation procedure may be identified and followed directly.

Hardware which is likely to fail will almost certainly be contained in one of the following modules:

- front panel assembly
- microwave RF module
- preselector module
- low frequency RF module
- 21.4 MHz IF amplifier module and 21.4 MHz IF filter module
- DCIF module
- video module
- synthesizer section (microwave synthesizer module, low frequency synthesizer module, fixed LO synthesizer module, plus parts of the microwave RF module and preselector module)
- power supply (part of rear panel assembly)

Fault isolation is normally to the level of one of the modules or assemblies listed above. In addition, some faults may be further isolated within certain assemblies, such as the front panel or power supply. Replacement is usually at the assembly level, but schematics and parts lists are provided in chapter 6 for isolation to the component level.

Note that catastrophic power supply failures may require replacement of more than just the power supply. Certain circuits in the R-110 can be damaged under conditions in which some power supply voltages are present and others absent.

Note too that the section of the R-110 most susceptible to failure under extreme temperatures is again the power supply.

Following is a list of typical fault conditions and fault isolation suggestions for each. It should be possible to find an example which is similar enough to any major fault encountered to enable the fault to be localized. Minor faults, such as barely failing a spec involving end-to-end performance, may be more difficult to localize.

5.2.2.1 Radio Completely Dead

If the radio does nothing at all when power is applied, and no front panel indicators illuminate, then there is a problem in the power supply. First check the fuses, located in the AC input module on the rear panel. After the AC input module the common power path includes the front panel power switch and the cabling to it across the cardcage, the AC range switch on the rear panel, the fan, and the primary of the power transformer. If the fan works properly then most of this, at least up to the transformer, is probably ok. If the fan isn't working, then the problem is probably in this area. Note that the front panel power switch connects to the rear panel assembly with connectorized cables, which allows the front and rear panels to be separated from the cardcage. In conditions of extreme vibration these connectors may come loose. The DC harness linking the cardcage and the front panel assembly to the power supply also plugs into the rear panel assembly, so it too should be checked.

Next check the RF input select indicators on the front panel, which are located inside the RF input select pushbuttons. These are controlled by opposite outputs of a flip-flop, so if +5 VDC is available to the front panel control assembly then one or the other should be illuminated. Note that there are two separate +5 VDC regulators in the power supply, one for the front panel and one for the cardcage.

If +5 VDC is present at the front panel then the processor and displays should be working and yielding reasonable indications. If the power supply checks out but the front panel is still dead then check the mating of the DC supplies to the front panel assembly (the 15 pin D-sub on the back of the assembly). If power is being delivered adequately then suspect the processor PCB in the front panel assembly.

5.2.2.2 Front Panel Displays/Indicators Illuminated But Random

If +5 VDC is being supplied to the front panel assembly then at least some of the indicators should be illuminated. If the displays and indicators make no sense at all then the problem is probably in the processor PCB. If most of the displays and indicators appear to be okay, and the pushbuttons appear to be at least partly functional, then the problem is probably in either the switch/display PCB or the interface PCB, both in the front panel assembly. The pushbuttons and the tuning and gain controls, the LED indicators inside the pushbuttons, and the LED status and mode indicators surrounding the LED matrix character displays, are all sensed or driven via separate connections to the interface PCB, so it is not too difficult to identify which PCB is at fault once they have been removed from the front panel assembly sheet metal to allow probing. The LED matrix character displays are connected in parallel to a control bus from the interface PCB. Each display consists of four characters. If one display is bad then the fault is probably in the switch/display PCB. If all six are out then it is probably the interface PCB at fault.

The front panel piezo transducer requires +/- 15 VDC as well as control supplied by +5 VDC to operate. If it is not working then either it or its on/off switching transistor on the switch/display PCB may be bad, or the DAC-controlled voltage driver on the interface PCB may be bad. If neither the piezo transducer nor the audible indicator source to the audio output amplifier are working then the problem is in the interface PCB.

Once a problem has been narrowed down to the front panel assembly control circuits, fault isolation to one of the three PCBs is accomplished by taking apart the front panel assembly, removing the three PCBs and re-attaching them together outside the sheet metal. The 15 pin power connector may then be re-attached to the back of the processor PCB and the tuning and gain controls may be dismounted and re-attached to the switch/display PCB. This results in a complete, working control assembly without the surrounding sheet metal, which allows probing to localize a fault.

5.2.2.3 RF Input Selection/Attenuation Inoperative

The RF input relays and attenuator are the only items in the radio which require the use of the +24 VDC supply. The supply is the first thing to check. If it is okay but neither the input select relay nor the attenuator work, then the driver IC on the interface PCB is probably at fault. If only one function is inoperative then it may be a bad relay or attenuator, or one section of the driver IC.

Tuning in band 3 causes the front panel band select relay to direct the signal to the microwave module, while tuning in bands 1 and 2 cause it to direct the signal to the low frequency RF module. Faults which may appear to be caused by bad cardcage modules may be traceable to this relay (or the driver on the interface PCB) as well.

5.2.2.4 Audio Output or X Axis Output Inoperative

The audio output amplifier and the X axis output buffer are located on the X axis/audio output PCB in the front panel assembly.

The X axis output buffer uses the +/- 15 VDC supply from the cardcage. Its input comes from the interface PCB in the front panel assembly, which uses a +/- 15 VDC supply based on a different pair of regulators. A failing X axis output, given that the power supplies are good, is traceable to either the interface PCB or the X axis/audio output PCB, or the coax cable linking them, which might possibly become pinched in the partition during assembly.

The audio output amplifier consists of a front panel volume control, a preamp, and a power amp. All of the circuitry except for the volume control are located on the X axis/audio output PCB. The preamp and power amp are supplied by separate pairs of +/- 15 VDC regulators. The preamp shares its supply with the cardcage and the X axis buffer, while the power amp shares its supply with the front panel control section, where it is used by the DACs and amplifiers for the piezo transducer, the audio output beeper, and the X axis source.

The audio signal originates at the video module in the cardcage and is passed to the front panel assembly via coax cable. It passes through the volume control and the preamp and is then combined with the audible indicator signal from the interface PCB at the power amp. Thus if the audible indicator function works but there is no audio from the video module, then the volume control and preamp are suspect. If there is neither audible indicator function nor audio output then the power amplifier is suspect. If only the audible indicator function is failing then first make sure that the programmed volume is not set too low. Then suspect the connecting cable from the interface PCB, which can become pinched in the partition during assembly.

The X axis/audio output PCB has its own 9 pin D-sub power connector. If a failure is traced to this PCB then make sure that the power connector is mating properly.

5.2.2.5 One or More DC Supplies Inoperative

Here is a list of the DC supplies. Each listing has separate regulators, except for the +24 VDC supply, which is unregulated:

- +5 VDC for the front panel control section
- +5 VDC for the cardcage and the front panel cardcage interface buffer
- +24 VDC for the front panel input relays and attenuator
- +/- 15 VDC for the cardcage, the front panel audio preamp and X axis output buffer
- +/- 15 VDC for the audible indicator and X axis sources, the piezo transducer, the RS-232 interface, and the audio output power amp
- +/- 8 VDC for the cardcage
- +50 VDC for the cardcage

Cardcage voltages may be conveniently measured at the feed-through capacitors in the sidewall of the cardcage. Here is the color coding:

- green: +5 VDC
- brown: +8 VDC
- blue: -8 VDC
- red: +15 VDC
- violet: -15 VDC
- yellow: +50 VDC
- black: ground

Table 5-3 shows the usage of the various power supplies.

Table 5-3: Power Supply Usage

	+5 #1	+5 #2	+8	-8	+15 #1	-15 #1	+15 #2	-15 #2	+24	+50
Control Section	X	X					X	X	X	
X Axis/Audio Amplifier PCB					X	X	X	X		
Microwave RF Module		X		X	X					
Preselector Module		X			X	X				
Low Frequency RF Module			X	X	X					
21.4 MHz IF Amplifier Module		X	X	X	X	X				
21.4 MHz IF Filter Module			X	X						
Video Module		X	X	X	X	X				
DCIF Module		X	X	X	X	X				
Fixed LO Synthesizer Module		X			X	X				
Low Frequency Synthesizer Module		X			X	X				
Microwave Synthesizer Module		X			X	X				X

When a particular supply is at fault then the cause may be either the supply itself or something connected to it which is drawing excessive current. The first step in isolating the fault is to unplug or disconnect those modules and assemblies which use that supply. If it still fails without a load then the power supply is at fault. It is also possible that the supply fails only under load, but this is less likely.

A power supply monitor circuit is provided which sends the control section three status signals: AC line high, AC line low, and DC regulation. All three of these are passed to front panel indicators, so that if +5 VDC is available to the control section then the power supply section can usually indicate a power supply problem. AC high and AC low indications may normally be alleviated by changing the setting of the line voltage subrange switch on the rear panel. AC high causes no real problems other than excessive power dissipation and heat generation in the regulators. If the regulators get too hot then they go into thermal shutdown. AC low, if excessive, can result in insufficient headroom for the regulators, causing a regulation error as well. Thus any AC status indications should be alleviated before suspecting the regulators. Of course, the 120 VAC/220 VAC switch should be properly set before powering up the radio.

All of the power supply outputs are monitored by the DC regulation status indicator except for two:

- the +5 VDC supply to the control section. It is assumed that if it goes out of regulation then the control section will not be operational, obviating the need for a status indication.
- the -15 VDC supply which is used for the audio output power amplifier and the control section source circuits for the audible indication and X axis functions, and for the RS-232 drivers.

The +24 VDC supply is monitored at looser tolerance because it is unregulated.

5.2.2.6 Front Panel Operative, Signal Path Inoperative

This is a wide-ranging fault which may eventually be traced to almost any part of the radio. It assumes that none of the three tuning bands are operative.

A ribbon cable links the front panel assembly to the cardcage backplane. This ribbon cable is used to set control latches in the cardcage modules, and to return status as well. The interface originates in the front panel on the interface PCB, but is buffered in both directions on the processor PCB. These buffers use the same +5 VDC supply that is used by the cardcage, while the rest of the front panel uses a different supply. The buffer circuits are completely isolated from the rest of the processor PCB.

A quick check to see if the front panel to cardcage link is operating is to select log mode and listen for relays clicking in the video module. More relays should click in the video module when going in and out of the DCIF bandwidth range. The following cardcage modules receive control from the front panel:

- 21.4 MHz IF amplifier module
- video module
- DCIF module
- fixed LO synthesizer module
- microwave synthesizer module
- low frequency synthesizer module

In addition, control is relayed from the 21.4 MHz IF amplifier module to the microwave RF module, the low frequency RF module, and the 21.4 MHz IF filter module. The control interface from the front panel is bussed all the way across the backplane, so all of the module connectors will have the same interface signals on the same contacts. One way to check for operation of the interface is to monitor the data, address, write, and clear lines with an oscilloscope and verify that they show activity at both 0 and +5 Volts. The interface circuitry is based on HCMOS, so logic levels should be near the rails. The 2.4 Volt threshold used by normal TTL is not usable here.

If the control interface seems to be operational then the next thing to check is the programmable low frequency synthesizer. This is the only synthesizer that is necessary to the operation of all three tuning bands. If it is not working then the lock status indicator on the front panel and one or both of the indicator LEDs showing through the top of the low frequency synthesizer module should be illuminated.

Next check the front panel RF input circuiry. Signals should be applied to the RF inputs and verified exiting the front panel assembly at the appropriate connectors for tuning in band 1/2 and tuning in band 3. One of the most frequent radio failures is that the coax relays degrade over time, more rapidly than their specs would indicate.

The signal path splits before it comes out of the front panel assembly. Since it is assumed that none of the tuning bands work, the next place to check is the point at which the paths come back together, at the inputs to the IF amplifier module. If no signals appear here in any tuning band, then the cardcage control interface is again suspect.

The signal path goes from the 21.4 MHz IF amplifier module to the 21.4 MHz IF filter module and back again under most operating conditions. To simplify matters, select the widest bandwidth and linear detection. This eliminates the bandwidth filters which are normally switched into the path in series as they are selected, and selects a standard IF pickoff point for detection. Verify that the signal passes properly from the IF amplifier module to the IF filter module and back again. There are also two monitor points in the 21.4 MHz IF which are sent to the rear panel, and which may be used to make checking easier.

Now check that the signal arrives properly at the video module. If it does then the video module is the about all that is left that can be at fault.

5.2.2.7 Tuning Bands 1 and 2 Operative, Band 3 Inoperative

The band 2/3 break is at 15 MHz, using the keypad. It will vary from this if the tuning knob and pushbuttons are used, due to applied hysteresis about the nominal break frequency. Signal paths begin in common through the input select relay and attenuator in the front panel assembly, but then, still in the front panel assembly, are split into band 3 and band 1/2 paths with a relay. The band 1/2 path goes to the low frequency RF module while the band 3 path goes to a filter on the preselector module and from there to the microwave RF module. A relay at the input of the 21.4 MHz IF amplifier module selects between the outputs of the low frequency RF and microwave RF modules, ending the separation of the signal paths. The band 3 signal path makes use of three synthesizers not used by the band 1/2 signal path: the programmable microwave synthesizer, the 2 GHz fixed LO, and the 523 - 533 MHz mixer loop.

All synthesizer and loop-generated LOs in the radio produce lock status signals which are bussed together to drive a front panel status indicator. If the front panel LOCK indicator shows a problem then there are two ways to proceed. Some of the discrete lock status signals also drive indicator LEDs which show through the tops of their respective cardcage plug-in modules. An illuminated LED indicates out-of-lock, but make sure that the particular LED in question is associated with a loop currently in use, as some loops will be active but lose lock when they are not in use.

The discrete status lines are also delivered to the cardcage backplane individually. A particular lock status may be determined from the assigned backplane connector pin. These lines are bussed all the way across the backplane, so status may be verified from any connector.

The first thing to check is that the programmable microwave synthesizer, the 2 GHz loop, and the 523 - 533 MHz loop are all locked. Then verify that the distribution relay in the front panel is operating properly, delivering the signal to the preselector module when the radio is tuned in band 3. Next make sure that the signal is passing through the filter on the preselector module and arriving at the microwave RF module. The 1470 MHz IF may be verified by selecting external wideband operation and observing the wideband output on the top of the microwave module. If it is operational then verify that the signal is being delivered to the IF amplifier module at 21.4 MHz. If it is, then the only remaining item is the input select relay in the 21.4 MHz IF amplifier module.

5.2.2.8 Tuning Band 3 Operative, Bands 1/2 Inoperative

As in the previous case, the difference in the signal paths is localized. In this case band 1 uses an LO not used elsewhere, that being the 3 MHz fixed LO used for upconversion. This LO is made by picking off the third harmonic of a 1 MHz reference, not by implementing a loop. Therefore there is no lock status indication for it. If band 1 is failing but band 2 is okay then this is the first thing to check.

The signal path splits at the front panel RF input distribution relay. A signal should be applied to the RF inputs and its presence verified at the low frequency RF module input connector when the radio is tuned in those bands. If present then it should be verified at the band 1/2 input to the 21.4 MHz IF amplifier module. If present then the only remaining item is the input select relay in the 21.4 MHz IF amplifier module.

5.2.2.9 One or More IF Bandwidths Inoperative

The wider bandwidth filters are in the 21.4 MHz IF filter module, the narrower ones in the DCIF module. The widest DCIF bandwidth is 20 kHz.

The 21.4 MHz IF filter module sections are attached in series for each narrower bandwidth. In other words, for an 80 kHz selected bandwidth the 15 MHz, 4 MHz, 1 MHz, and 300 kHz filters will all be in the signal path in front of the 80 kHz filter. Selection is controlled by signals passed through the cardcage backplane from the IF amplifier module, which in turn is controlled by the front panel assembly.

Fault isolation in the wider bandwidths consists of applying a signal and, starting at 15 MHz bandwidth, selecting progressively smaller bandwidths until the failing filter is switched in.

The DCIF module uses switched capacitor filters to determine the bandwidth, controlled by a timebase consisting of a PLL synthesizer on the fixed LO module and a triple programmable divider on the DCIF module. Typically all of the DCIF bandwidths will work or none of them will. The signal passes through all of the filter sections in the 21.4 MHz IF filter module before going to the DCIF module, so all of these must be operational as well before the DCIF will work.

If the DCIF bandwidths are failing then the first thing to do is to make sure that the DCIF synthesizers, both the filter clock PLL and the 21.4 MHz fixed LO, are working. Each contributes to the front panel lock status indicator, and each is provided with a discrete indicator LED which shows through the top of the fixed LO synthesizer module. The discrete LEDs illuminate when the associated synthesizer is out of lock.

The next thing to do is to make sure that the signal switching is working. Verify that the signal arrives at the DCIF input when bandwidth selection is in the DCIF range. Note that there are two pickoffs for the DCIF in the 21.4 MHz IF, one for linear mode and one for log mode. Finally, make sure that the DCIF output makes it to the video module. If it does then the remaining item to suspect is the select relay at the input of the video module.

5.2.2.10 Not Enough or Too Much IF Gain Control Range

The front panel IF gain control has a range of 50 dB set by lookup tables in firmware. Single failing gain control settings are traceable to errors in the EEPROM on the processor PCB. If the span of the gain control is off, rather than all of the range being offset high or low, then the problem is probably in the 21.4 MHz IF amplifier module.

Four attenuator circuits are provided in the 21.4 MHz IF amplifier module. Three are employed to implement front panel IF gain control and AGC. The fourth is used to set (fixed) end-to-end gain. Each has a nominal range of about 17 dB, so each one that fails can have that much effect on the total. Note that the first two are controlled by the same circuit, so a failure of this control circuit can have twice as much effect.

One exception is log mode, wherein the third attenuator is bypassed, limiting the gain control range to 16.7 - 50 dB.

5.2.2.11 Autorange Function Inoperative

The autorange function is administered by the processor PCB and operates on the RF input attenuator, based on overload and underload status signals from the 21.4 MHz IF amplifier module. The overload signal also feeds the front overload status indicator. If the attenuator operates normally under manual control and the autorange function may be selected normally on the front panel then the problem is probably in the 21.4 MHz IF amplifier module.

5.2.2.12 AGC Function Inoperative

AGC begins with a slowly varying DC level developed from the video signal on the video module. This signal is routed to the 21.4 MHz IF amplifier module where it is gated with the AGC enable function and then combined with the outputs of the DACs which provide settable gain control. If the function may be selected normally on the front panel then an AGC failure is traceable to either the video module or the IF amplifier module. Monitoring the signal on coax cable connecting them should determine which one is failing.

5.2.2.13 BFO or Z Axis Function Inoperative

Both of these functions are implemented on the video module, so the video module is the prime suspect. However, both functions are provided with front panel controls which may also be the cause of failure. They are linked to the video module via coax cables.

5.2.2.14 Log Detector Inoperative

The log detector is located on the video module, so the video module is the prime suspect. Note that the input to the log detector can come from either the 21.4 MHz IF filter module or from the DCIF module.

5.2.2.15 IEEE-488 Interface Inoperative

The IEEE-488 interface is located on the processor PCB and is cabled to the rear panel using a shielded ribbon cable. Before assuming that the IEEE-488 interface is faulty, be sure to verify that it is enabled in the front panel. The two operating modes are remote and MDC, and only one at a time (or neither) may be enabled. Make sure that the interface address is set properly.

5.2.2.16 General Suggestions

The foregoing cases dealt mainly with catastrophic failures, in which a function failed to perform entirely. Similar isolation procedures may be appropriate when a function is merely out of spec. On the other hand, finding something like a loss of a few dB end-to-end in the signal path may take considerably more testing and effort.

As a general rule check the power supplies first. If they are functioning properly then check the synthesizer lock status indicator on the front panel. If the synthesizers are locked as well and the problem is not in a function that can be localized to one module, then check the signals at the signal monitor and 21.4 MHz IF outputs on the rear panel, and the 1470 MHz external wideband connector on top of the microwave RF module. This should serve to provide the first step in localizing the problem.

5.3 Disassembly

The receiver consists of a one-piece cover and three major assemblies:

- the cardcage assembly (A1)
- the front panel assembly (A2)
- the rear panel assembly (A3)

Each of these major assemblies contains subassemblies. The cardcage is easiest to service because all of its subassemblies (except for the backplane) are in the form of plug-in modules, each held in place with a pair of finger-tight retaining screws. Disassembly of the other two major assemblies is more involved.

This section gives instructions for removing the cover, removing the front and rear panel assemblies from the cardcage assembly, and disassembling the front and rear assemblies sufficiently to remove and replace the subassemblies inside. Instructions are also given for replacing the cardcage backplane. General instructions are given for removing and replacing the cardcage's plug-in modules.

5.3.1 Cover Removal and Replacement

The receiver is contained in a one-piece cover. The internal assemblies are mounted together so that when the cover is removed, what remains will be a single unit.

Procedure:

1. Make sure that the power cord and other cable connections are removed from the receiver.
2. Remove the rack slides, if attached, by removing three screws from each.
3. Place the radio on a flat surface with the front panel facing upward.
4. Remove 14 flat-head screws from the cover: three in the top front, three in the bottom front, three in the top rear, three in the bottom rear, and one on each side in the rear.
5. Remove the cover by pulling it straight up. Since there is gasketing and an intentional tight fit between the internal assemblies and the cover, it may be necessary to press on the front panel as well.

CAUTION

BE CAREFUL OF THE GASKETING AROUND THE INNER EDGE OF THE LIP AROUND THE FRONT OF THE COVER, AND THE GASKETING AROUND THE OUTSIDE OF THE REAR PANEL ASSEMBLY. BOTH ARE DELICATE AND SUBJECT TO SHEARING AND BREAKAGE.

6. Replace the cover by reversing the preceding steps. Again, be very careful of the gasketing at the front of the cover and around the outside of the rear panel assembly.

5.3.2 Plug-In Module Removal and Replacement

Except for the microwave RF module (A1A1), the cardcage's plug-in modules consist of printed circuit boards mounted on shield plates. The plates slide into guides in the cardcage to locate the module, and are provided with ears which contain captive hold-down screws. The printed circuit board contains a double-row DIN connector which plugs into the backplane, plus a number of coax connections which are accessed through holes in the top of the shield plate. A harness of flexible and semi-rigid coax cables is spread across the top of the cardcage, linking the plug-in modules to each other and to the front and rear panel assemblies as well.

The microwave RF module consists of an aluminum block with cavities milled into it, each covered with an aluminum plate. The plates are held in place by aluminum strips, which in turn are held down with numerous small screws. The block is mounted to a printed circuit board which distributes power to the various cavities via feed-throughs. The module is mounted just past the end of the cardcage backplane. The printed circuit board slides into guides in the cardcage, and the aluminum block is provided with mounting ears which contain captive hold-down screws. In addition to coax connections, a discrete-wire pigtail from the backplane plugs into a header at the top of the printed circuit board.

Procedure:

1. Remove the cover. See paragraph 5.3.1.

2. Identify the module to be removed. Each is labeled with an assembly number, from A1 to A17, corresponding to its location in the cardcage.

3. Unplug the coax cables from the top of the module to be removed. They are color-coded for easy replacement. If the microwave RF module is to be removed, unplug the discrete wire pigtail connecting it to the backplane.

4. Unscrew the hold-down screw located at each end of the shield (or, for the microwave module, at each end of the aluminum block).

5. Remove the module by lifting it straight out.

CAUTION

MAKE SURE THAT ALL COAX CABLES ARE OUT OF THE WAY BEFORE REMOVING THE MODULE. DAMAGE TO THE CABLES MAY OTHERWISE RESULT.

6. Replace the module by reversing the preceding steps. Note that if a new or serviced module is being replaced, then recalibration of the receiver may be required.

5.3.3 Cardcage Backplane Removal and Replacement

Removal of the backplane is somewhat involved. It requires soldering and a certain amount of mechanical adjustment. In addition, the entire coax harness and all of the plug-in modules must be removed. Removal of the backplane is not recommended unless absolutely necessary, and even then it is recommended that it be done at the factory. If a single connector fails then it may be possible to replace it without removing the backplane from the cardcage.

The procedure is not given in complete detail, since it is assumed that the person performing it is already familiar with what is required.

Removal Procedure:

1. Remove the cover. See paragraph 5.3.1.

2. Unplug all of the coax cables from the plug-in modules. Unplug the discrete wire pigtail from the microwave RF module.

3. Remove all of the plug-in modules from the cardcage. Unplug the microwave module pigtail and the ribbon cable to the front panel assembly from the backplane. It may be more comfortable to remove the front and rear panel assemblies from the cardcage as well, but this is not strictly necessary.

4. Using a controlled-heat soldering iron, unsolder the ten discrete wires linking the backplane to the feed-through capacitors in the sidewall of the cardcage.

5. Remove the 11 screws holding the backplane to the cardcage. The backplane should now drop from the bottom of the cardcage.

Replacement Procedure:

1. Re-mount the backplane to the cardcage with the 11 screws previously removed.

2. Temporarily slide plug-in modules into place at each end to verify seating height. This may be adjusted by loosening the screws that hold the backplane mounting brackets to the cardcage proper. After verifying the seating height, remove the plug in modules.

3. Re-solder the power wires to the backplane. The backplane schematic (493061) given in section 6 indicates which wire goes where. Replace the front and rear panel assemblies if they were removed.

4. Plug the microwave RF module discrete wire pigtail and the front panel interface cable into the backplane. Then replace all of the plug-in modules, matching their labeled designations to the matching socket designations in the backplane. Plug the other end of the discrete wire pigtail into the microwave module.

5. Replace the coax harness. The connections are color-coded for each module. The flexible and semi-rigid cable diagrams (493055 and 493057) given in section 6 may assist in this.

6. Replace the cover.

5.3.4 Front Panel Assembly Removal and Replacement

The front panel assembly (493600) may be removed from the cardcage assembly by removing a few screws and unplugging a few cables.

Procedure:

1. Remove the cover. See paragraph 5.3.1.

2. There are two semi-rigid cables leading from the front panel assembly to the preselector module (A1A2) and the low frequency RF module (A1A5). Unplug them at the modules.

3. Remove the four flat-head screws in the cardcage flanges which hold the front panel assembly to the cardcage. Make sure to remove these four screws and not the ones adjacent to them in the front panel assembly itself. Separate the front panel assembly slightly from the cardcage, but do not try to remove it completely yet.

4. Unplug the following cables from the rear of the front panel assembly:

   - the IEEE-488 and rear panel status cables (the shielded ribbons).
   - the Z axis, BFO, video, and audio coax cables
   - the DC power connectors (9 and 15 pin discrete-wire D-subs)
   - the cardcage interface cable (37 conductor ribbon)
   - the AC cable (4 pin discrete)

   Do not remove the two semi-rigid coax cables.

5. The front panel assembly may now be completely removed from the cardcage.

6. To replace the front panel assembly, reverse the preceding steps. All cables except for the flexible coax will only fit in one front panel assembly connector, in one orientation. The flexible coax cables all lead to the video module (A1A11) and are color-coded.

5.3.5 Front Panel Disassembly

The front panel assembly (493600) contains three printed circuit boards:

- Switch/display PCB (A2A1)
- Interface PCB (A2A2)
- Processor PCB (A2A3)
- X axis/audio amplifier PCB (A2A4)

In addition, it contains numerous small electromechanical subassemblies which may eventually fail and require replacement. Disassembly is fairly easy, but reassembly is somewhat more tedious.

Disassembly Procedure:

1. Remove the cover. See paragraph 5.3.1.

2. Remove the front panel assembly from the cardcage. See paragraph 5.3.4.

3. Remove the hex nuts retaining the RF input connectors (the BNC connectors on the left side of the front panel). Be careful not to scratch the paint, and to keep track of the mounting hardware.

4. Remove the 12 flathead screws holding the front panel rear bulkhead to the rest of the assembly. Gently slide the bulkhead out of the rear of the assembly an inch or two. Make sure that the RF input connectors withdraw from their mounting holes in the front panel.

5. Unplug the three coax cables attached to the X axis/audio output PCB (A2A4), and the three other coax cables attached to feed-throughs around it. Unplug the audio output jack pigtail and the audio gain control pigtail from the X axis/audio output PCB. Unplug the relay and attenuator pigtails from the interface PCB (A2A2).

6. Now remove the bulkhead subassembly from the rest of the front panel assembly.

7. The X axis/audio output PCB and the coax relay and attenuator subassemblies, all mounted to the bulkhead, are now available for removal and replacement. The semi-rigid cables connecting the relays and the attenuator use SMA-type connectors. A torque wrench is required when re-mounting these cables. Note that the relays and the attenuator are isolated from the bulkhead by insulating wafers.

8. The power switch subassembly may be removed by first removing the screw which holds the pigtail connector to the side of the front panel box. The subassembly may then be pressed out through the front of the panel.

9. The X axis and video BNC connectors, the audio jack subassembly, the audio gain control subassembly, and the BFO and Z axis control subassemblies may now be removed by removing the nuts which retain them to the front panel. Note that the audio output jack requires insulating washers to isolate it from the front panel sheet metal.

10. The switch/display, interface, and processor PCBs (A2A1, A2A2, A2A3) may be removed by first removing the mounting screws from the back of the processor PCB. The three PCBs plug into each other in sequence, and are held together by threaded standoffs. Remove one PCB at a time until the desired PCB is removed. Note that the pigtails from the tuning and gain control subassemblies must be unplugged from the switch/display PCB before it may be removed.

11. Removal of the tuning and gain control subassemblies requires prior removal of all three of the PCBs. The controls may then be removed by removing the retaining nuts holding them to the front panel.

Reassembly Procedure:

1. Remount any front panel control and connector subassemblies (except for the RF input connectors) that have been removed. If the power switch has been removed then press it back in place with the wiring facing down, and remount the pigtail connector to the side of the front panel box. The audio gain control potentiometer and the tuning and gain controls must also be mounted wiring-side down. The BFO and Z axis controls must be mounted with the wiring facing up. The video output BNC connector has an SMB connector on its pigtail, while the X axis output connector has an MCX connector on its pigtail. Make sure that the audio output connector has been remounted with insulating washers, and verify that there is no electrical contact between the body of the jack and the front panel sheet metal.

2. Remount the switch/display PCB by first plugging in the pigtails from the tuning and gain controls. Then place the PCB against the standoffs, making sure that all of the pushbuttons fit through their holes in the front panel. Make sure that the tuning and gain control pigtails aren't pinched. Replace the standoffs and the two screws which hold it in place.

3. Replace the interface and processor PCBs by first plugging the interface PCB into the back of the switch/display PCB, being careful not to offset the double-row connectors. Then replace the standoffs and the screw which hold the interface PCB to the switch/display PCB. Plug the processor PCB into the back of the interface PCB, again being sure that the double-row connectors are not offset. Replace the screws holding the processor PCB to the interface PCB. Note that some of the screws may not be furnished with washers or lockwashers, in order to provide clearance for the bulkhead.

4. Reassemble the bulkhead by re-mounting the relays and the attenuator if they were removed. Note that insulating wafers are required between them and the bulkhead sheet metal. The relays are mounted with nylon screws, and the attenuator uses insulating washers. Note that the semi-rigid cables which connect to the bulkhead are also mounted with insulating washers. See the assembly drawing (493607) for details. When complete, verify that there is no electrical contact between the bodies of the relays, the attenuator, or the cables, and the bulkhead sheetmetal.

   Remount the X axis/audio output PCB by placing it on its standoffs and replacing the screws which hold the PCB to the bulkhead. Make sure that the mounting hardware does not contact the ground planes on the PCB. Make sure that the two connectors on the rear of the PCB do not contact the bulkhead sheetmetal. Then mount the two power ICs to the bulkhead. The larger one requires an insulating pad and nylon hardware, while the smaller one mounts directly. See the assembly drawing for details. Verify that there is no electrical contact between the ground planes of the PCB and the bulkhead sheetmetal, nor between the mounting tab of the larger power IC and the sheetmetal.

5. Place the bulkhead in position behind the front panel box, leaving a little space. Plug the relay and attenuator pigtails into their respective headers on the interface PCB. The attenuator pigtail plugs onto the four pin header, the input select relay pigtail into the upper three pin header, and the band select relay into the lower three pin header.

   Plug the flexible coax cables attached to the interface PCB into the X axis/audio output PCB. The short cable goes to the X axis input (J7) at the bottom center of the PCB while the long cable goes to the beeper input (J3) at the top of the PCB. Plug the X axis output connector pigtail into the X axis output connector (J6) at the bottom edge of the PCB. Plug the video output connector pigtail into the feed-through connector inside the "L" of the PCB. Plug the Z axis control pigtail into the feed-through connector which is the far-right member of the set of four at the top of the bulkhead. Plug the BFO control pigtail into the feed-through connector adjacent to it. Plug the audio gain control and audio output jack pigtails into the PCB.

6. Slowly slide the bulkhead into the back of the front panel box. The pigtails from the relays and the attenuator must fit into the notch at the top of the bulkhead partition. The two flexible coax cables connecting the interface PCB to the X axis/audio output PCB must first go between the interface and processor PCBs, going around the processor PCB through the cut-away part of the PCB at the bottom, next to the front panel box. The cables must then go through the notch at the bottom of the partition on the bulkhead. Make sure that the RF input connectors pass through their mounting holes in the front panel.

CAUTION

BE EXTREMELY CAREFUL NOT TO PINCH THE CONNECTING WIRES AND CABLES WHEN SLIDING THE BULKHEAD INTO THE BACK OF THE FRONT PANEL ASSEMBLY. ELECTRICAL DAMAGE MAY RESULT WHEN POWER IS RE-APPLIED.

7. Replace the 12 flathead screws holding the bulkhead to the front panel can. Replace the mounting hardware holding the RF input connectors to the front panel. Note that insulating washers are required. Verify that there is no electrical contact between the connectors and the front panel sheetmetal.

5.3.6 Rear Panel Assembly Removal and Replacement

The rear panel assembly (493700) mounts to the rear of the cardcage inside a mu-metal shield, and contains the power supply. It also supports rear-panel connections for AC input, the IEEE-488 interface, and various analog and digital signal monitors.

The assembly consists of a sheet metal panel, a PCB, and assorted hardware in between.

Procedure:

1. Remove the cover. See paragraph 5.3.1.

2. Remove the mounting hardware holding the 20 MHz clock reference monitor jack to the rear panel sheetmetal. This is the only one of the monitor jacks which is fed by semi-rigid cable. Unplug the remaining flexible coax cables from their connections on the cardcage plug-in modules.

3. Remove the two screws which hold the digital connector butch plate to the rear panel.

4. Remove the four screws (one at each corner of the rear panel) which holds the rear panel to the cardcage. Gently draw the rear panel assembly slightly away from the cardcage, making sure that the 20 MHz reference monitor BNC connector and the digital connector butch plate do not bind.

5. Unplug the AC (four pin) and DC (25 pin D-sub) pigtails coming from the cardcage, from their mating connectors in the rear panel assembly.

6. Gently remove the rear panel assembly from the cardcage, drawing the flexible coax cables out through the hole in the mu-metal shield.

7. To reassemble, reverse the preceding steps. The cardcage coax cable assembly drawing (493055), provided in section 6, indicates where to reconnect the flexible coax cables in the cardcage.

5.3.7 Rear Panel Disassembly

The rear panel assembly (493700) consists of the rear panel sheetmetal, the power supply PCB, and various other hardware. The procedure given here will separate the power supply PCB from the sheetmetal, which provides easy access to all of the other hardware.

Procedure:

1. Remove the cover. See paragraph 5.3.1.

2. Remove the rear panel assembly from the cardcage. See paragraph 5.3.6.

3. Remove the hardware holding the AC line range/subrange switch to the rear panel.

4. Unplug the three slide-on connections from the rear of the AC line entry module. Unplug the power cable leading to the fan.

5. Remove the six screws holding the heatsinks to the rear panel. Remove the large bolt holding the power transformer to the rear panel.

6. Remove the power supply PCB from the rear panel. The AC line range switch will remain connected to the PCB, free-hanging. It is recommended that dummy hardware be used to hold the heatsink assemblies and the power transformer to the power supply PCB while it is being serviced.

7. To reassemble the rear panel, reverse the preceding steps.

5.4 Field Service Adjustments

In order to bring the R-110 receiver into spec after replacement of a module or assembly, or simply in the course of time, a number of trimmers must be adjusted. This may be done in the field providing adequate signal source and measurement equipment is available. Adjustment should be performed after replacing any of the signal path or synthesizer hardware in the radio, or occasionally as part of periodic maintenance. All of the adjustments are made to modules which plug into the cardcage; no adjustments are available in the front or rear panel assemblies. In order to perform adjustment on a plug-in module, a field service kit is available which provides an extender PCB and extender rods and cables which allow a module to be raised up out of the cardcage for access to its circuitry.

Performance of these adjustments do not necessarily constitute a full calibration of the receiver. Full calibration can only be assured by performing the entire acceptance test procedure (ATP) and making any adjustments required to pass it.

Field service adjustments include:

- microwave RF module (A1A1): input limiter VSWR
- preselector module (A1A2): VCO input voltage clamps for the 523 - 533 MHz synthesizer
- low frequency RF module (A1A5): none
- 21.4 MHz IF amplifier module (A1A6): front end overload, underload thresholds; AGC
- 21.4 MHz IF filter module (A1A8): back end overload threshold
- video module (A1A9): log amp null, BFO offset, Z axis offset, overload detector threshold
- DCIF module (A1A11): first stage offset
- fixed LO synthesizer module (A1A15): none
- microwave synthesizer module (A1A16): integrator bias for the programmable microwave synthesizer
- low frequency synthesizer module (A1A17): integrator bias for the synthesizer and mixer loops; mixer loop relock threshold

There is a separate procedure provided for each adjustment.

5.4.1 Microwave RF Module Input Limiter Adjustment

The input limiter is the first subassembly (A1A1A1) that the signal goes to upon entering the microwave RF module. Being the input limiter it may occasionally burn out on severe overloads and thereafter be replaced. The new subassembly will need to be tuned to minimize its VSWR. The tuning components are C3 and C4.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables and the discrete wire pigtail from the microwave module (A1A1) and remove the microwave module from the cardcage. Remove the small cover at the top left of the module, adjacent to the signal input connector.

3. Remount the microwave module in the cardcage, using extender rods, so that the circuitry revealed by the removed cover is accessible. Use extender cables to reconnect the inputs and outputs.

4. Power up the radio. Tune it to 1 GHz. Apply a CW signal at 1 GHz and amplitude below -30 dBm, through a coupler. Monitor the other output of the coupler with a spectrum analyzer or power meter.

5. Adjust C3 and C4 in the input limiter cavity to maximize the return loss measured on the signal monitor. When adjusted the VSWR should be below 2.0, so the return loss should be above 9.5 dB.

6. An artifact at 800 MHz occasionally presents itself when the input limiter is perfectly tuned at 1 GHz. Set the input signal to 800 MHz and check the return loss. It should still be above 9.5 dB. If not then it may be necessary to readjust the capacitors to strike a balance between the return loss at 800 MHz and the return loss at 1 GHz.

5.4.2 Front End Overload and Underload Threshold Adjustments

The front end overload and underload threshold adjustments are located on the 21.4 MHz IF amplifier module (A1A6). The signal is picked off after the first amplifier following the input select relay, amplified, and compared to overload and underload thresholds, each set by a trimmer. The overload threshold trimmer is R64. The underload threshold trimmer is R69.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the 21.4 MHz IF amplifier module (A1A6). Then remove the module from the cardcage. Remount it using the extender PCB and rods. Do not reconnect the coax cables.

3. Power up the radio. It should be tuned above 20 MHz. Using a signal generator, apply a 21.4 MHz unmodulated sine wave at -30 dBm to J9. Plug a 50 Ohm termination into J7. Monitor cardcage backplane interface connector P1 pin B21 with an oscilloscope or other voltage monitor. Adjust the signal generator and R64 on the module so that P1 pin B21 goes TTL low when the signal generator level is at or above -19 dBm, and TTL high when the signal generator level is below -19 dBm.

4. Monitor cardcage backplane interface connector P1 pin B20 with the voltage monitor. Adjust the signal generator and R69 on the module so that P1 pin B20 goes TTL low when the signal generator level is at or below -32 dBm, and TTL high when the signal generator level is above -32 dBm.

5.4.3 Back End IF Overload Adjustment

The back end IF overload threshold adjustment is located on the 21.4 MHz IF filter module (A1A8). The pickoff is behind the input amplifier, before the filters. Other contributors to back end overload detection are the DCIF module and the video module, which are adjusted in separate procedures. The threshold here is set by trimmer R1.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the top of the 21.4 MHz IF filter module (A1A8) and remove the module from the cardcage. Now remount it using the extender PCB and rods. Do not reconnect the coax cables.

3. Power up the radio. Apply a CW signal at 21.4 MHz and -40 dBm to J1. Monitor cardcage backplane interface connector P1 pin B18 with an oscilloscope or other signal monitor.

4. Vary the amplitude of the input signal and adjust R1 so that the voltage level at P1 pin B18 is TTL high when the input amplitude is below -34 dBm and TTL low when the input amplitude is -34 dBm or greater.

5.4.4 AGC Adjustment

The AGC adjustment is located on the 21.4 MHz IF amplifier module (A1A6). In normal use a DC signal is developed from detected video and returned here, where it is conditioned and used in combination with the front panel gain control/IEEE-488 gain command to set the first three PIN diode attenuator circuits. The adjustment is for the threshold at which the AGC kicks in. The trimmer is R100.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the top of the IF amplifier module (A1A6). Then remove the module from the cardcage and remount it using the extender PCB and rods. Do not reconnect the coax cables, but use a short coax jumper to connect J5 to J4. Make sure that trimmer R101 is set fully clockwise.

3. Power up the radio. Tune it to band 3 (any frequency over 20 MHz). Set the front panel gain control to maximum (50 dB). Enable AGC.

4. Apply a CW signal at 21.4 MHz and -70 dBm to J9. Connect a DC power supply to J6 and set it to about +3 VDC. Connect an oscilloscope or other signal monitor to J3.

5. Vary the amplitude of DC supply and observe the output on the signal monitor. Adjust R100 so that the monitored signal begins to fall off when the voltage applied to J6 rises above 3.0 VDC.

5.4.5 DCIF Offset Adjustment

Of all the adjustments on the DCIF module, only the first stage offset trim is suitable for field service. The other adjustments on the module are made during factory test and then locked.

The DCIF begins with a quadrature signal splitter and ends with a recombination circuit. In between are two identical processing channels. The gains and offsets of both channels must be matched exactly, because any error is directly related to errors in the output. (For example, a mismatch beween channels of one part in one hundred will limit the usable range of the output to 40 dB, which again is one part in one hundred. A well-adjusted module will optimally exhibit channel matching to one part in one thousand.)

There are two first stage offset adjustments, one for each channel. The trimmers are R41 and R46.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the top of the DCIF module (A1A11) and remove the module from the cardcage. Now remount the module using the extender PCB and rods. Reconnect the coax cable to J2 using a cable extender.

3. Power up the radio. Select a narrow bandwidth (20 kHz or less). Select linear detection. Apply a CW signal at 21.401 MHz and -10 dBm to J3 on the DCIF module. Monitor J5 on the module with an oscilloscope.

4. Interactively adjust R41 and R46 for minimum AC content at J5. There should be substantial DC content, however.

5.4.6 Log Detector Adjustment

The log detector is part of the video module (A1A9). It consists of a pair of log detector ICs which are connected in series to increase the dynamic range. They are followed by an output amplifier. The only adjustment available in this circuit, trimmer R6, allows the output to be nulled for zero input.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the top of the video module (A1A9) and remove the module from the cardcage. Now remount it using the extender PCB and rods. Do not reconnect the coax cables.

3. Power up the radio. Tune it to band 3 (above 20 MHz) and make sure that the selected bandwidth is 80 kHz or higher. Select log detection.

4. Monitor the main video output at J7 with an oscilloscope or other DC voltage monitor. Adjust R6 for minimum monitored output.

5.4.7 BFO Adjustment

The BFO detector is part of the video module (A1A9). It consists of a 21.4 MHz crystal oscillator, the frequency of which may be varied by a few kHz using a front panel control which sends a DC voltage to the circuit. The oscillator output is mixed with the 21.4 MHz IF and the resulting beat frequency filtered and delivered to the audio output of the module and from there to the audio output of the radio. The available adjustment is trimmer R112, which centers the adjustment range of the oscillator on 21.4 MHz.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the top of the video module (A1A9) and remove the module from the cardcage. Now remount it using the extender PCB and rods. Reconnect the coax cables to J3 and J5 using cable extenders.

3. Power up the radio. Make sure that the bandwidth is set above the DCIF range (80 kHz or above). Apply a CW signal to the radio input at a frequency which is compatible with the bandwidth (200 kHz or above) at -35 dBm or less. Tune the radio to this frequency and set the gain and attenuation to eliminate overloads. Monitor the audio output from the video module at J10. Enable BFO detection.

4. Set trimmer R112 so that the frequency deviation at J10 with the BFO control knob fully counterclockwise is the same as the deviation with the control fully clockwise, with a null in between.

5.4.8 Z Axis Output Adjustment

The Z axis inverter and output circuit are part of the video module (A1A9). Output amplitude is set by a front panel control which sends a DC voltage to the circuit. Inversion is carried out by an analog multiplier which multiplies the signal by plus or minus the amount indicated by the front panel control. A trimmer (R63) is provided to minimize the output when the front panel control is set fully counterclockwise.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the top of the video module (A1A9) and remove the module from the cardcage. Now remount the module using the extender PCB and rods. Reconnect the coax cable to J4 using an extender cable.

3. Power up the radio. Apply a CW signal at 21.4 MHz and 0 dBm, with 1 kHz AM modulation, to module connector J3. Tune the radio to band 3 (above 20 MHz) and at least 80 kHz bandwidth. Enable the Z axis output. Monitor the Z axis output at J9 with an oscilloscope.

4. Set the front panel Z axis control fully counterclockwise. Now adjust trimmer R63 to null the output seen on the oscilloscope.

5.4.9 Video Overload Threshold Adjustment

The adjustment is trimmer R44 on the video module (A1A9). The output of the main video amplifier is compared to a reference set by the trimmer.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the top of the video module (A1A9) and remove it from the cardcage. Now remount it using the extender PCB and rods. Do not reconnect the coax cables.

3. Power up the radio. Select a narrow bandwidth (20 kHz or less) and linear detection. Monitor cardcage backplane interface connector P1 pin B18 with an oscilloscope.

4. Apply 5.125 VDC to the narrowband input (J2) of the video module. Now adjust R44 so that the output at P1 pin B18 just breaks between TTL high and TTL low.

5.4.10 Programmable Microwave Synthesizer Adjustment

The VCO for the programmable microwave synthesizer is located in the microwave RF module (A1A1). The rest is located on the microwave synthesizer module (A1A17). The loop contains an adjustment (R30 on the microwave synthesizer module) to adjust the DC offset on the loop integrator. The offset affects the reference sidebands in the output of the loop.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax connections from the top of the microwave synthesizer module (A1A17) and remove it from the cardcage. Now remount it using the extender PCB and rods. Reconnect the coax cables using cable extenders.

3. Power up the radio. Tune it to 20 MHz. Select external wideband operation (one of the bandwidth mode selections). Connect a spectrum analyzer to the external wideband connector on top of the microwave RF module (J4).

4. Locate the LO artifact at 1470 MHz on the spectrum analyzer. Observe the reference sidebands spaced 625 kHz around it. Now adjust R30 on the microwave synthesizer module to minimize these reference sidebands. They should null to better than -60 dBc.

5.4.11 523 - 533 MHz Mixer Loop Adjustment

The VCO for this synthesizer is located in the microwave RF module (A1A1). The rest of the loop is located on the preselector module (A1A2). The 2 GHz fixed LO is divided by four to produce 500 MHz, which is then subtracted from the loop VCO output and the result compared to the programmable low frequency synthesizer output. The 2 GHz and settable low frequency references come from elsewhere. The loop features clamping of the VCO tune voltage at both the high and low ends to keep it within lock range. The components to be adjusted are R13 and R14 on the main preselector PCB, which are used to set the clamp voltages.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the preselector module (A1A2). Then remove the preselector module from the cardcage. Remount it using the extender PCB and rods. Do not reconnect the coax cables.

3. Power up the radio. Tune it to band 3 (above 20 MHz). Connect a DC source to microwave module J8. Monitor microwave RF module J7 with a frequency counter or spectrum analyzer.

4. Characterize the VCO by determining the tuning voltages at which the VCO outputs 518 MHz and 540 MHz. Record these voltages.

5. Monitor U3 pin 7 on the preselector module main PCB with a DVM. Adjust R14 so that the voltage at U3 pin 7 matches the 540 MHz VCO tune voltage.

6. Monitor U3 pin 1 with the DVM. Adjust R13 so that the voltage at U3 pin 1 matches the 518 MHz VCO tune voltage.

5.4.12 Low Frequency Synthesizer Adjustment

The programmable low frequency synthesizer consists of a double loop, one programmable in 1 MHz steps and the other to mix the output of the first one with the output of the direct digital synthesizer (DDS). All of this is located on the low frequency synthesizer module (A1A16). There is an offset adjustment (R36) for the programmable loop integrator, which is used to minimize the reference sidebands in the output of the loop. The mixer loop has a similar adjustment (R58), plus a threshold adjustment (R68) for a kickout circuit which will reset the VCO tune voltage if it goes out of acceptable range.

Procedure:

1. Remove the cover from the radio. See paragraph 5.3.1.

2. Unplug the coax cables from the top of the low frequency synthesizer module (A1A16) and remove the module from the cardcage. Then remount the module using the extender PCB and rods. Reconnect the coax cables using cable extenders.

3. Remove IC U21 from the low frequency synthesizer module. This is the integrator for the mixer loop. Connect a 10k resistor from pin 4 to pin 6 of the U21 socket. Now power up the radio and tune it to 7.5 MHz. Connect a spectrum analyzer to an unused output of the programmable loop VCO (A1A16A1 subassembly, pin 2 or pin 4).

4. Find the programmable loop VCO output at 29.9 MHz on the spectrum analyzer. Observe the reference sidebands 1 MHz away from the main output. Adjust R36 to minimize the reference sidebands.

5. Power down the radio. Remove the 10k resistor from the U21 socket and replace the IC. Power up the radio and tune it to 7.5 MHz. Connect the spectrum analyzer to low frequency synthesizer module J3.

6. Find the mixer loop VCO output at 28.9 MHz on the spectrum analyzer. Observe the reference sidebands 1 MHz away from the main output. Adjust R58 to minimize the reference sidebands.

7. Tune the radio to 270 kHz. Select the 1 kHz digit for tuning and, using the tuning knob and pushbuttons BUT NOT THE KEYPAD, step the tuned frequency down to 225 kHz WITHOUT OVERSHOOTING. This sets the low frequency synthesizer to its minimum frequency, which is at the bottom of the hysteresis region at the bottom of band 2.

8. Measure the tuning voltage on the mixer loop VCO (A1A16A2 subassembly, pin 8, or U21 pin 6 on the main low frequency synthesizer module PCB). Now monitor U23 pin 2 on the low frequency synthesizer module main PCB with a DVM. Adjust R68 to set the voltage at U23 pin 2 to 0.8 Volts lower than the measured tuning voltage.