APPENDIX B. HARDWARE ADDRESS MAP

B.1 Introduction

The R-110 uses an 80C31 microprocessor. This part supports two external address spaces, one for instructions and one for data. Data addresses are read/write, while instruction addresses are read only. Each address space may be up to 64k bytes (65536 locations, each eight bits wide) in size, using sixteen address bits. The board (A2A3) which contains the processor also provides configuration jumpers which makes it possible to merge the upper half of each space for common access, or to keep them totally separate. When merged, instructions may be downloaded from an external source and written into memory as data, and then executed as instructions. As currently implemented the upper halves are merged, but when code size exceeds 32k the other configuration will be required.

This memory map shows how hardware in the radio is allocated to the two address spaces in the merged configuration. In the separated configuration everything remains the same except that the instruction address space is devoted exclusively to the EPROM.

B.2 I/O Configuration

The address decoding hardware on the processor board (A2A3) allocates a segment of 256 data addresses for I/O functions (everything else is some sort of memory). A physical I/O bus is implemented, leading to the interface board (A2A2) and from there to the displays on the display board (A2A1) and the cardcage backplane (A1A20), where the various cardcage boards can connect to it. In this appendix the allocation of the I/O bus will be indicated in the main data address map and then will be given its own map, using eight bit addresses. To determine the address the processor uses to access a particular address on the I/O bus, preface the I/O address with 7F(hex).

B.3 Hexadecimal Addressing

Addresses dealt with here are either eight or sixteen bits long. The number system which best lends itself to binary numbers of this size is hexadecimal, which is base 16. In this system numbering begins with zero through nine, and continues to the equivalent of fifteen with the first three letters of the alphabet. Either upper or lower case letters are permitted.

For example:

0(hex) = 0(decimal)
9(hex) = 10(decimal)
A(hex) = 10(decimal)
F(hex) = 15(decimal)
10(hex) = 16(decimal)
1F(hex) = 31(decimal)
20(hex) = 32(decimal)
FF(hex) = 255(decimal)
100(hex) = 256(decimal)
FFFF(hex) = 65535(decimal)

B.4 Code Address Map

Address 0000(hex) - 7FFF(hex) = EPROM (fixed instruction memory)

Address 8000(hex) - FFFF(hex) = RAM (volatile data or instruction memory)

Note: in non-merged configuration the entire code address space, 0000(hex) - FFFF(hex) is assigned to EPROM, and RAM is unavailable for execution of instructions.

B.5 Data Address Map

Address 0000(hex) - 7EFF(hex) = EEPROM (nonvolatile data memory)

Address 7F00(hex) - 7FFF(hex) = I/O bus (see separate map)

Address 8000(hex) - FFFF(hex) = RAM (volatile data or instruction memory)

Note: in non-merged configuration the RAM space is not usable as instruction memory.

B.6 I/O Bus Address Map

These are the 256 addresses identified as the I/O bus in the preceding paragraph. They are listed with eight bit addresses. The full address is the eight bit addressed prefaced by 7F(hex), for example, I/O address 80(hex) = data address 7F80(hex).

For a particular I/O address, the hardware peripheral assigned to it may allocate specific data bits for different purposes. Bit allocations will be given for those addresses which require it. As listed, bit zero is the least significant bit on the data bus, while bit 7 is the most significant.

In some instances there is redundant mapping. This means that a single hardware peripheral port was mapped into multiple (contiguous) addresses on the I/O bus. This is normally done to simplify the design of the decoding hardware. It wastes addresses, but at present there is a surplus. Peripheral ports which are redundantly mapped may be accessed through any of the assigned addresses, with no difference in effect between one and another.

In addition, some notes pertaining to the states of the bits are often provided.

Since the overall map is fairly extensive it will be presented in pieces according to the assemblies associated with it. The first half of the address space is allocated to the cardcage cards. All of these addresses are therefore write only, since no provision is made for reading from the cardcage. The upper half of the address space is allocated to the front panel assembly, and may be either written to or read from.

B.6.1 Low Frequency Synthesizer Module (A1A16)

This board uses the Qualcomm Q2334 direct digital synthesizer (DDS). It contains two separate but identical synthesizer circuits. See the manufacturer's application notes for more information.

Address 00(hex) - 1F(hex) = Q2334 direct digital synthesizer (write only)
Address 00(hex) = synthesizer #1 phase increment latch A bits 0 - 7
Address 01(hex) = synthesizer #1 phase increment latch A bits 8 - 15
Address 02(hex) = synthesizer #1 phase increment latch A bits 16 - 23
Address 03(hex) = synthesizer #1 phase increment latch A bits 24 - 31
DDS frequency in Hz = phase increment code / 214.7483648
Address 04(hex) = synthesizer #1 phase increment latch B bits 0 - 7
Address 05(hex) = synthesizer #1 phase increment latch B bits 8 - 15
Address 06(hex) = synthesizer #1 phase increment latch B bits 16 - 23
Address 07(hex) = synthesizer #1 phase increment latch B bits 24 - 31
Address 08(hex) = synthesizer #1 synchronous mode control latch
Address 09(hex) = reserved by Q2334
Address 0A(hex) = synthesizer #1 asynchronous mode control latch
Address 0B(hex) = reserved by Q2334
Address 0C(hex) = synthesizer #1 accumulator reset
Address 0D(hex) = reserved by Q2334
Address 0E(hex) = synthesizer #1 asynchronous hop clock
Address 0F(hex) = reserved by Q2334
Address 10(hex) = synthesizer #2 phase increment latch A bits 0 - 7
Address 11(hex) = synthesizer #2 phase increment latch A bits 8 - 15
Address 12(hex) = synthesizer #2 phase increment latch A bits 16 - 23
Address 13(hex) = synthesizer #2 phase increment latch A bits 24 - 31
Address 14(hex) = synthesizer #2 phase increment latch B bits 0 - 7
Address 15(hex) = synthesizer #2 phase increment latch B bits 8 - 15
Address 16(hex) = synthesizer #2 phase increment latch B bits 16 - 23
Address 17(hex) = synthesizer #2 phase increment latch B bits 24 - 31
Address 18(hex) = synthesizer #2 synchronous mode control latch
Address 19(hex) = reserved by Q2334
Address 1A(hex) = synthesizer #2 asynchronous mode control latch
Address 1B(hex) = reserved by Q2334
Address 1C(hex) = synthesizer #2 accumulator reset
Address 1D(hex) = reserved by Q2334
Address 1E(hex) = synthesizer #2 asynchronous hop clock
Address 1F(hex) = reserved by Q2334

Data to the asynchronous hop clock is unimportant, since the write strobe acts as a trigger to the IC. The control latch for the phase locked loop which operates in conjunction with the DDS is also mapped to this address, and the data written is used to set the PLL frequency. In this manner, both parts of the synthesizer can be updated at the same time.

Address 0E(hex) = back end phase locked loop control latch (write only)
Bits 0 - 5 = phase locked loop divide code
Frequency in MHz = code + 1, from 19 - 38 MHz
Bits 6 - 7 = tuning band select code
Code 0 = band 1 select
Code 1 = band 2 select
Code 2 = band 3 select
Code 3 = unused

B.6.2 DCIF Module (A1A11)

Address 40(hex) - 43(hex) = DCIF timebase counter-timer (write only)
Address 40(hex) = counter-timer circuit 0 data
Address 41(hex) = counter-timer circuit 1 data
Address 42(hex) = counter-timer circuit 2 data
Address 43(hex) = counter-timer mode

The DCIF timebase counter-timer is an 82C54, available from several manufacturers. See their application notes for more information.

Address 44(hex) = DCIF I channel gain control DAC #1 low data (write only)
Bits 0 - 7 = DCIF I channel gain control DAC #1 bits 0 - 7
Address 45(hex) = DCIF I channel gain control DAC #1 high data (write only)
Bits 0 - 3 = DCIF I channel gain control DAC #1 bits 8 - 11
Bits 4 - 7 = spare

Address 46(hex) = DCIF Q channel gain control DAC #1 low data (write only)
Bits 0 - 7 = DCIF Q channel gain control DAC #1 bits 0 - 7
Address 47(hex) = DCIF Q channel gain control DAC #1 high data (write only)
Bits 0 - 3 = DCIF Q channel gain control DAC #1 bits 8 - 11
Bits 4 - 7 = spare

Address 48(hex) = DCIF I channel gain control DAC #2 low data (write only)
Bits 0 - 7 = DCIF I channel gain control DAC #2 bits 0 - 7
Address 49(hex) = DCIF I channel gain control DAC #2 high data (write only)
Bits 0 - 3 = DCIF I channel gain control DAC #2 bits 8 - 11
Bits 4 - 7 = spare

Address 4A(hex) = DCIF Q channel gain control DAC #2 low data (write only)
Bits 0 - 7 = DCIF Q channel gain control DAC #2 bits 0 - 7
Address 4B(hex) = DCIF Q channel gain control DAC #2 high data (write only)
Bits 0 - 3 = DCIF Q channel gain control DAC #2 bits 8 - 11
Bits 4 - 7 = spare

Address 4C(hex) = DCIF control latch (write only)
Bit 0 = filter #1 and filter #3 clock ratio select
0 = 100:1
1 = 50:1
Bit 1 = filter #2 clock ratio select
0 = 150:1
1 = 75:1
Bit 2 = DCIF input select
0 = linear mode IF tap
1 = log mode IF tap
Bit 3 = clock receiver and overload status driver enable (set = enable)
Bits 4 - 7 = spare

Address 4D(hex) = DCIF gain control DAC load strobe (data unimportant) (write only)

B.6.3 21.4 MHz IF Amplifier Module (A1A6)

Address 50(hex) = IF gain control DAC #1 low data (write only)
Bits 0 - 7 = IF gain control DAC #1 bits 0 - 7
Address 51(hex) = IF gain control DAC #1 high data (write only)
Bits 0 - 3 = IF gain control DAC #1 bits 8 - 11
Bits 4 - 7 = spare

Address 52(hex) = IF gain control DAC #2 low data (write only)
Bits 0 - 7 = IF gain control DAC #2 bits 0 - 7
Address 53(hex) = IF gain control DAC #2 high data (write only)
Bits 0 - 3 = IF gain control DAC #2 bits 8 - 11
Bits 4 - 7 = spare

Address 54(hex) = IF gain control DAC #3 low data (write only)
Bits 0 - 7 = IF gain control DAC #3 bits 0 - 7
Address 55(hex) = IF gain control DAC #3 high data (write only)
Bits 0 - 3 = IF gain control DAC #3 bits 8 - 11
Bits 4 - 7 = spare

Address 56(hex) = IF gain control DAC #4 low data (write only)
Bits 0 - 7 = IF gain control DAC #4 bits 0 - 7
Address 57(hex) = IF gain control DAC #4 high data (write only)
Bits 0 - 3 = IF gain control DAC #4 bits 8 - 11
Bits 4 - 7 = spare

Address 58(hex) = gain control DAC load strobe (data unimportant) (write only)

Address 59(hex) = IF control latch (write only)
Bits 0 - 2 = bandwidth select code
Code 0 = 15 MHz bandwidth select
Code 1 = reserved for 8 MHz bandwidth select
Code 2 = 4 MHz bandwidth select
Code 3 = 1 MHz bandwidth select
Code 4 = 300 kHz bandwidth select
Code 5 = 80 kHz bandwidth select
Code 6 = spare
Code 7 = wideband select
Bit 3 = bandwidth enable (set = enable bandwidth selection)
Bit 4 = high/low band select
0 = high band
1 = low band
Bit 5 = band 1/2 select
0 = band 2
1 = band 1
Bit 6 = AGC enable (set = enable)
Bit 7 = spare

B.6.4 Fixed LO Synthesizer Module (A1A15)

Address 70(hex) = fixed oscillator and DCIF timebase control (write only)
Bit 0 = band 1 enable (set = enable)
Bit 1 = DCIF phase locked loop enable (set = enable)
Bits 2 - 7 = spare

Address 71(hex) = DCIF phase locked loop divider (write only)
Bits 0 - 7 = DCIF phase locked loop divider code
Frequency = (255 - code) * 50 kHz

B.6.5 Microwave Synthesizer Module (A1A17)

Address 78(hex) = microwave synthesizer skip counter (write only)
Bits 0 - 3 = microwave synthesizer skip counter code
Code = (frequency / 5 MHz) MOD 10
where "MOD" is the remainder from dividing by 10
Bit 4 = spare
Bit 5 = band 3 enable (clear = enable)
Bits 6 - 7 = spare

Address 79(hex) = microwave synthesizer divider (write only)
Bits 0 - 7 = microwave synthesizer divider code
Code = [(frequency / 5 MHz) DIV 10] - 1
where "DIV" is truncated integer division

B.6.6 Video Module (A1A9)

Address 7E(hex) = video control latch 0 (write only)
- Bit 0 = 4 MHz video filter enable (set = enable)
- Bit 1 = 400 kHz video filter enable (set = enable)
- Bit 2 = 40 kHz video filter enable (set = enable)
- Bit 3 = 4 kHz video filter enable (set = enable)
- Bit 4 = log detector input select
  - 0 = DCIF input
  - 1 = 21.4 MHz IF input
- Bit 5 = log/linear detector select
  - 0 = linear detector
  - 1 = log detector
- Bit 6 = video output select
  - 0 = processed 21.4 MHz IF
  - 1 = processed DCIF
- Bit 7 = spare

Address 7F(hex) = video control latch 1 (write only)
- Bit 0 = BFO enable (set = enable)
- Bit 1 = Z axis enable (set = enable)
- Bit 2 = Z axis invert (set = invert)
- Bit 3 = reserved for slideback enable
- Bit 4 = reserved for pulse stretch enable
- Bits 5 - 7 = spare

B.6.7 Processor PCB (A2A3)

Address 80(hex) - 83(hex) = dipswitch (redundant mapping) (read only)
- Bit 0 = switch #1 ("on" = 0, "off" = 1)
- Bit 1 = switch #2
- Bit 2 = switch #3
- Bit 3 = switch #4
- Bit 4 = switch #5
- Bit 5 = switch #6
- Bit 6 = switch #7
- Bit 7 = switch #8

Address 80(hex) - 83(hex) = external counter-timer interrupt request clear (redundant mapping) (write only) (data is unimportant to clearing the request, but is used by the other write function mapped here -- see below)

Address 80(hex) - 83(hex) = serial port receive data select (redundantly mapped) (write only) (this write address is also used by another write function -- see above)
- Bit 0 = data select
  - 0 = RS-232
  - 1 = serial data from cardcage
- Bits 1 = 7 = spare

Address 84(hex) - 87(hex) = external counter-timer ports
Address 84(hex) = counter-timer circuit 0 data (read/write)
Address 85(hex) = counter-timer circuit 1 data (read/write)
Address 86(hex) = counter-timer circuit 2 data (read/write)
Address 87(hex) = counter-timer status (read)
Address 87(hex) = counter-timer mode (write)

The external counter-timer is an 82C54, available from several manufacturers. See their application notes for more information.

Address 88(hex) - 8F(hex) = IEEE-488 controller ports
Address 88(hex) = interrupt request status 0 (read)
Address 88(hex) = interrupt mask 0 (write)
Address 89(hex) = interrupt request status 1 (read)
Address 89(hex) = interrupt mask 1 (write)
Address 8A(hex) = address status (read only)
Address 8B(hex) = bus status (read)
Address 8B(hex) = auxiliary command (write)
Address 8C(hex) = controller address (write only)
Address 8D(hex) = serial poll data (write only)
Address 8E(hex) = command pass-through (read)
Address 8E(hex) = parallel poll configuration (write)
Address 8F(hex) = data in (read)
Address 8F(hex) = data out (write)

The IEEE-488 controller is a Texas Instruments TMS9914A. See the manufacturer's application notes for more information.

B.6.8 Interface PCB (A2A2)

Address B0(hex) = LED latch 0 (write only)
Bit 0 = RF input indicator select
0 = RF input #1 select indicator
1 = RF input #2 select indicator
Bits 1 - 7 = spare

Address B1(hex) = LED latch 1 (write only)
Bit 0 = spare indicator (left end of attenuation display)
Bit 1 = autorange indicator
Bit 2 = AGC indicator
Bit 3 = absolute gain indicator
Bit 4 = delta gain indicator
Bit 5 = CW gain indicator
Bit 6 = wideband mode indicator
Bit 7 = spare indicator (right end of bandwidth display)

Address B2(hex) = LED latch 2 (write only)
Bits 0 - 3 = operating mode indicator code
Code 0(hex) = tune mode indicator
Code 1(hex) = start mode indicator
Code 2(hex) = stop mode indicator
Code 3(hex) = step mode indicator
Code 4(hex) = rate mode indicator
Code 5(hex) = scan mode indicator
Code 6(hex) = store mode indicator
Code 7(hex) = recall mode indicator
Code 8(hex) = GPIB mode indicator
Code 9(hex) = remote mode indicator
Codes A(hex) - F(hex) = spare
Bit 4 = select left indicator
Bit 5 = select step indicator
Bit 6 = select right indicator
Bit 7 = AC high indicator

Address B3(hex) = LED latch 3 (write only)
Bit 0 = AC low indicator
Bit 1 = DC regulation indicator
Bit 2 = unlock indicator
Bit 3 = front end overload indicator
Bit 4 = back end overload indicator
Bit 5 = bandwidth limit indicator
Bit 6 = step gap indicator
Bit 7 = downconverter mode indicator

Address B4(hex) = LED latch 4 (write only)
Bit 0 = reserved for slideback enable indicator
Bit 1 = reserved for pulse stretch enable indicator
Bit 2 = BFO enable indicator
Bit 3 = Z axis output enable indicator
Bit 4 = Z axis invert enable indicator
Bit 5 = alternate function select pending indicator
Bit 6 = reserved for alternate video detector enable indicator
Bit 7 = log video enable indicator

Address B5(hex) = rear panel status latch 0 (write only)
Bits 0 - 7 = rear panel processor status bits 0 - 7

Address B6(hex) = rear panel status latch 1 (write only)
Bits 0 - 7 = rear panel processor status bits 8 - 15

Address B7(hex) = front panel RF control latch (write only)
Bits 0 - 2 = input attenuation code
Code 0 = 0 dB
Code 1 = 10 dB
Code 2 = 20 dB
Code 3 = 30 dB
Code 4 = 40 dB
Code 5 = 50 dB
Code 6 = 60 dB
Code 7 = 70 dB
Bit 3 = reserved for GLI control
Bits 4 - 5 = RF input select code
Code 0 = no change
Code 1 = RF input #1 select
Code 2 = RF input #2 select
Code 3 = illegal
Bits 6 - 7 = high/low band select code
Code 0 = no change
Code 1 = band #1/2 select
Code 2 = band 3 select
Code 3 = illegal

Address B8(hex) = button buffer 0 (read)
Bits 0 - 3 = keypad code
Code 0(hex) = "C" key
Code 1(hex) = "M" key
Code 2(hex) = "K" key
Code 3(hex) = "H" key
Code 4(hex) = "." key
Code 5(hex) = "9" key
Code 6(hex) = "8" key
Code 7(hex) = "7" key
Code 8(hex) = "6" key
Code 9(hex) = "5" key
Code A(hex) = "4" key
Code B(hex) = "3" key
Code C(hex) = "2" key
Code D(hex) = "1" key
Code E(hex) = "0" key
Code F(hex) = no key
Bit 4 = select left key
Bit 5 = select step key
Bit 6 = select right key
Bit 7 = alternate function enable key
Address B8(hex) = X axis DAC low port and X axis DAC strobe(write)
Bits 0 - 7 = X axis DAC bits 0 - 7

Address B9(hex) = button buffer 1 (read)
- Bit 0 = RF input #1 select key
- Bit 1 = RF input #2 select key
- Bit 2 = attenuation up key
- Bit 3 = attenuation down key
- Bit 4 = bandwidth up key
- Bit 5 = bandwidht down key
- Bit 6 = tune up key
- Bit 7 = tune down key

Address B9(hex) = X axis DAC high port (write)
- Bits 0 - 3 = X axis DAC bits 8 - 11
- Bits 4 - 7 = spare

Address BA(hex) = button buffer 2 (read)
- Bit 0 = reserved for slideback enable key
- Bit 1 = reserved for pulse stretch enable key
- Bit 2 = BFO enable key
- Bit 3 = Z axis output enable key
- Bit 4 = Z axis invert enable key
- Bit 5 = reserved for alternate detector select key
- Bit 6 = log/linear detector select key
- Bit 7 = spare

Address BA(hex) = beep headphone volume DAC port (write)
- Bits 0 - 7 = beep headphone volume DAC bits 0 - 7

Address BB(hex) = shaft encoder buffer (read)
- Bit 0 = gain encoder direction (set = clockwise)
- Bit 1 = gain encoder rotation (set = new rotation detected)
- Bit 2 = tune encoder direction (set = clockwise)
- Bit 3 = tune encoder rotation (set = new rotation detected)
- Bits 4 - 7 = spare

Address BB(hex) = beep transducer volume DAC port (write)
- Bits 0 - 7 = beep transducer volume DAC bits 0 - 7

Address BC(hex) = cardcage status buffer 0 (read)
- Bit 0 = combined lock status (clear = all locked)
- Bit 1 = combined front end overload (clear = no overload)
- Bit 2 = combined back end overload (clear = no overload)
- Bit 3 = front end underload (clear = no underload)
- Bit 4 = spare
- Bit 5 = video overload (clear = no overload)
- Bit 6 = DCIF overload (clear = no overload)
- Bit 7 = IF overload (clear = no overload)

Address BC(hex) = short beep trigger (write) (data unimportant)

Address BD(hex) = cardcage status buffer 1 (read)
Bit 0 = RF overload (clear = no overload)
Bit 1 = variable MW synthesizer lock status (clear = locked)
Bit 2 = 2 GHz synthesizer lock status (clear = locked)
Bit 3 = 530 MHz synthesizer lock status (clear = locked)
Bit 4 = back end synthesizer lock status (clear = locked)
Bit 5 = mixer lock status (clear = locked)
Bit 6 = 21.4 MHz synthesizer lock status (clear = locked)
Bit 7 = DCIF timebase synthesizer lock status (clear = locked)
Address BD(hex) = long beep trigger (write) (data unimportant)

Address BE(hex) = power supply status buffer (read only)
Bit 0 = AC line high (clear = within tolerance)
Bit 1 = AC line low (clear = within tolerance)
Bit 2 = DC regulation (clear = all voltages within tolerance)
Bit 3 = spare power supply status
Bit 4 = spare cardcage status
Bit 5 = spare cardcage status
Bits 6 - 7 = spare

B.6.9 Switch/Display PCB (A2A1)

Addresses used by components on the display board are partly decoded by logic on the interface board (A2A2). The tuning displays are Siemens PD3535, 4 character alphanumeric LED displays. The other displays are Siemens PD2435, which are similar but smaller in size. See the manufacturer's application notes for more information.

Address C0(hex) - C7(hex) = tuning display 0 (the rightmost 4 characters)
Address C0(hex) - C3(hex) = control port (redundantly mapped) (read/write)
Address C4(hex) = character 0 port (rightmost of 4) (read/write)
Address C5(hex) = character 1 port (read/write)
Address C6(hex) = character 2 port (read/write)
Address C7(hex) = character 3 port (leftmost of 4) (read/write)

Address C8(hex) - CF(hex) = tuning display 1 (the middle 4 characters)
Address C8(hex) - CB(hex) = control port (redundantly mapped) (read/write)
Address CC(hex) = character 0 port (rightmost of 4) (read/write)
Address CD(hex) = character 1 port (read/write)
Address CE(hex) = character 2 port (read/write)
Address CF(hex) = character 3 port (leftmost of 4) (read/write)

Address D0(hex) - D7(hex) = tuning display 3 (the leftmost 4 characters)
Address D0(hex) - D3(hex) = control port (redundantly mapped) (read/write)
Address D4(hex) = character 0 port (rightmost of 4) (read/write)
Address D5(hex) = character 1 port (read/write)
Address D6(hex) = character 2 port (read/write)
Address D7(hex) = character 3 port (leftmost of 4) (read/write)

Address D8(hex) - DF(hex) = attenuation display (4 characters)
Address D8(hex) - DB(hex) = control port (redundantly mapped) (read/write)
Address DC(hex) = character 0 port (rightmost of 4) (read/write)
Address DD(hex) = character 1 port (read/write)
Address DE(hex) = character 2 port (read/write)
Address DF(hex) = character 3 port (leftmost of 4) (read/write)

Address E0(hex) - E7(hex) = gain display (4 characters)
Address E0(hex) - E3(hex) = control port (redundantly mapped) (read/write)
Address E4(hex) = character 0 port (rightmost of 4) (read/write)
Address E5(hex) = character 1 port (read/write)
Address E6(hex) = character 2 port (read/write)
Address E7(hex) = character 3 port (leftmost of 4) (read/write)

Address E8(hex) - EF(hex) = bandwidth display (4 characters)
Address E8(hex) - EB(hex) = control port (redundantly mapped) (read/write)
Address EC(hex) = character 0 port (rightmost of 4) (read/write)
Address ED(hex) = character 1 port (read/write)
Address EE(hex) = character 2 port (read/write)
Address EF(hex) = character 3 port (leftmost of 4) (read/write)

Address F0(hex) - FF(hex) = reserved for DVM display

B.6.10 Unused Addresses

The following segments of the I/O address space are currently unused. Note that that addresses 00(hex) - 7F(hex) are cardcage addresses, which are write-only. Some addresses, while not assigned in the memory map, are nevertheless decoded by hardware to the point where a card will be partly enabled. These addresses are omitted from this list.

Address 20(hex) - 3F(hex)

Address 60(hex) - 6F(hex)

Address 90(hex) - AF(hex)

Address B0(hex) - B7(hex) (only read is unused)

Address BE(hex) (only write is unused)

Address BF(hex)