6. Repair of the faulty subassembly

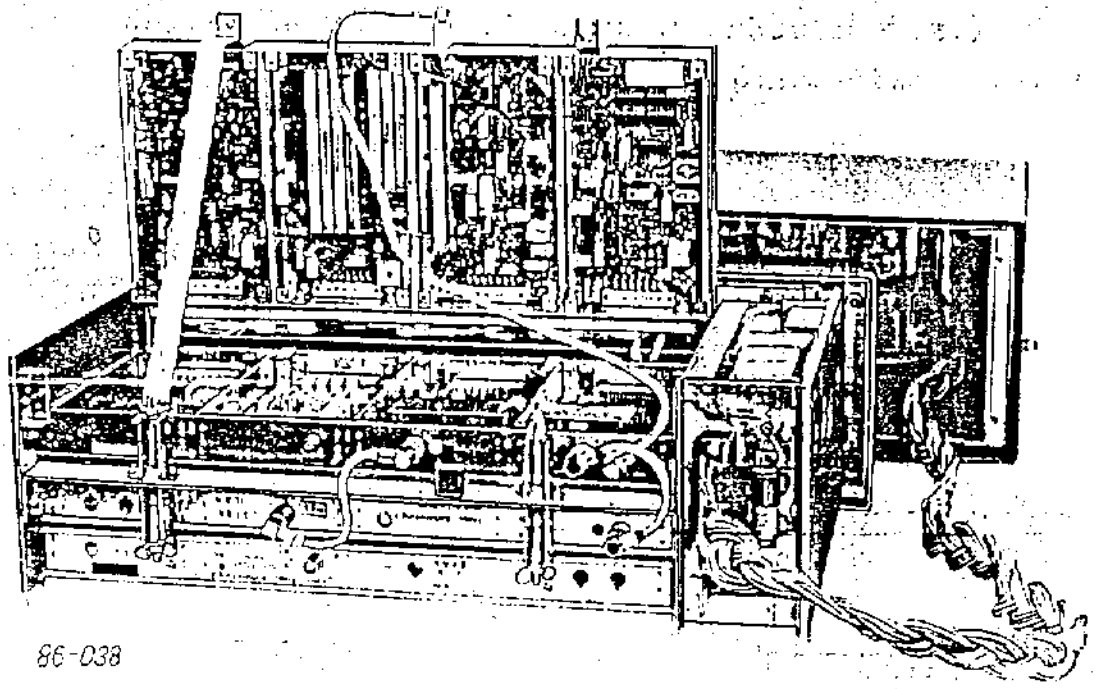


Figure 4

Service work on the cassettes of the signal path (SW1 and SW2) or on the cassettes of the frequency processing (FA1 and FA2)

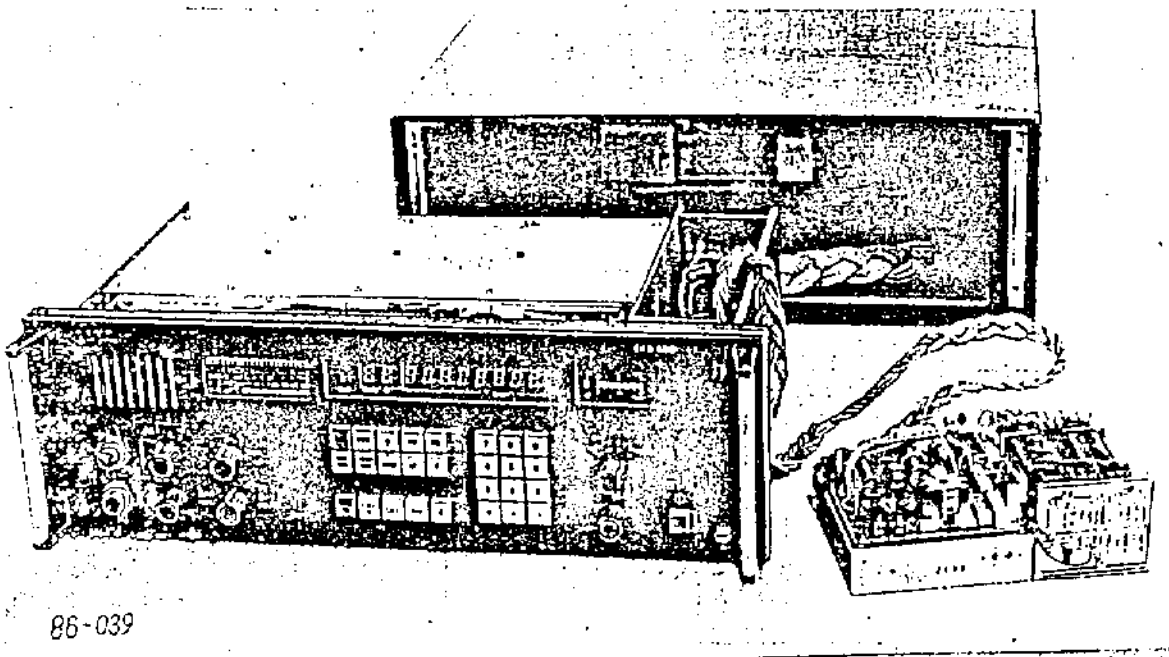


Figure 5

Unit arrangement for service work on the power supply section

6.1. Power supply section 1340.039-01500

6.1.1. Input and output values

EKD: f_E = 2.00 kHz

B_R8E, channel A

medium volume, $I_{\sqcap\!\sqcup}$ = 40 mA

Power consumption of the entire unit

Current measurements with PB at U_{rated} in the mains- or battery lead.

All indicated current values are approximate ones.

Mains operation:	~ 127 V ac	:	approx. 400 mA
	~ 220 V ac	:	approx. 230 mA
Battery operation:	⎓ 24 V dc	:	approx. 1.5 A
	⎓ 12 V dc	:	approx. 3.0 A

Output voltages

For measuring or correction:

Operate the plug-in outside the casing via the 30-core adapter cable (accessories).

Measurement with P6 at the measuring points according to Figure 1

+18 V	:	at X1001/A7, B7
+22 V	:	at X1003/A7, B7
-12 V	:	at X1003/A5, B5
+5 V	:	at X1004/A1, A2

Fine corrections only after an operating time of the receiver of = 30 min.

+18 V	±	100 mV	correction with R 5213	(I = approx. 650 mA)
+5 V	±	20 mV	correction with R 5217	(I = approx. 1.2 A)
-12 V	±	50 mV	correction with R 5114	(I = approx. 250 mA)
+22 V	-	2 V	-	(I = approx. 70 mA)

Check current load before every correction.

Hum voltages of the output voltages

The ripple is to be measured with load and 220 V ac input voltage by means of P6 (peak-to-peak value).

+18 V path	:	≤ 30 mV	(20 kHz)
+5 V path	:	≤ 50 mV	(20 kHz)
-12 V path	:	≤ 20 mV	(100 Hz or noise)
+22 V path	:	≤ 50 mV	(20 kHz +100 Hz)

Control behaviour

With change of the input voltage by±10 %, the variations of the individual output voltages - measured with P9, amount to:

+18 V path	:	ΔU	= 60 mV
+5 V path	:	ΔU	= 20 mV
-12 V path	:	ΔU	= 10 mV

The input voltage variation is to be simulated with the adjustable transformer (? 12).

6.1.2. Measuring values within the power supply divider

measured with mains operation 220 V and load

Rectifier voltages

+18/+5 V path

(measured at C 5003) : approx. 30 V

-12 V path

(measured at C 5105) : approx. 20 V

Additional voltage for 22 V path

(measured at C 5108) : approx. 4 V

Overcurrent limitation

The +18 V-, +5 V-, and -12 V path are provided each with a permanently adjusted current limitation.
This current limitation is to be checked by an additional load (slide resistor (R1) 100 ⟶ 0 ohm).

Fault

	Sweep current	s-c current
+18 V path	approx. 2 A	≡ 2.5 A
+5 V path	approx. 3 A	≡ 4 A
-12 V path	approx. 0.4 A	≡ 0.25 A

Shorting the +18 V- and +5 V paths causes switching controller noises in the audible range.

Curve shape

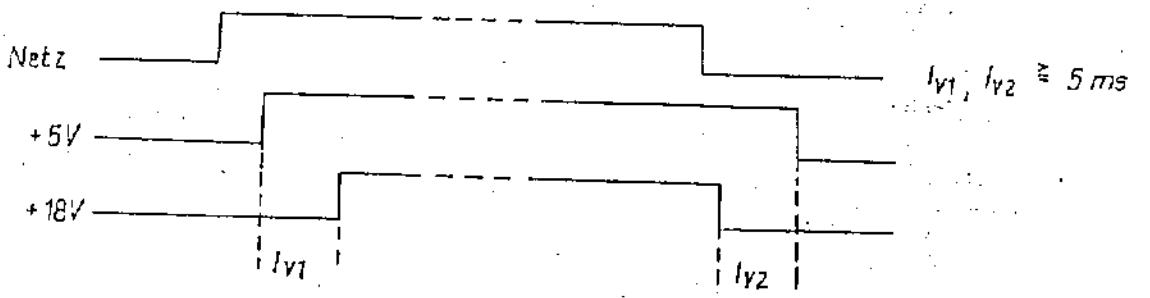
At the test points P01 to P06 indicated in the circuit diagram the prescribed curve shapes shall be detected with P6.

Working frequency

The transverter operates at rated voltage with a frequency of roughly 80 Hz.
It greatly depends on the input voltage.
The switching controller is to be adjusted to 20 kHz ± 3 kHz by means of R 5227.

Closing behaviour

The unit-specific time sequence of the partial voltages in case of ON and OFF switching is the precondition for the functionability of the control unit.



t_{V1}, t_{V2} = delay time of ON and OFF switching

When t_{V1}, t_{V2} is not kept, the power supply needs repair.

6.1.3. Troubleshooting table

Fault	Possible fault reason	Fault elimination
a) Transverter does not start to oscillate	- False voltage protection responds	- viz. b)
	- V5101, V5102 faulty	- Replace V5101, V5102
	- Contact trouble at K5001/5002	- Replace K5001, K5002
	- Contact troubles at circuit closer on front plate	- viz. c)
	- Overload at secondary end	- causes increased power consumption with mains operation
b) False voltage protection responds	- Battery voltage does not comply with the voltage adjusted on the terminal board X 5002.	
	- Component in the protective circuit faulty	- e.g. V 5107, V 5106, V 5103, K 5101
c) Starting aid for oscillation not excitated (C 5101 not charged or not discharged with connection or disconnection)	- Interruption in the oscillation-start circuit X 5001/b3(+)- k 02/7/5/11/13- R 5111-V 5110- circuit closer (on front plate)	

Fault	Possible fault reason	Fault elimination
d) F 5101 responds	- Overvoltage in the +5 V- or +18 V path	- Disconnect load in the unit (e.g. TTL circuits) - dissolder connections 6 and 7 on pc board 51 - check if an exceeding voltage presents at the output of one of the two paths. In this case e.g. transistor V 5101 or V 5102 or the control (MAA 723) is faulty.
	- Short in the circuit	- Separate load and check if the fuses keep responding. In this case e.g. V 5212, V 5214 or transistor insulation faulty.
	- Overvoltage protection circuit faulty	- e.g. V 5107, V 5108 or V 5109 (thyristor)
e) Noise caused by switching controller	- Sawtooth generator (V 5210, V 5207) faulty	- Check curve shapes at P 01, P 02. Trace signal up to circuit connection 3

Fault	Possible fault reason	Fault elimination
5) Output voltage of the -12 V-path too high	- V 5001 faulty - N 5101 faulty	
6) Frequency of rectifier hum voltage amounts, with mains oper., to 50 Hz instead of 100 Hz	- One rectifier branch of the respective rectifier faulty	- Measurement at C 5105: -12-V path C 5108: Additional voltage for 22-V path C 5003: +5-V path +18-V path

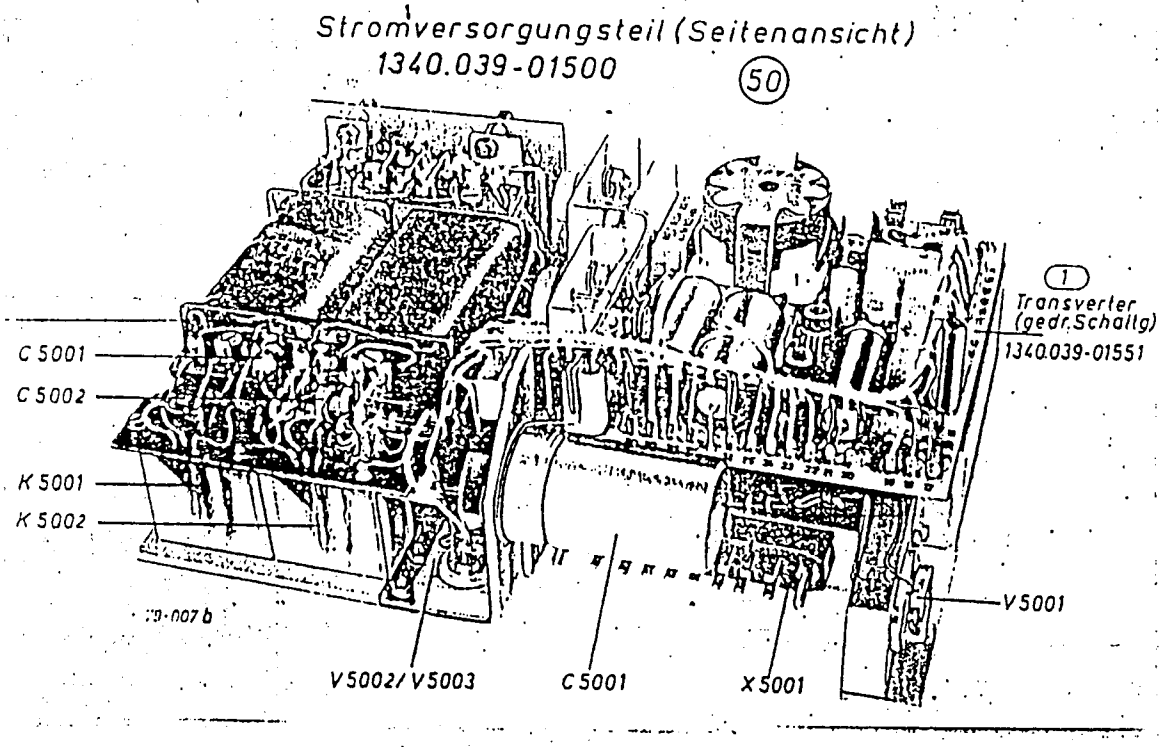


Figure 6

Power supply section 1340.039-01500

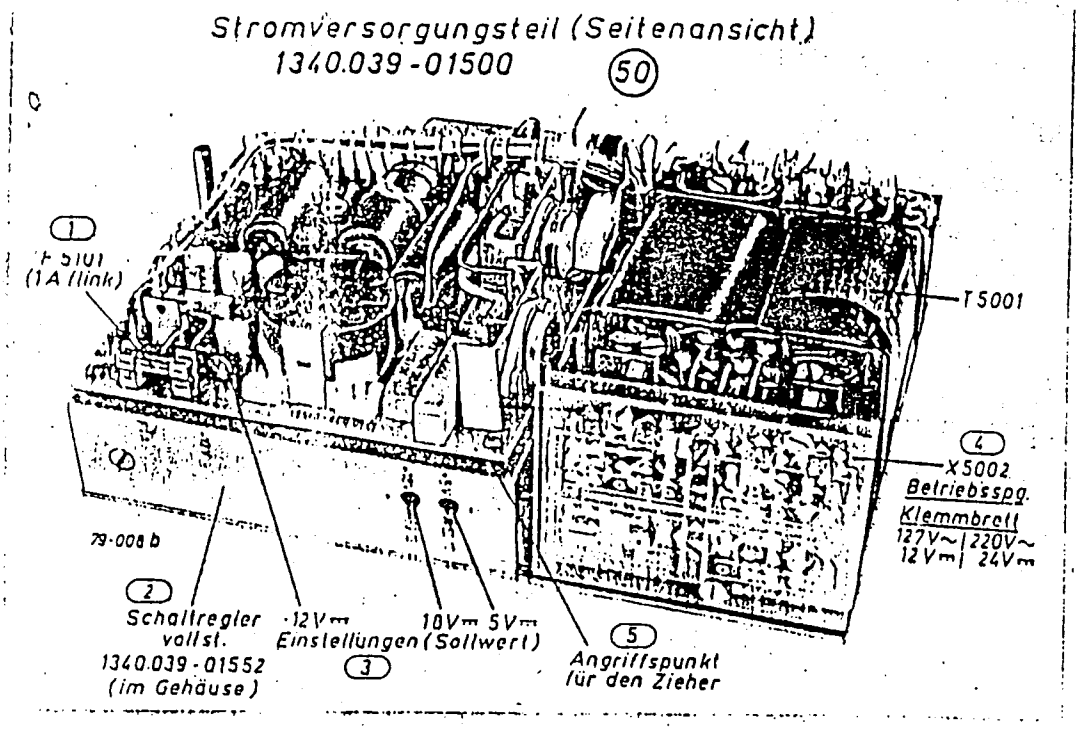


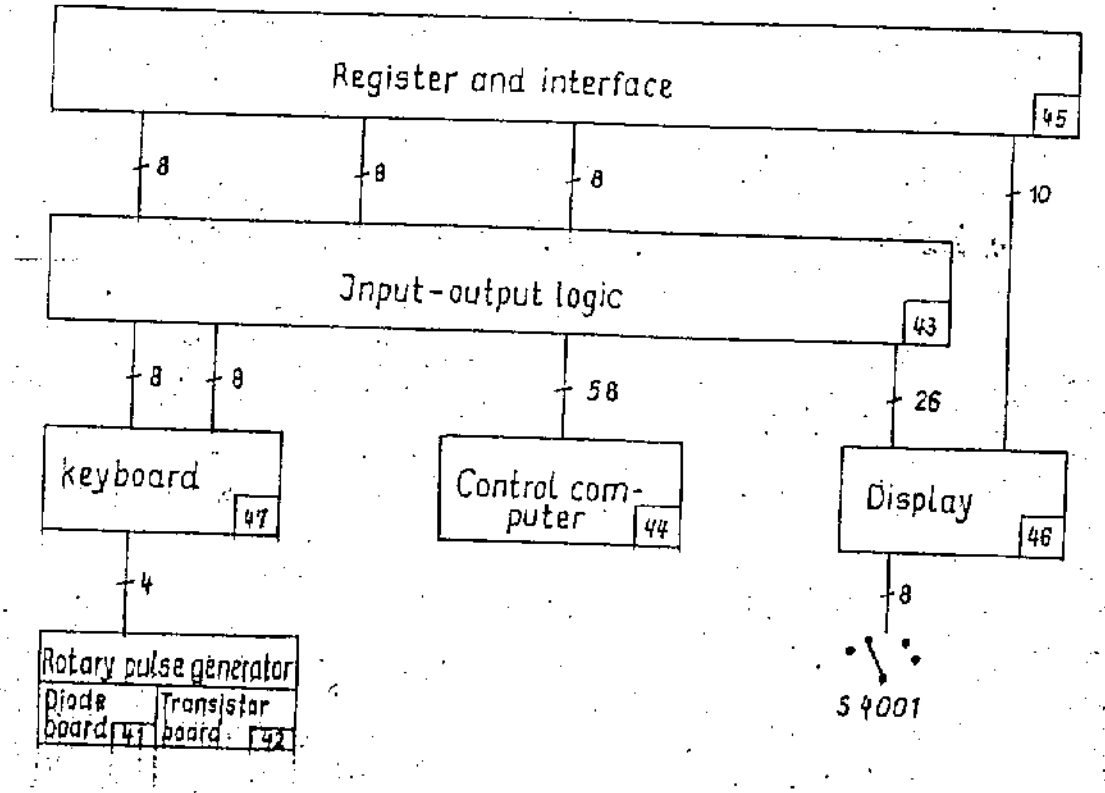
Figure 7

Power supply section 1340.039-01500

6.2. Control unit

6.2.1. Function principle

After switching on the unit as well as after mains fa the microcomputer is brought in the initial position and the receiver is adjusted to its codition before the disconnection or mains failure.
Subsequently, a program for multiplexer control of the displa is initiated.
All operating measurements carried out via keyboard or 24-V i face cause via port A an interruption of the PIO circuit.
Mains failure and test routines are controlled via the non-mas interrupt input of CPU. The RAM circuits of the control comput are backed by an internal battery.
In case of a total breakdown, it is recommended to start troub shooting in the computer core because fault detecting is suppo by the software. The following sequence is to be adhered to: Control computer - input-output logic - keyboard - display - register and interface.



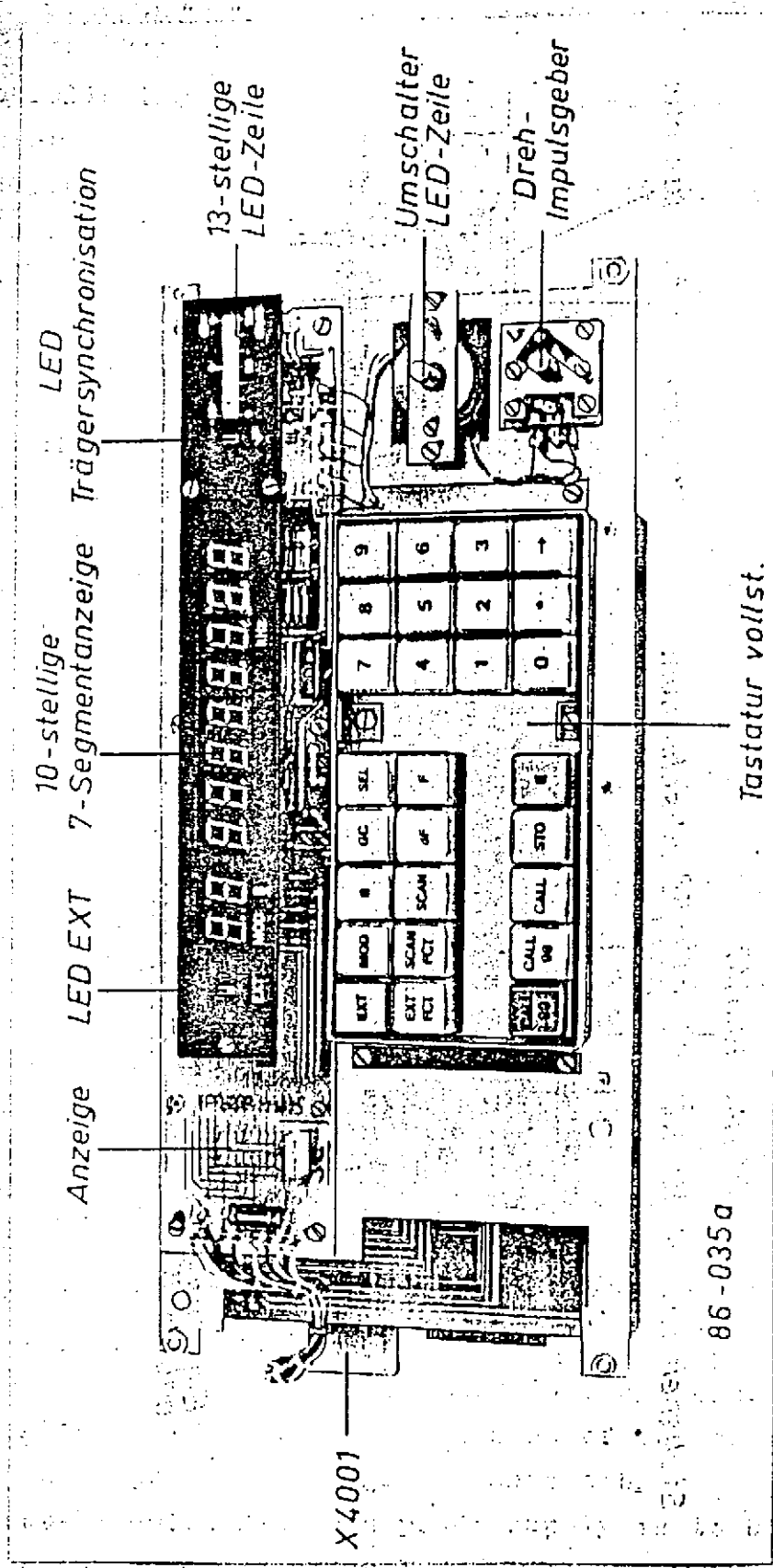


Figure 8

Control unit - Front view

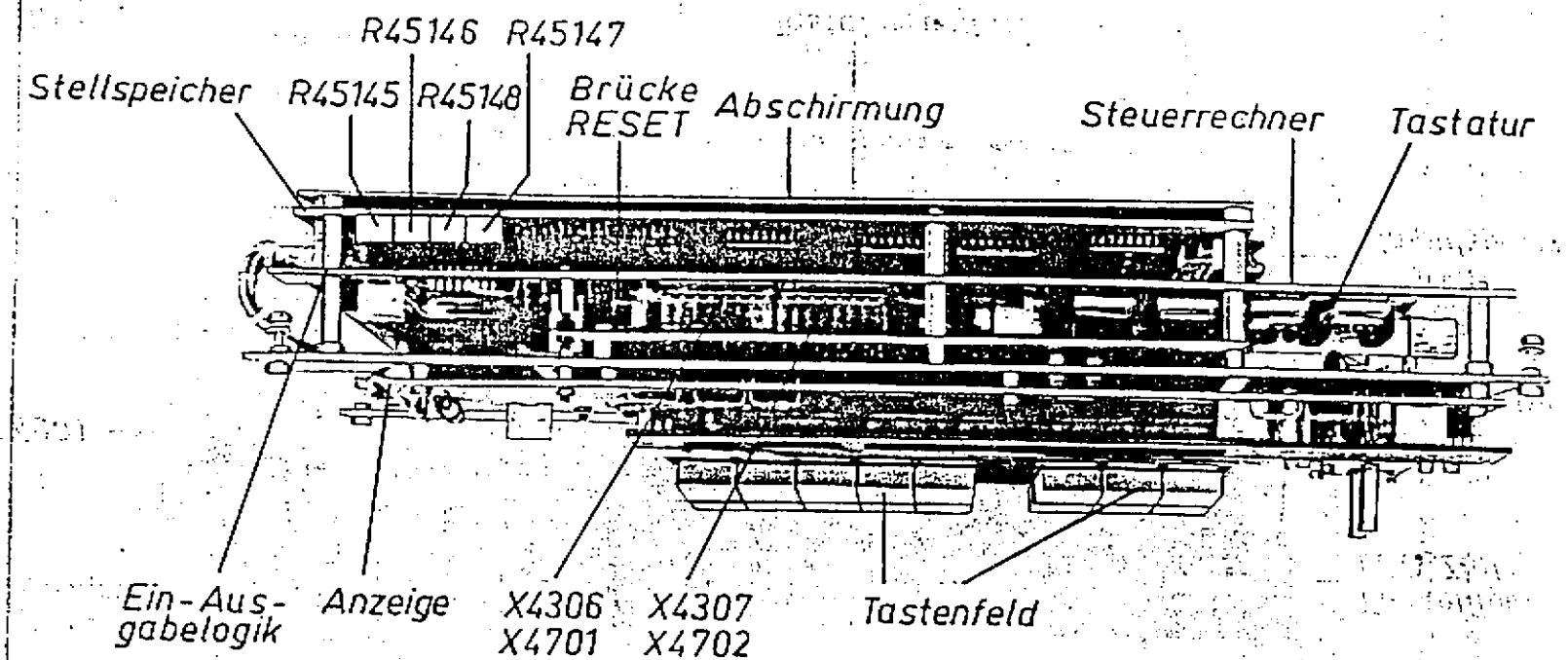


Figure 9
Control unit - view from above

6.2.2. Test and check arrangements

- Control unit inserted

The following components of the plug-in are accessible from above:

. R45145 ... R45147 to balance the control voltage linearization (cf. Section 6.2.9.)

. X4701, X4702 to check and repair the keyboard (cf. Section 6.2.7.)

. Strip 01-02 (RESET) on input-output logic.

Open the receiver front plate, remove screening. The control unit is accessible from the soldering side of the register and interface.

On the soldering side of the control computer U_{RAM} can be checked at C4408.

- Control unit removed

By means of connection adapter P15 the control unit can be operated from an external mains unit; +5 V, +18 V, -12 V, ⊥

- Check of display and keyboard

Open the front plate of the plug-in, slacken the plug-and-socket connetions X4501-X1023 and X4505-X1022, take off the control unit and place it upright such that the plug-and-socket connections can be reestablished again. The complementation side of the display is accessible. If necessary, unscrew the cover.

- Check of control computer and input-output logic

Take off the control computer; establish connection plug-in X1023 - input-output logic X4303/04/05by means of adapter cable P14. The complementation side of the control computer and the input-output logic is accessible.

Connect P14 with P15 when power supply is to be performed from an external mains unit.

6.2.3. Repair sequence 'local operation'

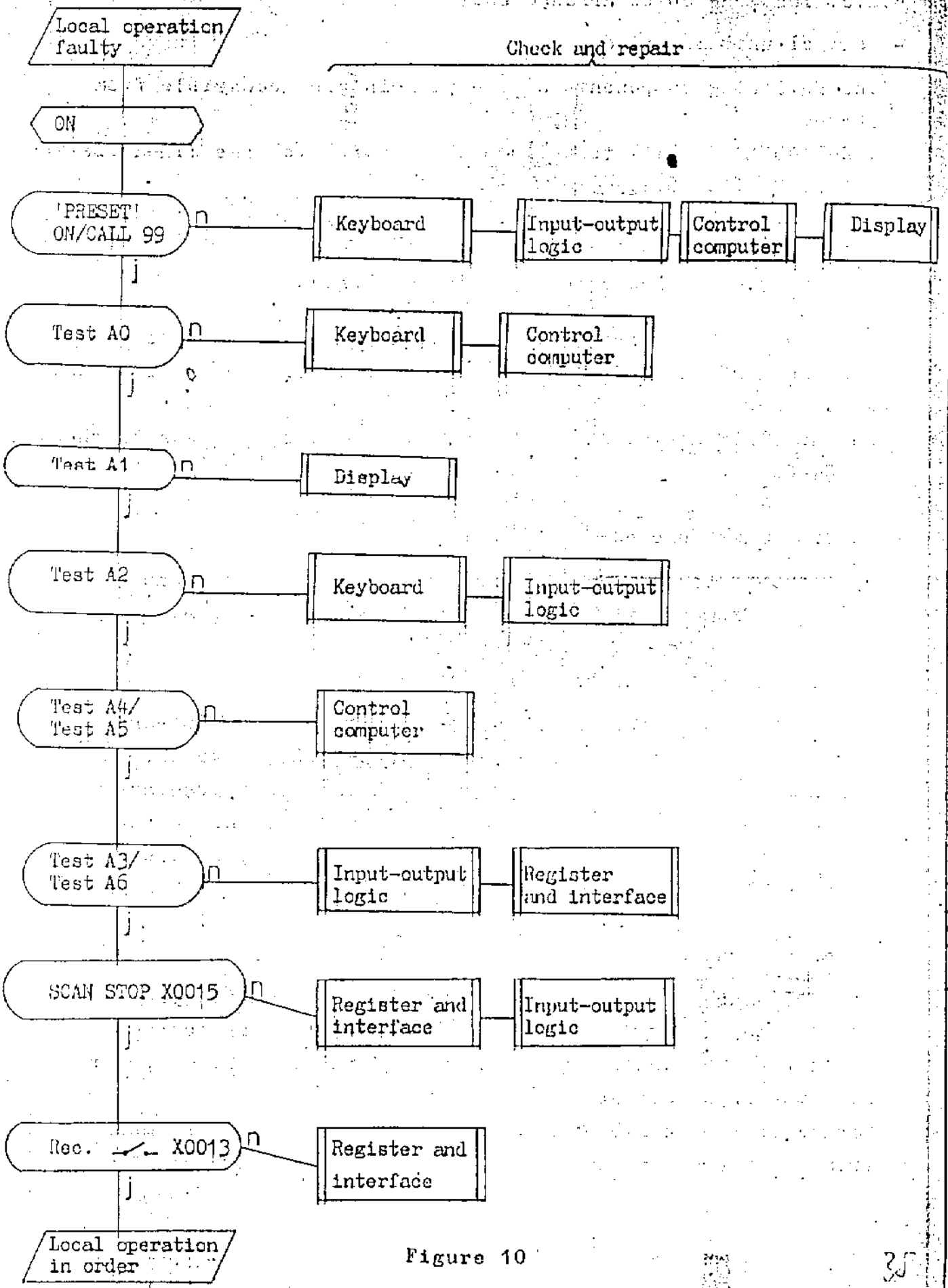


Figure 10

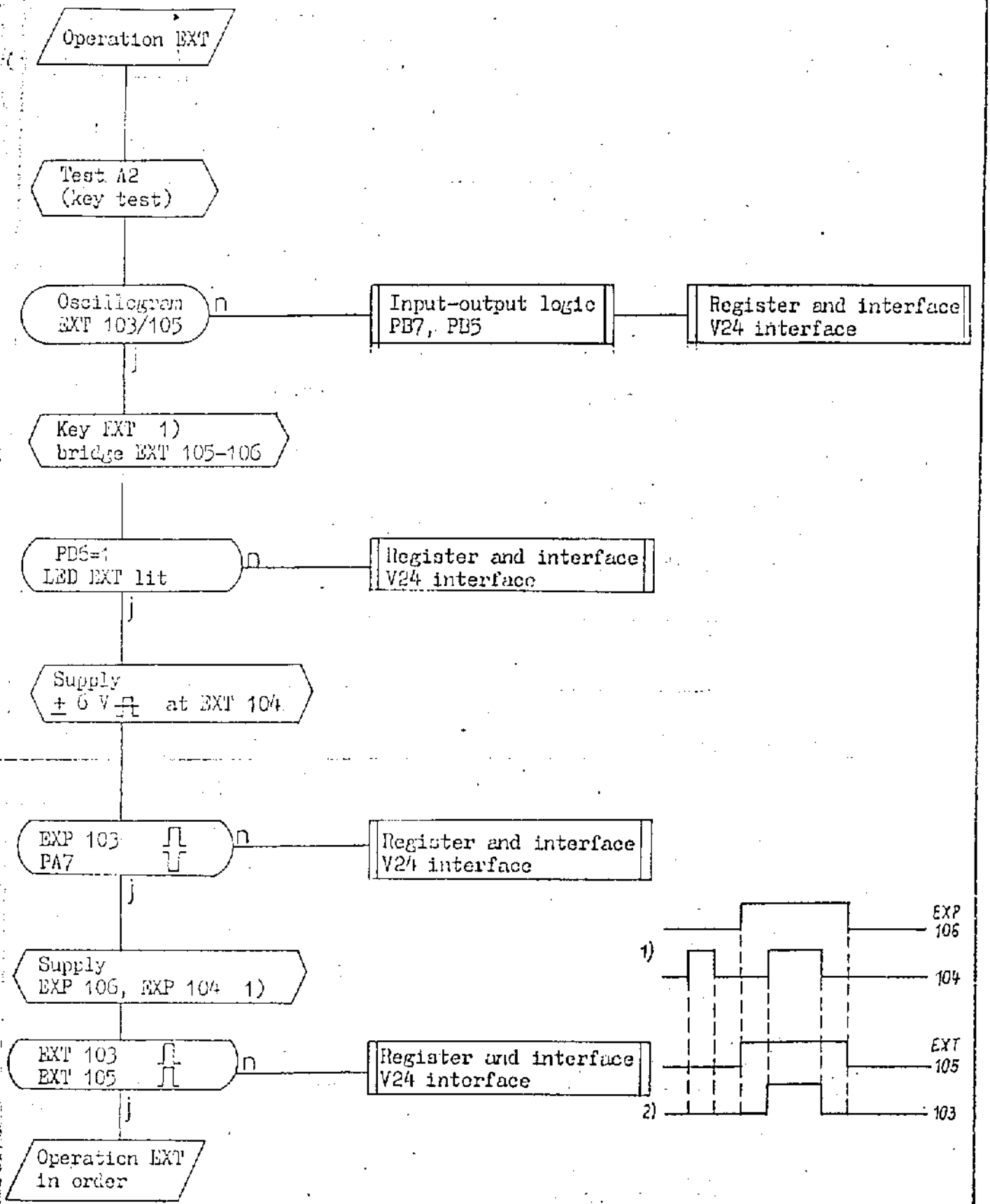


Figure 11

1) The unit is to be programmed in advance as 'slave'.

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6.2.5. Control computer

- Operating voltages

  +5 V at D04/11, U_{RAM} at C08 (cf. Section 6.2.6. U_{RAM} changeover)

- Input signals of CPU

  $\overline{BUSRQ}$, $\overline{WAIT}$, $\overline{RESET}$, $\overline{NMI}$, $\overline{INT}$ = 1 (≙3.5 V)

  Clock at D04/6 ⊓⊓ 1.2 MHz U_{high} ≙ 4.8 V, U_{low} ≙ 0.5 V

- CPU bus and store selection signals

  Open wire strap 03-04, establish connection 04-13.
  Cyclic program call is performed. The data bus, the address bus and the control bus of the CPU can be oscillographically checked concerning correct low-high signal change. With this, also the connections of the bus lines to the circuits as well as shorts can be checked.

Signal	U_{low}	U_{high}
D0 ... D7	<0.7 V	3.5 V
A0 ... A3		>3.5 V
A4 ... A15		>2.5 V
M1, RD, WR, MREQ, RFSH		>2.5 V
CS0 test point 03		>2.5 V
CS1 R07		>3.5 V
CS2 test point 05		>2.5 V
CS3 test point 07		>2.5 V
CS4 test point 09		>2.5 V
CS5 test point 11		>2.5 V

- Software-aided checks

(cf. equipment documentation Section III/5.2.)

a . Test (key [EXT] and [EXT FCT])

This test, an NMI access to the CPU, checks the function of the input gate PIO port A, i.e. it is tested if the data are red. Furthermore, the function of the EPROMs are checked, i.e. if data are put out.

Troublefree function:
All keys are open (PA 6...PA 0 = 78 H), serial input in STOP condition (PA 7 = 1). All EPROMs supply data.

Display: AA-A0 last receive condition. In condition AA a program loop is running cyclically. It is possible to check oscillographically the CPU signals $\overline{IORQ}$, $\overline{MERQ}$, $\overline{M1}$, $\overline{RD}$, $\overline{WR}$, and the decoder signals CS 0 ... CS 5.

Malfunctioning:
The key code of a faulty key is indicated or PA 7 is not in STOP condition or port A of the PIO does not work.
Display 01 indicates: EPROMs by switching further with key [→] (01, 02 ...); the faulty EPROM does not appear on the display but any display as e.g. FF. Consider the departure from the correct sequence.

b . Test A4 RAM test

Results: FF, F1, F2
FF = troublefree, F1 = RAM 1 (D 4405) faulty,
F2 = RAM 2 (D 4406) faulty.

c . Test A5 ROM test

Results: FF, F1, F2, F3, F4
FF = troublefree, F1 ... F4 = faulty EPROM D 4408 ... D 4411.

Attention

Individual EPROMs must not be exchanged.
When a component - circuits D 4408, D 4409, D 4410, D 4411, (D 4412) - has proved itself to be faulty, the entire pc board control computer 1340.041-01454 is to be replaced.

6.2.6. Input-output logic

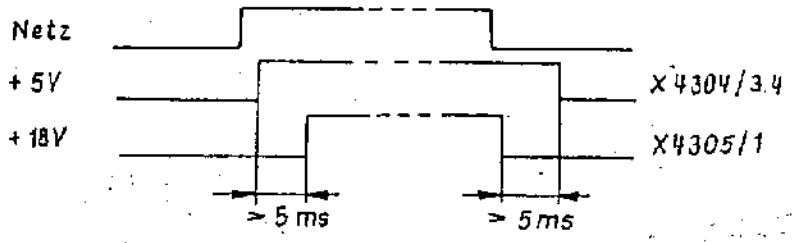
Test sequence:

- RESET-and NMI generation
- U_{RAM} changeover
- Input-output gate addresses and assigned output signals

- RESET- and NMI generation

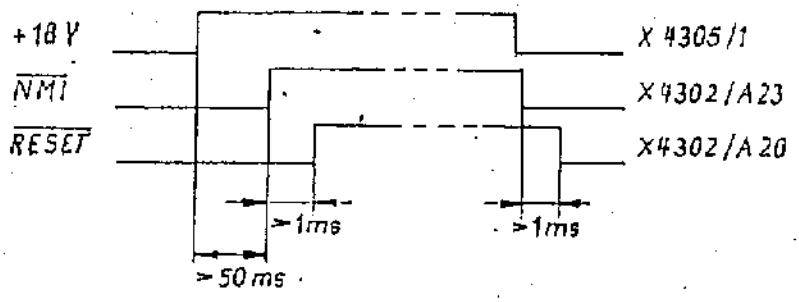
. unit switch ON/OFF, check voltage curve with double-beam oscillograph P5

+5 V and +18 V



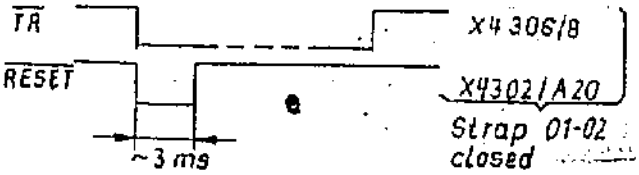
When these conditions are not met — repair power supply in accordance with Section 6.1.

$\overline{NMI}$ and $\overline{RESET}$



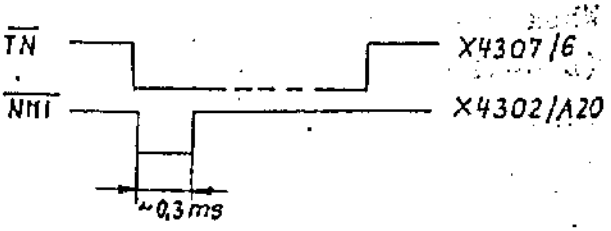
. RESET pulse

Key CALL 99



NMI pulse

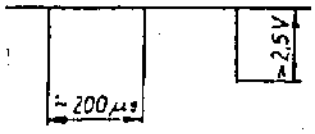
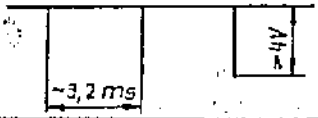
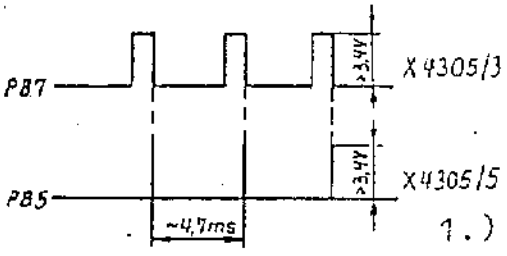
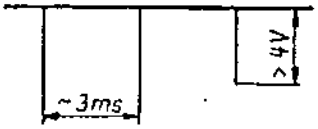
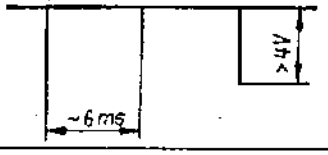
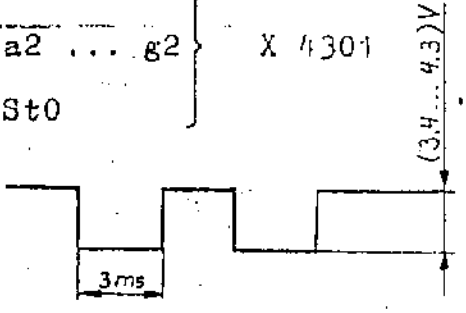
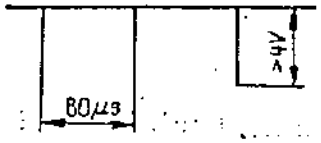
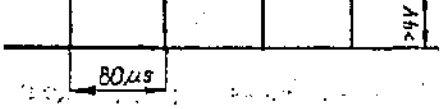
Keys EXT EXT FCT 0



- U_{RAM} changeover

Unit switch	U_{RAM} to C 4408
ON	+5 V from power supply
OFF	+ (3.6 ... 4.1)V from support battery

- Input-output gate addresses and assigned output signals

Input	Output	Pulses to be checked	Output signals
Test	AA	$\overline{30H}$ at D 4302/12 	
Test A1	8 ... 8	$\overline{10H}$ at D 4302/14 $\overline{20H}$ at D 4302/13 	a1 ... g1 a2 ... g2 p1, p2 St0 ... St4 } X 4301 2.)
TEst A2 Key EXT	00	$\overline{30H}$ at D 4303/12 Oscillogram without synchronization U 2.5 V	 1.)
Test-A3	A3 00	$\overline{10H}$ at D 4302/14 $\overline{20H}$ at D 4302/13  $\overline{50H}$ at D 4302/10 	a1 ... g1 a2 ... g2 } X 4301 St0 
Test A6	A6	$\overline{40H}$ at D 4302/11 	D0 ... D7 to X 4303/1...8 A0 ... A2 at X 4304/6,7,8 

1) cf. Section 6.2.9. V24 interface/example 2
2) cf. Sections 6.2.8. and 6.2.9.

6.2.7. Keyboard

Figure 12.

Output signals

Taste	Hexa-code	X4701/ 1 PA6	2 PA5	3 PA4	4 PA3	5 PA2	6 PA1	7 PA0	8 IR	X4702/ 6 III	
EXT	00	⊓	⊓	⊓	⊓	0	0	0	1	1	1 ms
2ND	6d	1	1	⊓	1	1	0	1	1	1	
B	62	1	1	⊓	⊓	0	1	0	1	1	
MC	67	1	1	⊓	⊓	1	1	1	1	1	
DEL	76	1	1	1	⊓	1	1	0	1	1	
EXT FCT	20	0	1	0	0	0	0	0	1	1	
SCAN FCT	61	1	1	⊓	⊓	0	0	1	1	1	
SCAN	6C	1	1	⊓	1	1	0	0	1	1	
[illegible]	64	1	1	⊓	⊓	1	0	0	1	1	
[illegible]	66	1	1	⊓	⊓	1	1	0	1	1	
CALL 99	21	⊓	1	⊓	⊓	0	0	1	0	1	
CALL 90	22	⊓	1	⊓	⊓	0	1	0	1	1	
CALL	63	1	1	⊓	⊓	0	1	1	1	1	
[illegible]10	73	1	1	1	⊓	0	1	1	1	1	3 ms
	65	1	1	⊓	⊓	1	0	1	1	1	
[illegible]	30	⊓	1	1	⊓	0	0	0	1	1	
1	31	⊓	1	1	⊓	0	0	1	1	1	
2	32	⊓	1	1	⊓	0	1	0	1	1	
3	33	⊓	1	1	⊓	0	1	1	1	1	
4	34	⊓	1	1	⊓	1	0	0	1	1	
5	35	⊓	1	1	⊓	1	0	1	1	1	
6	36	⊓	1	1	⊓	1	1	0	1	1	
7	37	⊓	1	1	⊓	1	1	1	1	1	
8	38	⊓	1	1	1	0	0	0	1	1	
9	39	⊓	1	1	1	0	0	1	1	1	
.	2E	⊓	1	⊓	1	1	1	0	1	1	
—	36	⊓	1	1	1	0	1	1	1	1	
EXT+EXT FCT	00	0	0	0	0	0	0	0	0	0	
⌒	20	⊓	1	⊓	1	0	⊓	⊓	1	1	0,5 ms
⌒	24	⊓	1	⊓	1	⊓	0	⊓	1	1	
keine Taste	70	1	1	1	1	0	0	0	1	1	

Für jede Taste kann der Code ebenfalls erzeugt werden, wenn gleichzeitig die Taste EXT FCT gedrückt wird.

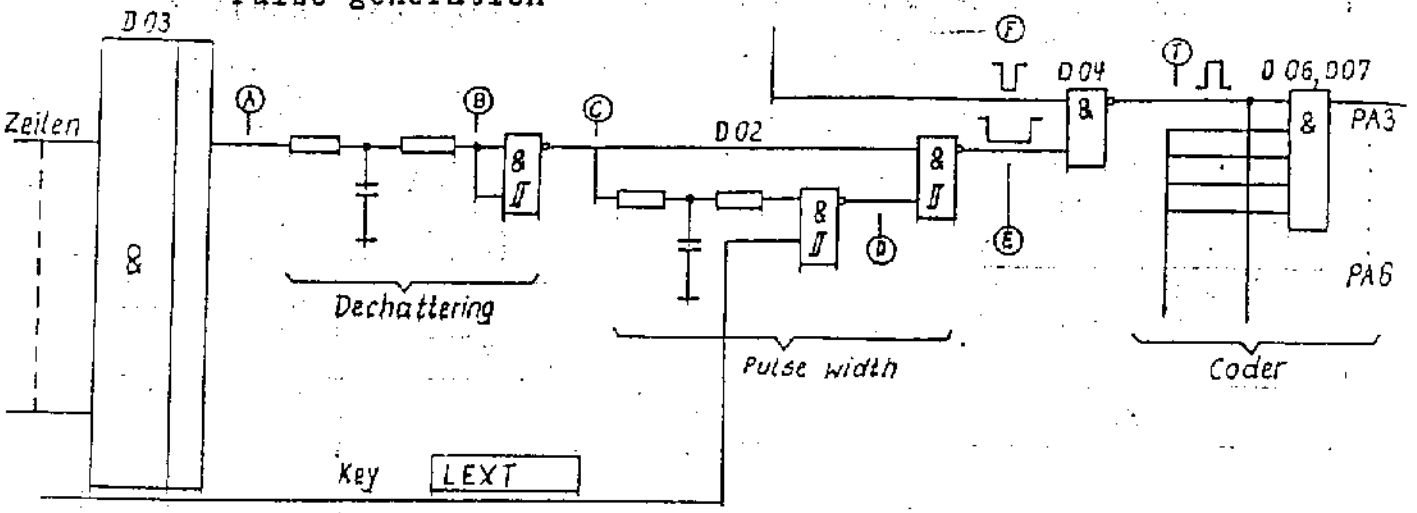
Code can be generated for each key if EXT FCT is pressed simultaneously

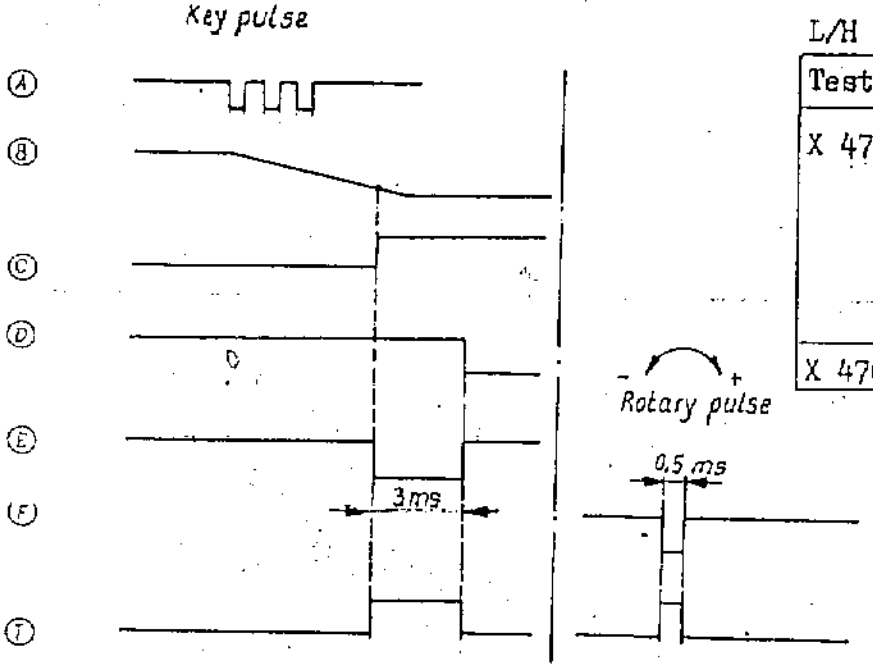
- Low/high levels

Static L/H levels are to be provided at the outputs by depressing the respective key. Checks should be performed according to the scheme below.

Outputs		Low		High	
		Key	Level	Key	Level
X 4701/8	$\overline{TR}$	"CALL 99"			
7	PA 0				
6	1				
5	2	"EXT" and			
4	3	"EXT FCT"	<0.5 V	"7"	>4.0 V
3	4				
2	5				
1	6				
X 4702/6	$\overline{TN}$				

- Pulse generation

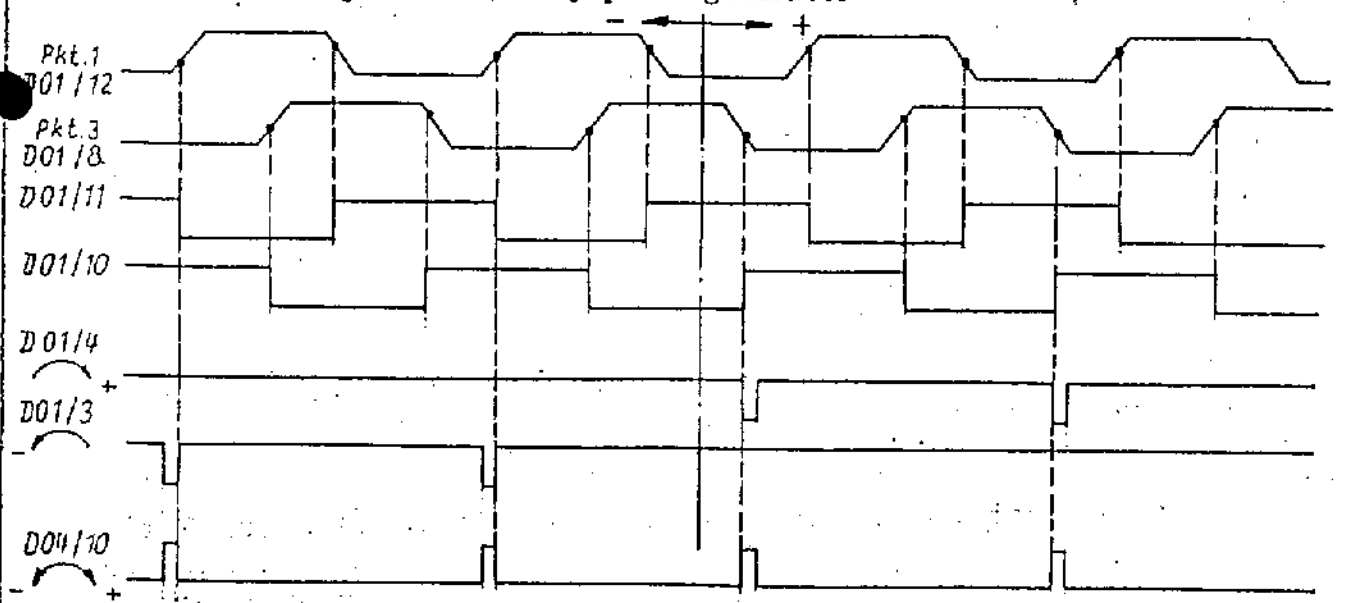




L/H level

Test point		L (V)	H (V)
X 4701/1	PA 6	< 0.5	> 4.5
.	.	.	.
.	.	.	.
7	PA 0	< 0.5	> 4.5
8	$\overline{TR}$	< 0.5	> 3
X 4701/6	TN	< 2.6	> 3

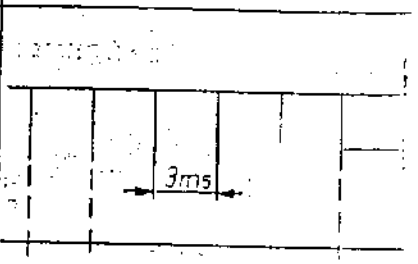
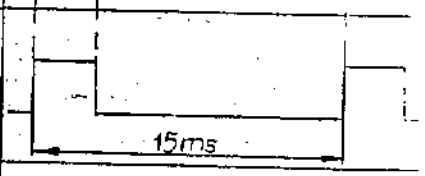
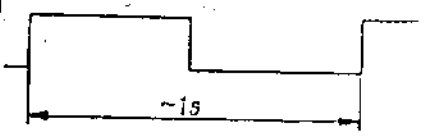
- Pulse diagram for rotary pulse generator



6.2.8.

- Digital display

  Voltage curve in test A1

Segment	Test point at X 4601	$\hat{U}$	
a1 ... g1	A4, B3, B13, B12 A13, A3, B4	~3.4 V	
a2 ... g2	A1, A2, A11, A12 B11, B2, B1		
p1, p2 St0...St4	A5, B10 A8, B9, B7, A10 B8	~4.3 V	
LED EXT	A9	~4.3 V ~4.7 V	

- LED row

  Voltage values

Position S 4001	U at input	Point	U at point 15	Lighting LED
△ F x 1	0 V	04	2.7 $V_{=}$	V 17
△ F x 2				V 17
E_{γ}	4.8 $V_{=}$	19		V 17
U_{AF}	1.4 V~ (1 kHz)	03	4.7 $V_{=}$ 1)	V 22

1) correction with R 4631

Check entire row with test A3 according to the Equipment documentation Section III/5, S 4001 to E_{γ} .

- Register and interface matrix

The receiver setting is stored in the 12 register circuits D 4504 to D 4515 that form the register and interface being arranged as matrix (7 rows/8 columns). The rows are the addresses, the columns the data.

Assignment of the circuit function

A \ D	7 6 5 4	3 2 1 0
1	D 4505 100 Hz	D 4504 10 Hz
2	D 4707 10 kHz	D 4506 1 kHz
3	D 4509 1 MHz	D 4508 100 kHz
4		D 4510 10 MHz
5	D 4512 MOD	D 4511 B
6	D 4514 SEL	D 4513 SEL
7		D 4515 GC

Example — Short-time reaction at $\Delta F \equiv 1$ kHz

Setting 73 E 12345.67 SEL 1 GC 4

A \ D	7	6	5	4	3	2	1	0
1	0	1	1	0	0	1	1	1
2	0	1	0	0	0	1	0	1
3	0	1	0	0	0	1	0	1
4	0	0	1	0	0	0	1	1
5	0	1	1	1	1	1	0	0
6	0	1	1	0			0	1
7						1	0	0

Note:

Data for B stored in inverted form. The letterings on the lines at the outputs of the register circuits correspond with this matrix.

48

Example: 3/5 means address 3/data bit 5, i.e. bit 2^1 of the 1-Hz digit of the frequency.

- The frequency data correspond with the decimal places in the 8-4-2-1 code. Output is performed via drivers D 4516 to D 4520. The output lines are marked in accordance with the decimal points. The levels are CMOS levels.
  Example: Setting to 1.23 kHz

Frequency		x 1 kHz			x 100 Hz				x 10 Hz			
Line	d3	c3	b3	a3	d2	c2	b2	a2	d1	c1	b1	a1
Logic condition	0	0	0	1	0	0	1	0	0	0	1	1
X 4501	B20	B19	B18	B17	B24	B23	B22	B21	B28	B27	B26	B25

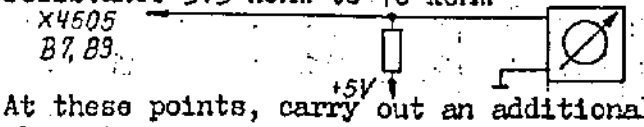
- The selector data are derived automatically from the frequency i.e. the interconnection is contained in the ROM test. The output lines go directly out from the store circuits; the voltages are CMOS levels. For MOD, B and GC the store data are decoded and logically connected. The output signals are generated via driver stages.
- Check of the register and interface outputs
  Precondition: Input and display in order. Input signals A0...A2 at X 4503 and D0...D6 at X 4504 available, if not, check $\overline{40}$ H at input-output logic (cf. Section 6.2.6.). Correct display does not indicate proper output of the register and interface.
  Checking the outputs is performed with test A6

  Setting [A6] (test 6)

  With key [→] switch digits 00 to 99 further one after the other; Check with this the logic conditions at the soldering side according to the table for register and interface test. (cf. Fig. 13)
  Observe the following:

  X 4501/a 16 — This point lies next to +18 V. Be cautious with test prod.

  X 4505/B7 /B9 — Check of the logic conditions with pull-up resistance 3.3 kohm to 10 kohm



  X 4501/A 16, X 4505/B5 /B9 — At these points, carry out an additional check of the short-time reaction at $\Delta F \triangleq 1$ kHz.

Table

Display in testing procedure

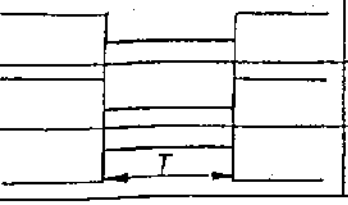
	Measur. point	Register and interface test										Level 0/1
		00	11	22	33	44	55	66	77	88	99	
F	X4501/B3	0	0	1	1	0	0	1	1	0	0	≤0,8V/≥2,4V
	B4	0	1	0	1	0	1	0	1	0	1	
		Code 8421 corresponds to dcba										
	x 10 Hz B25	0	1	0	1	0	1	0	1	0	1	
	x 10 Hz B26	0	0	1	1	0	0	1	1	0	0	
	x 10 Hz B27	0	0	0	0	1	1	1	1	0	0	
	x 10 Hz B28	0	0	0	0	0	0	0	0	1	1	
SEL	X4501/A26	0	1	0	1	0	1	0	1	0	1	≤0,5V/≥4,5V
	A27	0	0	1	1	0	0	1	1	0	0	
	A28	0	1	0	1	0	1	0	1	0	1	
	A29	0	0	1	1	0	0	1	1	0	0	
	B29	0	0	0	0	1	1	1	1	0	0	
MOD	X4501/A25	0	1	0	0	0	0	0	0	0	0	≤0,2V/≥17,5V
	A24	0	0	1	0	0	0	0	0	0	0	
	A23	0	0	0	1	0	1	0	0	0	0	
	A22	0	0	0	1	0	1	0	0	0	0	
	A21	0	0	0	0	1	0	1	0	0	0	
	A20	0	0	0	0	0	1	1	0	0	0	
	A19	0	0	0	0	0	0	0	1	1	0	
	A18	0	0	0	0	0	0	0	0	0	1	
	A17	0	0	0	0	0	0	0	1	1	1	
	A16	0	0	0	0	0	0	0	0	1	1	≤0,2V/≥12V
B	X4505/B1	0	1	0	1	0	1	0	1	0	1	≤1V/≥6V
	B2	0	0	1	1	0	0	1	1	0	0	
	B3	0	0	0	0	1	1	1	1	0	0	
	B4	0	0	0	0	0	0	0	0	0	1	
	B5	0	0	0	0	0	0	0	0	0	1	
GC	X4505/B7	0	1	0	1	0	1	1	1	1	1	≤0,2V/≥3V
	B8	1	0	0	1	1	1	1	1	1	0	
	B9	1	1	1	1	1	0	1	1	1	0	

Figure 13

- Short-time reactions

In case of frequency changes of ≙ 1 kHz the control computer supplies the output GC = 8 that initiates through the monostable flipflop (D 4523) a dynamic behaviour of lines FS 1/0, ☟ and U_{block}. A short lighting up of V 4623 (right LED) presents in the LED row.

Setting [73 E 0.00] dF = 1 kHz

Test point	Line	Pulse	Condition
X 4501/A 16	FS 1/0		MOD 8 or 9
X 4505/B9	☟		GC ≠ 5
X 4505/B5	U_{block}		

T = 125 ... 155 ms

- Receive blocking (cf. Equipment documentation, Section II/2.7.)

The blocking signal of + (3...15) V at X 0013/X 0014 and bandwidth B = 9 have the same effects:

Test point	Line	Logic condition	Level
X 4505/B4	5/3	1	≙ 1 V/ ≙ 6 V
X 4505/B5	U_{block}	1	≙ 1 V/ ≙ 6 V
X 4501/A16	FS 1/0	0	≙ 0.2 V/ ≙ 12 V

- SCAN STOP

The control signal at X 0015/X 0016 acts via N 4501/8 and D 4501/4 on PB Ø.

Funtion	$U_{=}$ at X 0015/X 0016	PB Ø at X 4502/6	Level 0/1
SCAN	-15 V ... +0.8 V 1)	1	≙ 4.5 V
SCAN STOP	+3 V .. +15 V	0	≙ 0.5 V

1) Control signal -15 V ... +8 V is equivalent to 'sockets open'.

Precondition: Function of the signal path in order.

. Setting 1 | 16 E 0.00 | GC 1

Set f_{AF} to 1 kHz with A1 ≈

Set U_{AF} to 0 dB_m (0.77 V) at X 1020/A - B with ≈

Frequency F = 1.50 kHz

Check if U_{AF} ≅ -12 dBm

. Setting 2 | 48 E 1.00 | GC 1

U_{AF} to 0 dBm as above

Frequency F = 2.50 kHz

Check if U_{AF} ≅ -3 dBm

If U_{AF} is not adjustable or in case of distortions, check level with setting 1:

Incoming AF voltage at X 4505/A 13 ~ 0 dBm (0.77 V)

outgoing AF voltage at X 4505/B 13 ~ -12 dBm (0.2 V)

- Checking and balancing the control voltage linearization

Precondition: Function of the signal path in order.

Do not unscrew front panel of the plug-in; balancing elements are accessible from above (cf. Figure 9). Balancing requires feeding of a defined aerial signal with calibration level. Use aerial socket X 0001 at the casing rear; % = 75 ohm. The voltages to be supplied are emf ratings.

. Setting | 47 E 4500.00 | GC 1, SEL 0

. Frequency setting on test oscillator 4501.00 kHz

Make use of A3, perform balancing according to the table below:

Aerial emf	Number	Balancing element	Remarks
30 dB (/uV) ≙ 32 /uV 90 dB (/uV) ≙ 32 mV	15 45	R 45 145 R 45 146	alternating until residual error = 0
10 dB (/uV) ≙ 3.2 /uV	05	R 45 148	
120 dB (/uV) ≙ 1 V	60	R 45 147	

Check by repetition

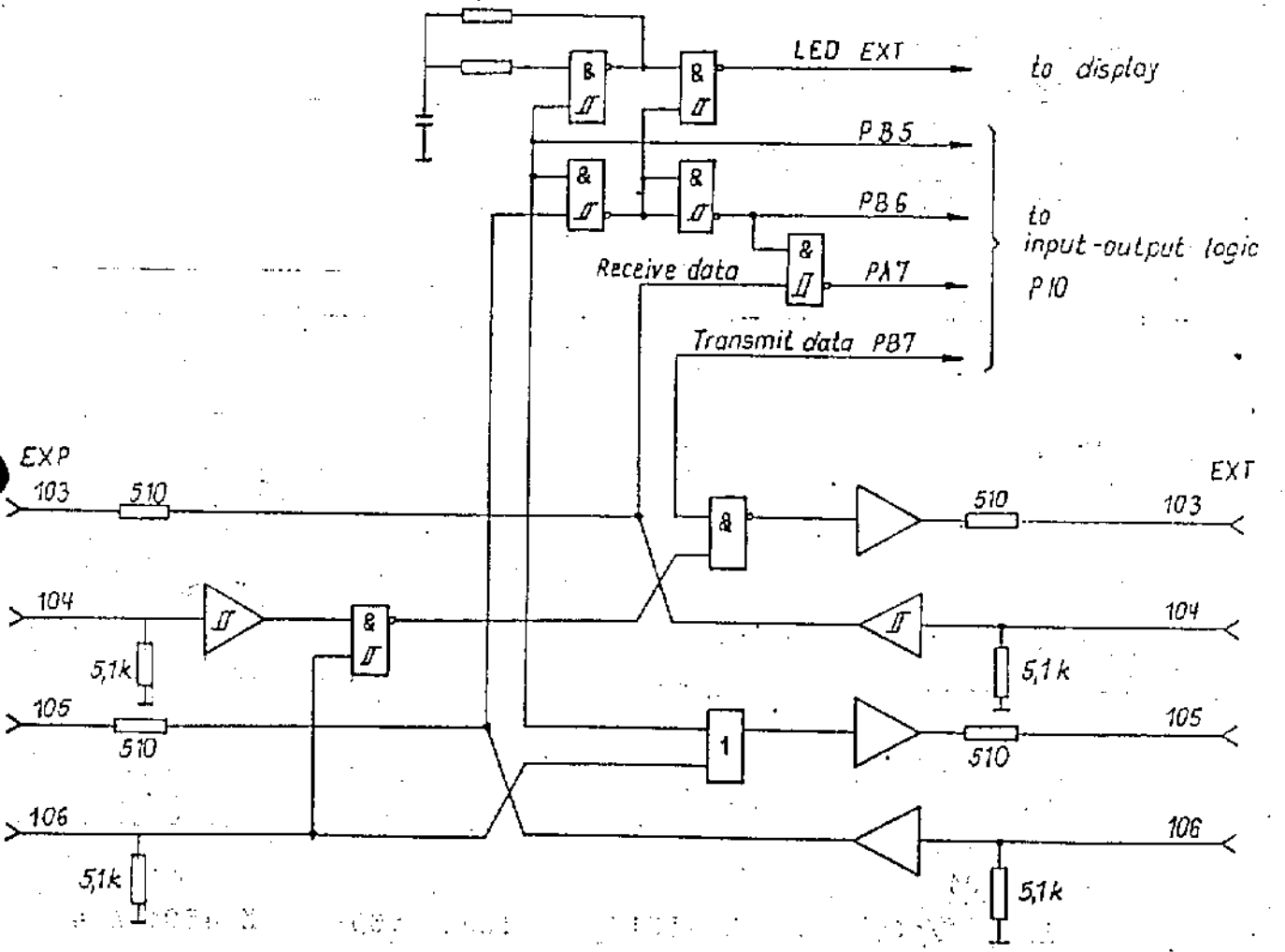
In balanced condition, the display fault amounts in digits to ± 2, i.e. to ± 4 dB (/uV).

- V-24 interface

Lines

101 Protective earth
102 System earth
103 Transmitting data to data transmission equipment (DÜE)
104 Receiving data from DÜE
105 Request to transmit to DÜE
106 Ready for transmission from DÜE

. Schematic circuit diagram



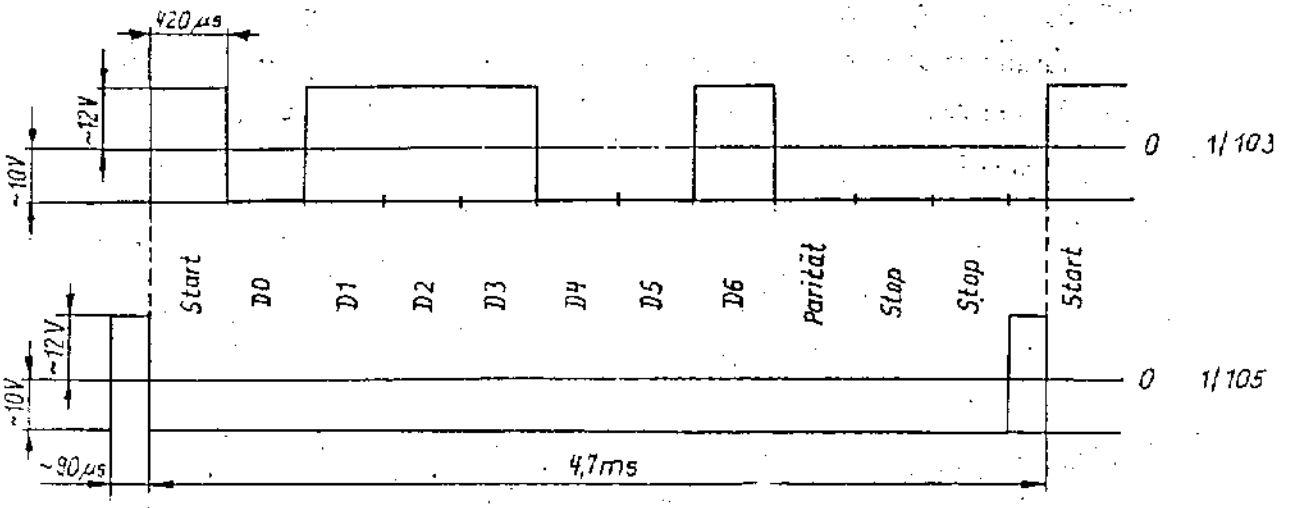
Setting test A2

Double-beam oscillograph

B channel at line 1/103, X 0005/E - A, B (⊥)
A channel at line 1/105, X 0005/C - A, B (⊥)
} A channel synchronizes B channel

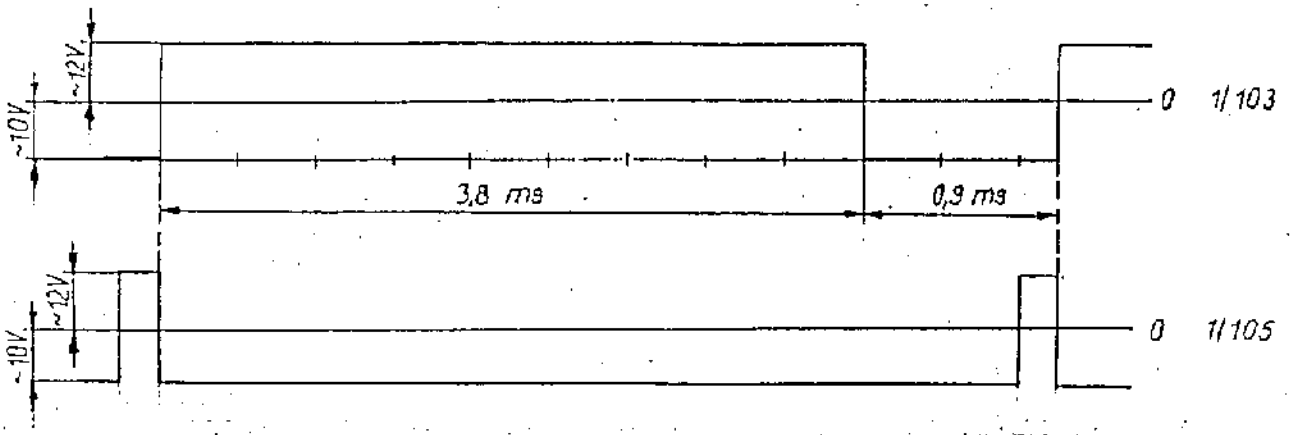
Oscillograph pulse curve

Example 1 Key [1] , 31 H



If no double-beam oscillograph available, select key [EXT] , 00 H. Oscillograph lines 1/103 and 1/105 separately.

Example 2 Key [EXT] , 00 H



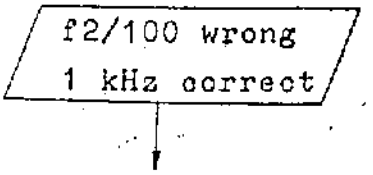
If no pulses can be detected, trace the signal back up to X 4501

Line 1/103 X 4501/A2, line 1/105 X 4501/A 4

6.3. Frequency processing

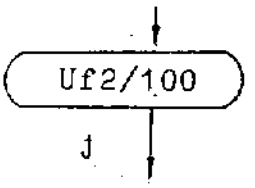
6.3.1. Troubleshooting sequence

The test programs for troubleshooting are given in the following in accordance with the principle of frequency processing. Each program starts with indication of the fault, e.g.



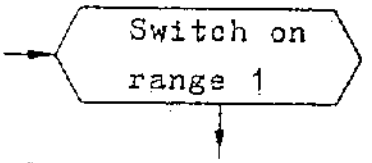
that means that frequency f2/100 is wrong, the 1-kH signal correct.

After that, different test measurements are carried out which are indicated as abridged questions, e.g.



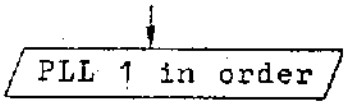
that means that the volta or the voltage curve Uf2/ are available as represen in the General diagram.

The measurements indicate which component is to be checked. The required test program or test instructions are given, e.g. → PLL2

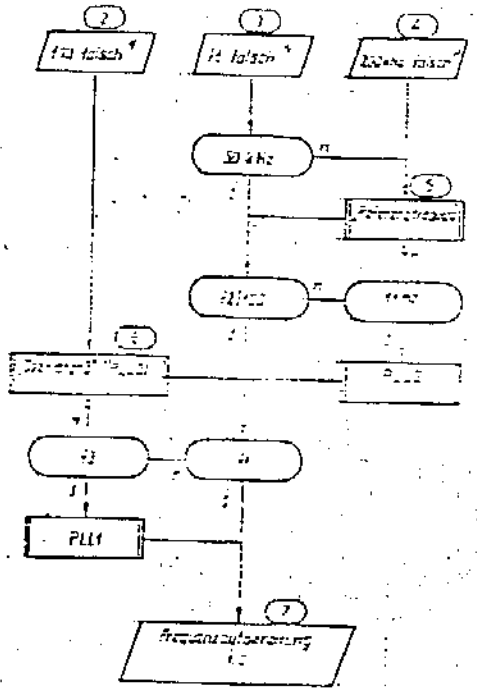


For each test program the measuring points are given in the opposite diagrams.

The test program is terminated with the information that the component to be tested is troublefree, e.g.

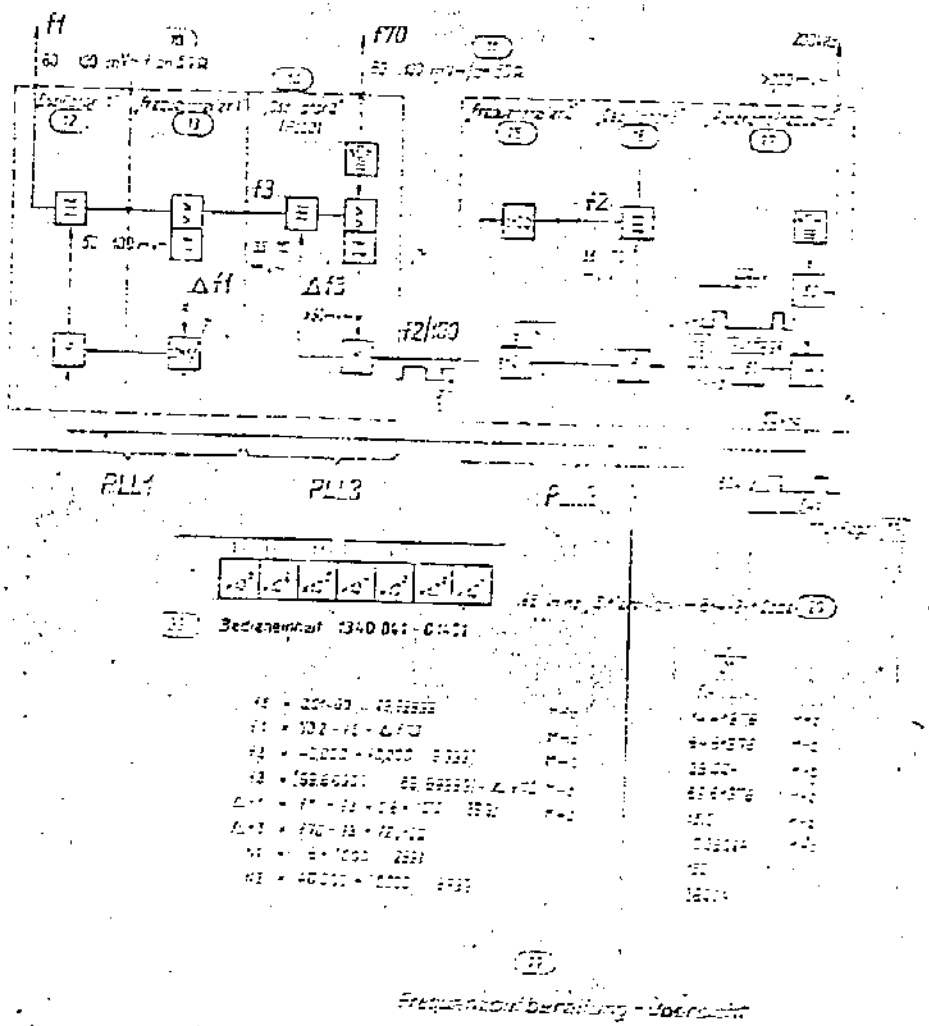


(1) Programm für die Fehlersuche



8 falsch = Frequenz falsch
* Bei falschen Pegeln werden die entsprechenden Leitungsbits gesetzt

(9) Vereinfachter Übersichtsschaltplan - Frequenzen und Pegel



Frequenzaufbereitung - Übersicht

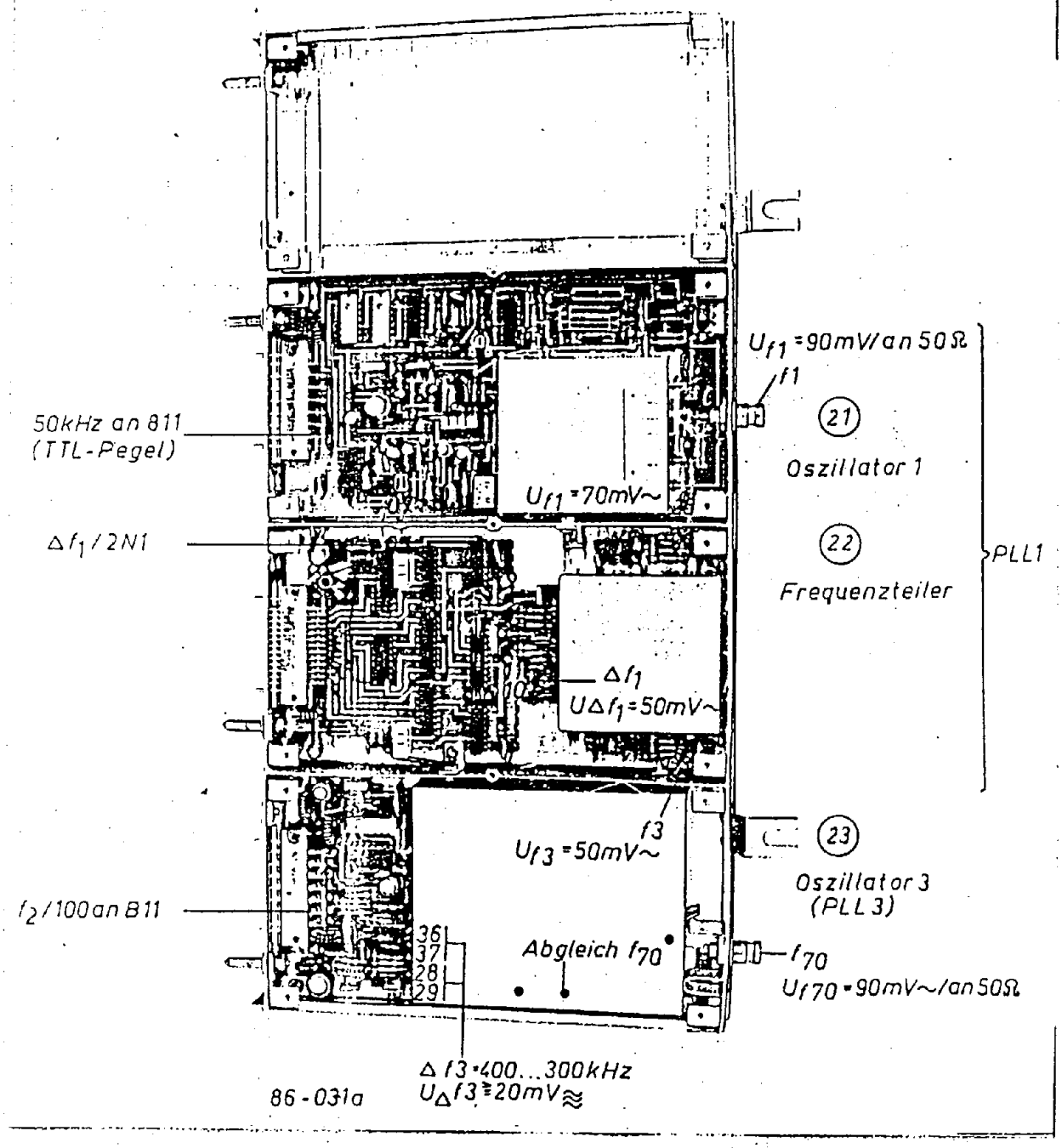
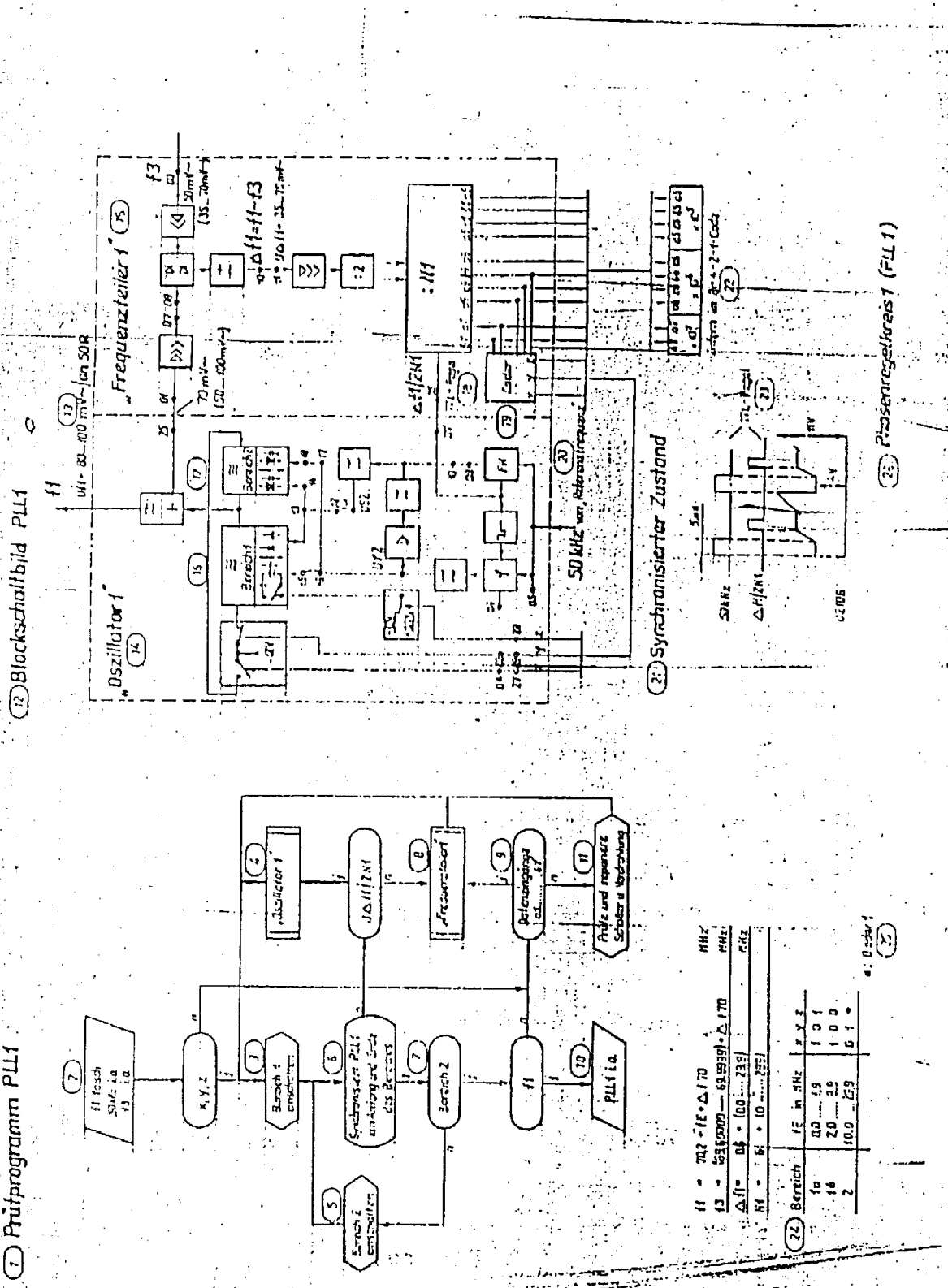


Figure 14

Frequency processing 1 1340.041-01211

6.3.3. Phase-lock loop 1 (PLL1)



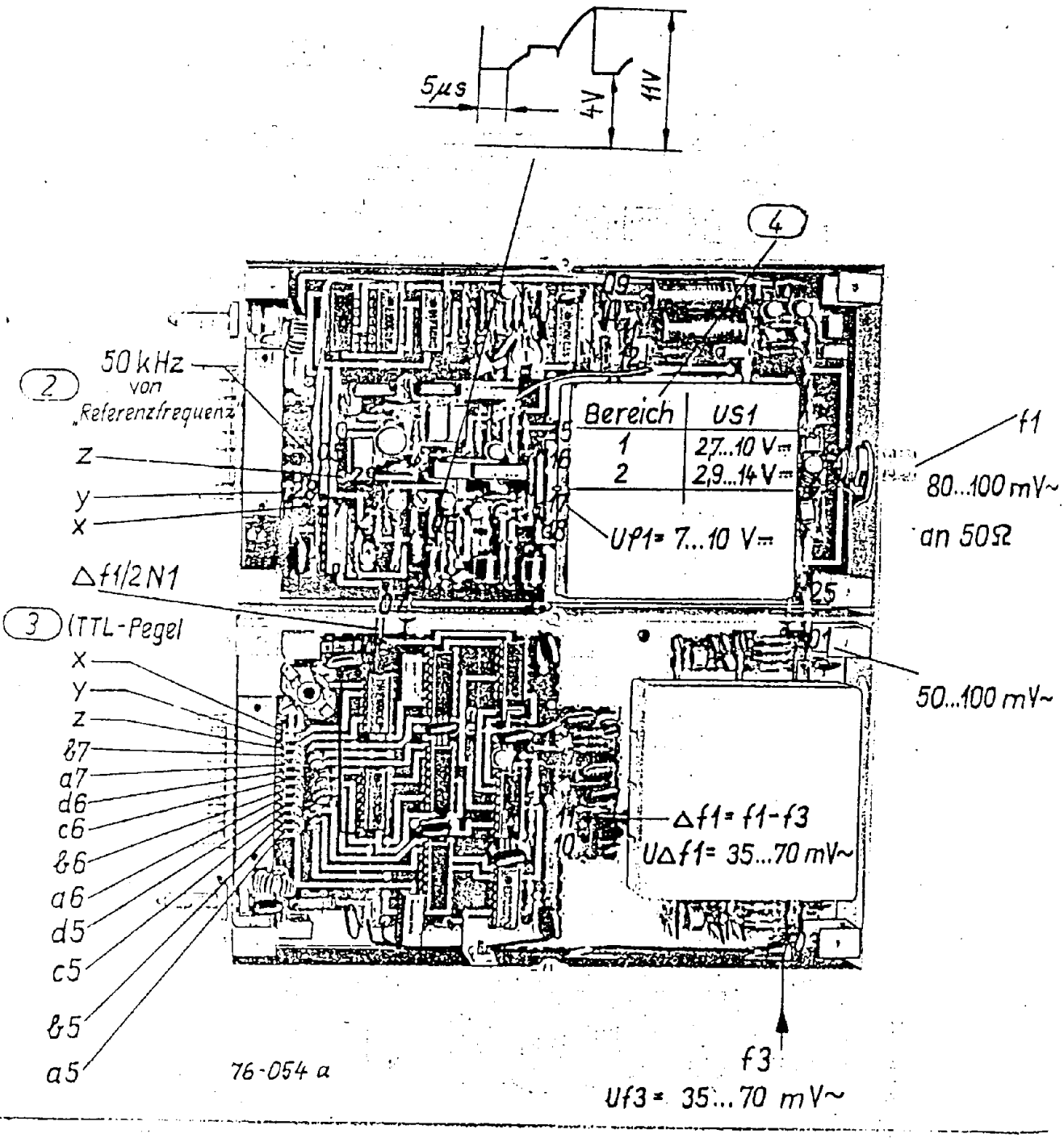


Figure 15
Positions of test points PLL1

6.3.4. Oscillator 1

(1)

Kontrolle des [illegible] (Fanghilfe)

D01, D02, D03, V10, V11 u. V12

Brücke 09...10 öffnen

Brücke 11...12 öffnen

an 12 ca. +3 V anlegen (C15 hat geeignete Spannung)

fe	f1/N1	D03 Pin 2	D03 Pin 5	09
10 000 00	> 50 kHz			< 1 V
30 000 00	< 50 kHz			> 14 V

Kontrolle des Verstärkers N02

Brücke 09...10 öffnen

Brücke 11...12 öffnen

Mit R2125 einstellen:

[illegible]

[illegible]

Abgleich der Oszillatorfrequenz

Wenn V2125, V2125, V2125 oder V2125 gewechselt werden, ist ein Abgleich der Oszillatoren notwendig. Der Abgleich erfolgt im Bereich 1 mit C24 und im Bereich 2 mit C34 durch Wechseln der Kondensatoren.

Abgleichbedingungen (mit Abschirm-Kappe gemessen?)

Frequenz-Einstellung	U_S an Pkt. 11 (P 8, R_i > 3 MOhm)
1. 10 000 00	2,7...2,9 V = U (1.)
2. 30 000 00	< 14 V
3. 31 000 00	synchronisiert ?
4. 00 000 00	U (1.) - 0,2 V
5. 09 999 99	9...11 V

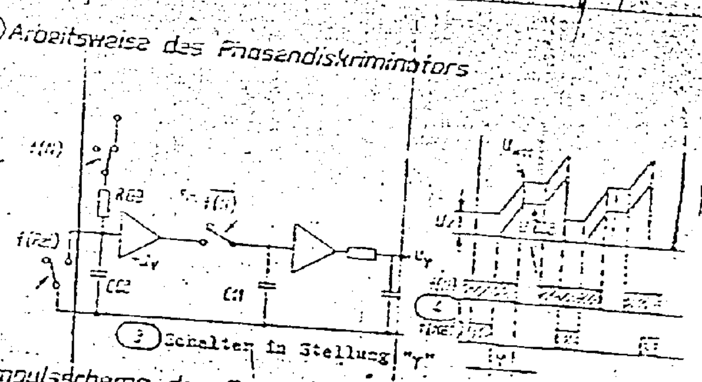
Abgleich des Phasendiskriminators

Einstellen mit R 2125

U_P = 7...10 V an Pkt. 15...18 bei f_E = 20 000 00

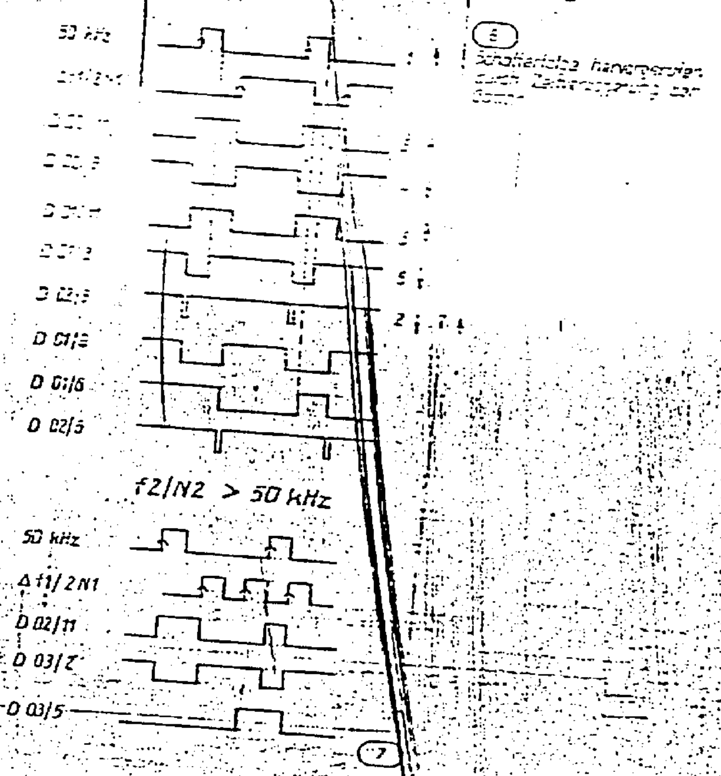
Oszillogramm an C2108 und R2111 beachten!

(2) Arbeitsweise des Phasendiskriminators



(3) Schalter in Stellung "Y"

(5) Impulsschema des Frequenzdiskriminators



Oszillator 1

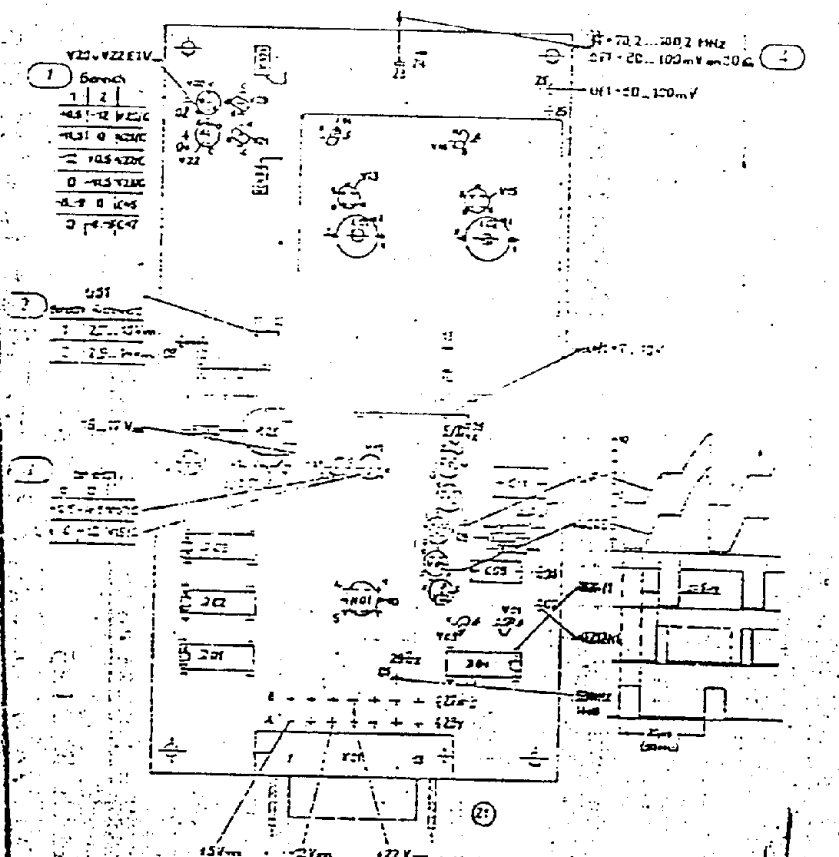
Test sequence

No output voltage f1

1. UC45 or UC47
2. U 1 (15...18)
3. US1 (12)
4. Does oscillator work?

Control circuit does not synchronize (OG)

1. Operating voltages
2. 50 kHz (ref) (05)
3. ΔF1/2N1 (07)
4. UF1 (15...18)
5. US1 (12)
6. Open bridge 11...12, apply approx. +8 V dc to 12, synchronize with frequency switch '10 MHz' and '1 MHz'
7. Check capture aid and N 02
8. Balance phase discriminator



Prüfablauf

Keine Ausgangsspannung Z1

1. UG45 bzw. UG47
2. U 1 (15..18)
3. US1 (32)
4. schwingt Oszillator ?

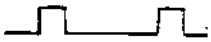
Regelkreis synchronisiert steht (G6)

1. Betriebsspannungen
2. 50 kHz (Ref) (G5)
3. ΔP1/2?? (G7)
4. US1 (15...18)
   ?? (32)
5. Brücke 17...18 ziehen, an 12 ca. +6V= anlegen, die Frequenzanzeige muß [illegible] synchronisieren
6. Tastköpfe auf 12 Oszilloskop
7. Abgleich Phasendiskriminator

Check of the frequency discriminator (capture aid)

D01, D02, D03, V10, V11 and V12

Open bridge 09 ... 10
Open bridge 11 ... 12
Apply approx. +8 V dc to 12 (suitable voltage applied to C15)

fe	f1/N1	D03		
		Pin 9	Pin 5	09
10 000 00	> 50 kHz			< 1 V
30 000 00	< 50 kHz			> 14 V

Ckeck of the amplifier N 02

Open bridge 09 ... 10
Open bridge 11 ... 12

Adjust with R 2125

$U_{pin\ 4} >> U_{pin\ 5}$ ⟶ U (11) < 2 V

$U_{pin\ 4} >> U_{pin\ 5}$ ⟶ U (11) >13 V

Balancing the oscillator frequency

After replacing V 2125, V 2126, V 2128 or V 2129 the oscillators have to be balanced. Balancing is performed in range 1 with C24 and in range 2 with C34 by exchanging the capacitors.

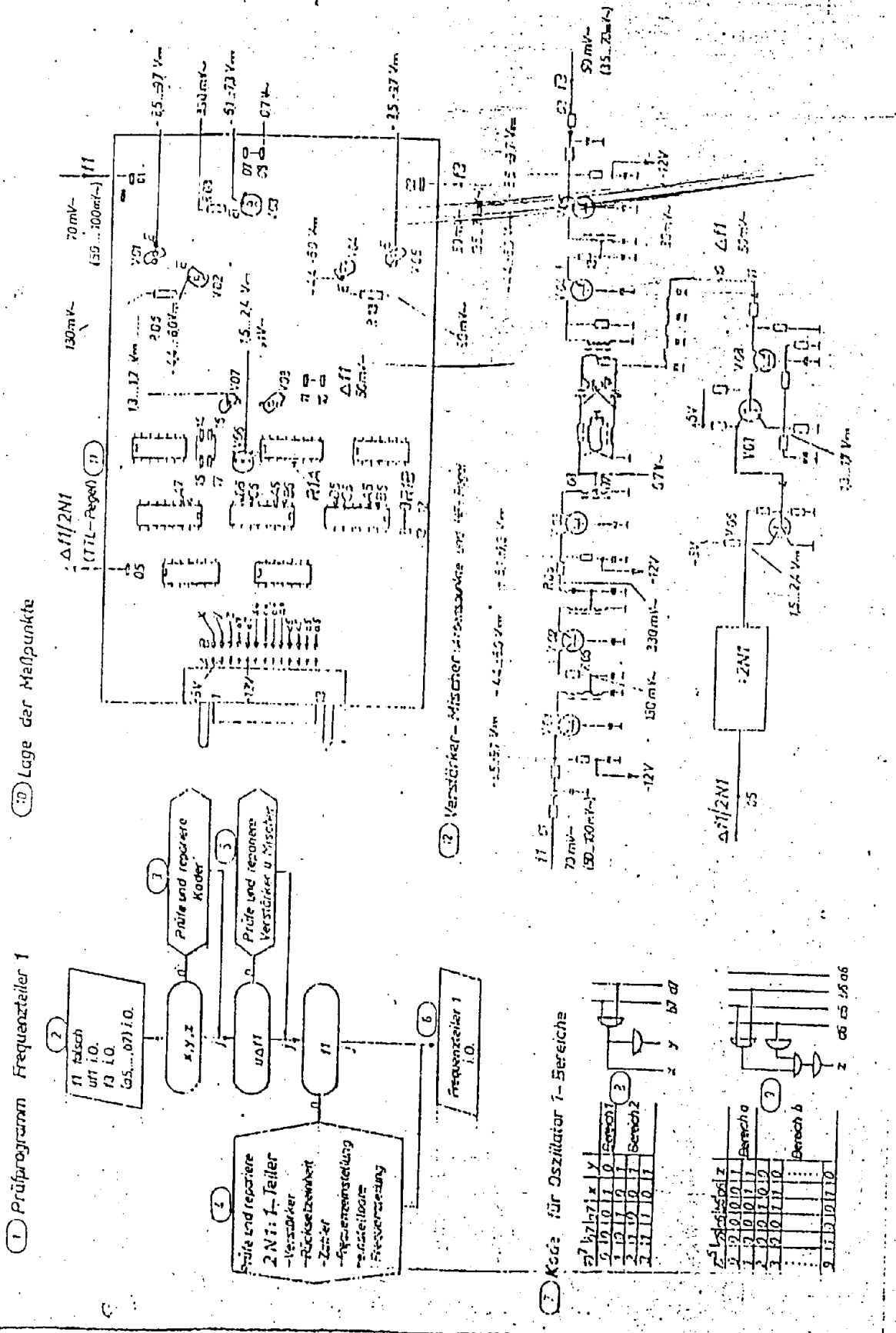
Balancing conditions (had measurement been performed with screening cap?)

Frequency setting	U_S at point 11 P 8, R_i 3 Mohm
1. 10 000 00	2.7 ... 2.9 V = U (1.)
2. 30 000 00	<14 V
3. 31 000 00	synchronized ?
4. 00 000 00	U (1.) - 0.2 V.
5. 09 999 99	9 ... 11 V

Balancing the phase discriminator

Setting with R 2125
U φ = 7 ... 10 V at point 15 ... 18 at f_E = 20 000 00
Obsereve oscillogram at C 2108 and R 2111!

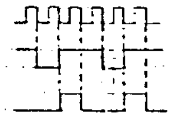
6.3.5. Frequency divider 1



(1) Prüfung des Einstellbaren Frequenzteilers 1

- Rücksetzeinheit (3:1 - Teilung)

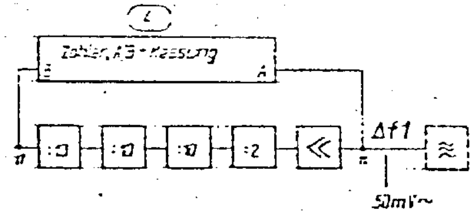
(2)
- Brücken 12 - 13 offen; 14 - 15 verbunden; 16 - 17 offen; 12 - 16 verbunden — Takt an D7/5; $\overline{R1A}$ an D5; R1B an 12
- 10^3 Hz - Schalter auf „1"
- U Δf1 = 50 mV~



- Zähler A/B = 2000

(3)
- Brücken 12 - 13 offen; 14 - 15 offen; 16 - 17 offen; 12 - 16 verbunden
- U Δf1 = 50 mV~

(4)



- Frequenzeinstellung

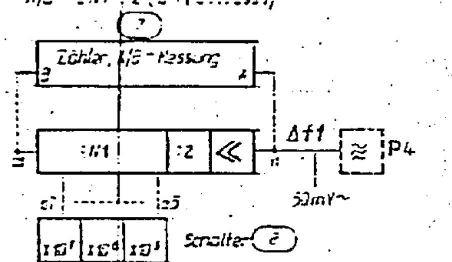
(5)
- Brücken 12 - 13 offen; 14 - 15 offen; 16 - 17 offen; 13 - 12 verbunden; 15 - 12 verbunden

- U Δf1 = 50 mV~

- Einstellbare Frequenzteilung A/B = 2N1 = 2 (6 + (0 ... 999))

(6)
- Brücken 12 - 13 verbunden; 14 - 15 verbunden; 16 - 17 verbunden
- U Δf1 = 50 mV~

(7)

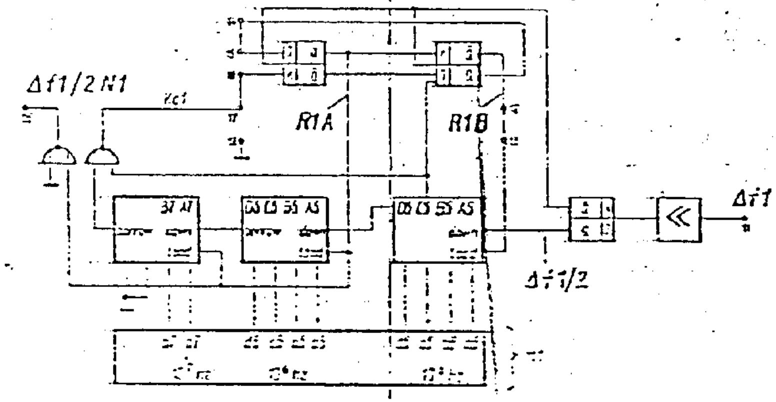


(9) Für die Fehlersuche kann man am Eingang (Punkt 11) ein Signal mit einem Pegel von 50 mV~ aus einem externen Generator (P4) einspeisen.

Einstellbarer Frequenzteiler 1

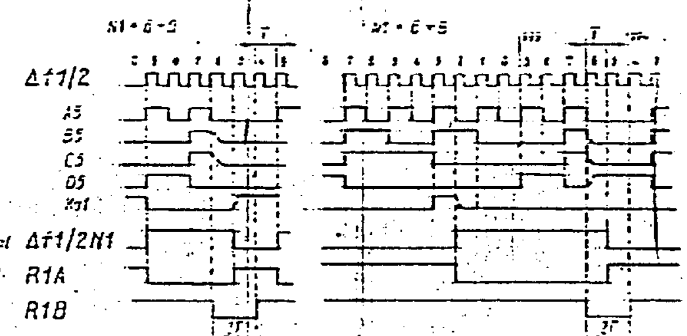
Eingangsfrequenz	Δf1 = 0,5 + 22,3 ... 29,9 MHz
(10) Ausgangsfrequenz	Δf1/2N1 = 50 kHz, im synchronisierten Zustand von PLL 1
Teilerfaktor	2N1 = 2 · (6 + N1)
Zählanfang	N1 = 000 ... 299 Ziffernzahl im 8-4-2-1-Code
Zählende	n1 = 994
Zählung	rückwärts, im 8-4-2-1-Code

(11) Blockschaltbild



Impulsdiagramme für 2 Beispiele

(12)



(13) Frequenzteiler 1

Level balancing: Accomplish the following adjustments:

With L 04	70-MHz voltage at 17 to minimum
With L 02	70-MHz voltage at 17 to maximum
With R 37	70-MHz voltage at 26
With R 28	70-MHz voltage at 17

Frequency balancing

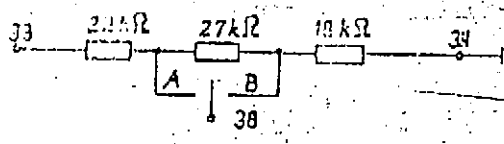
Balance f = 70 MHz with L 03, $\Delta f < \pm 150$ Hz.

6.3.6.2. f_3 oscillator

Level balancing f_3:

Set 03 to ~ 50 mV/50 ohm with R 02 (tapping on the coil decoupling loop of L 01).

Frequency balancing f_3:



Open bridge 38/39.

Apply positive voltage via opposite voltage divider to 38.

In position A (10 V dc) $f_3 > 69.7$ MHz; in position B (4 V dc) $f_3 < 69.6$ MHz. If this cannot be reached, change C 04. Increasing C 04 causes decrease of frequency.

6.3.6.3. Phase discriminator

Image wave test:

$f_3 > 70$ MHz --→point 9/D02=low level--→$U_{39} < 2$ V dc

Capture test:

$f_2/100 = 350$ kHz at 39

$f_3 < 69.650$ MHz --→wide negative pulses at point 5/D-02

--→$U_{39} > 13$ V dc

$f_3 > 69.650$ MHz --→wide negative pulses at point 5/D-02

--→$U_{39} < 2$ V dc

(The narrow negative pulses presenting at point 9/D-02 or 5/D 02 - approx. 50 ns - are only visible with appropriate setting of the oscillograph.)

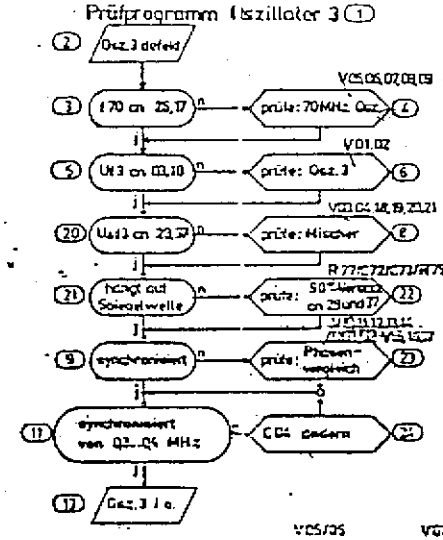
Phase discriminator:

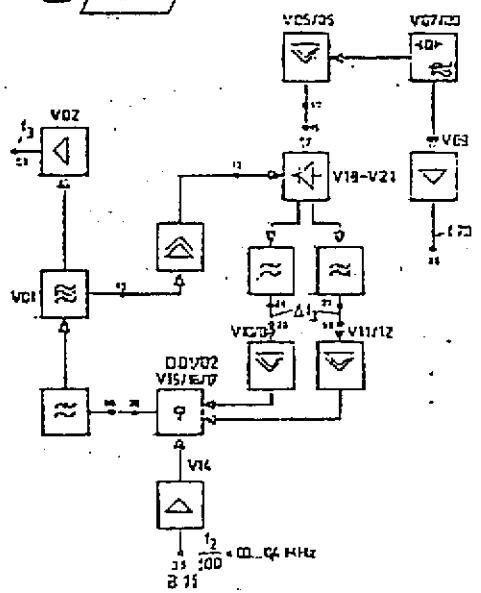
Close bridge 38/39.

PLL synchronized ($U_{39} = +4 \ldots +11$ V).

In case of triggering with $f_2/100$ the oscillograph supplies a stationary pattern of P30 and P54.

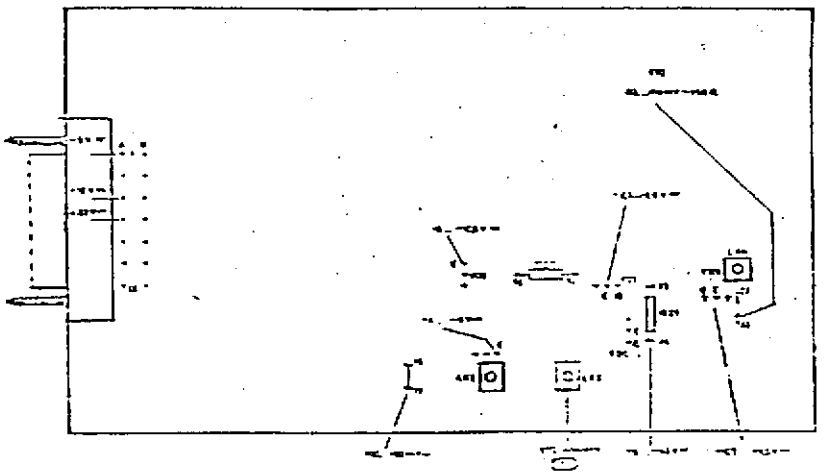
Prüfprogramm Oszillator 3 (1)

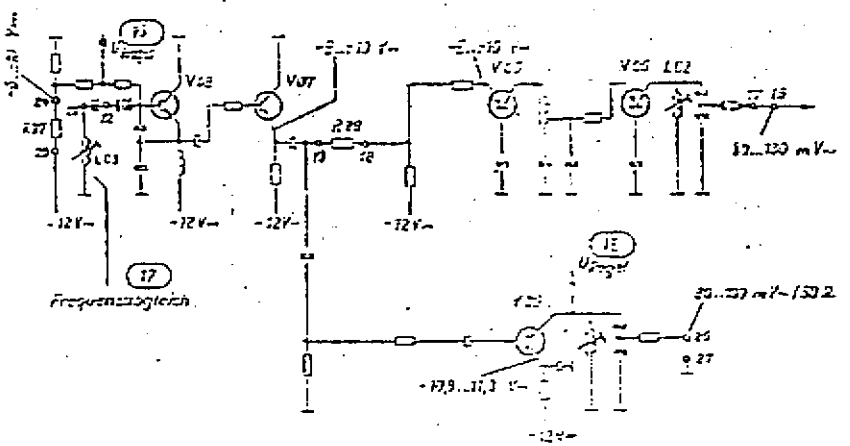


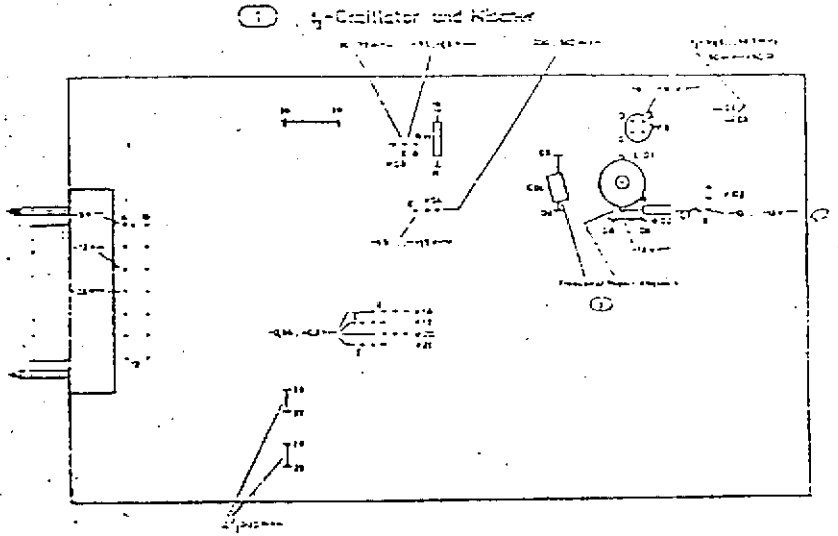


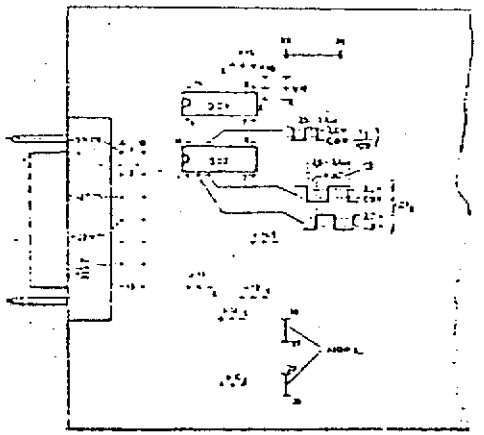
(73) Oszillator 3

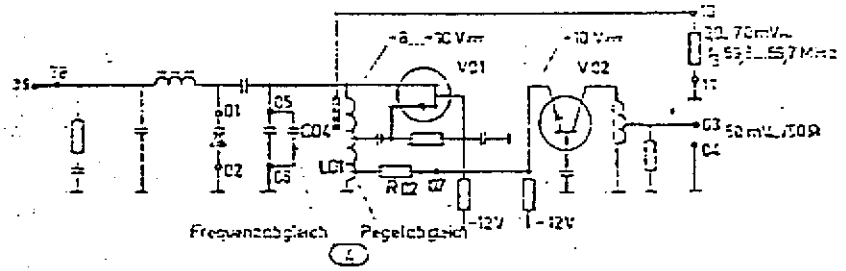
(1) 70 MHz-Oszillator

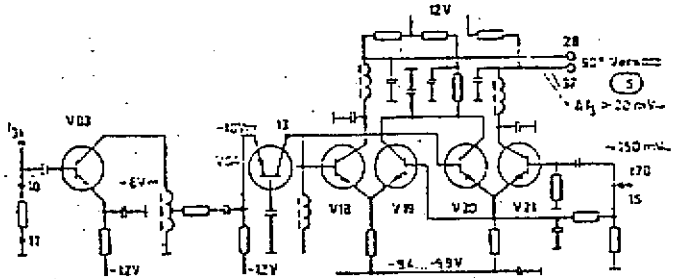


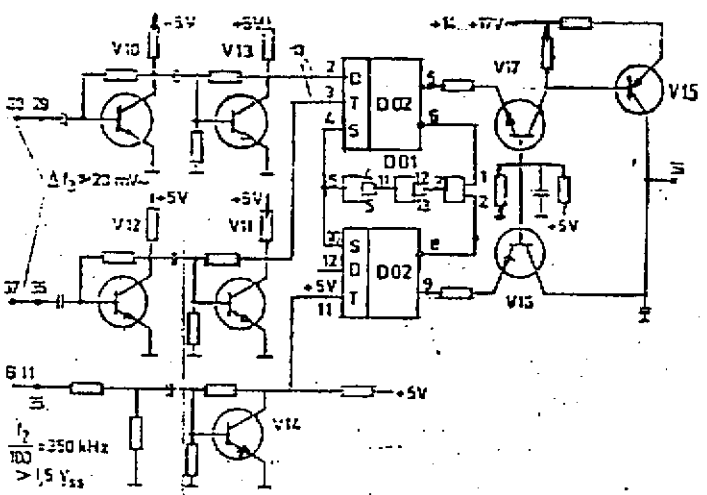












Oszillator 3

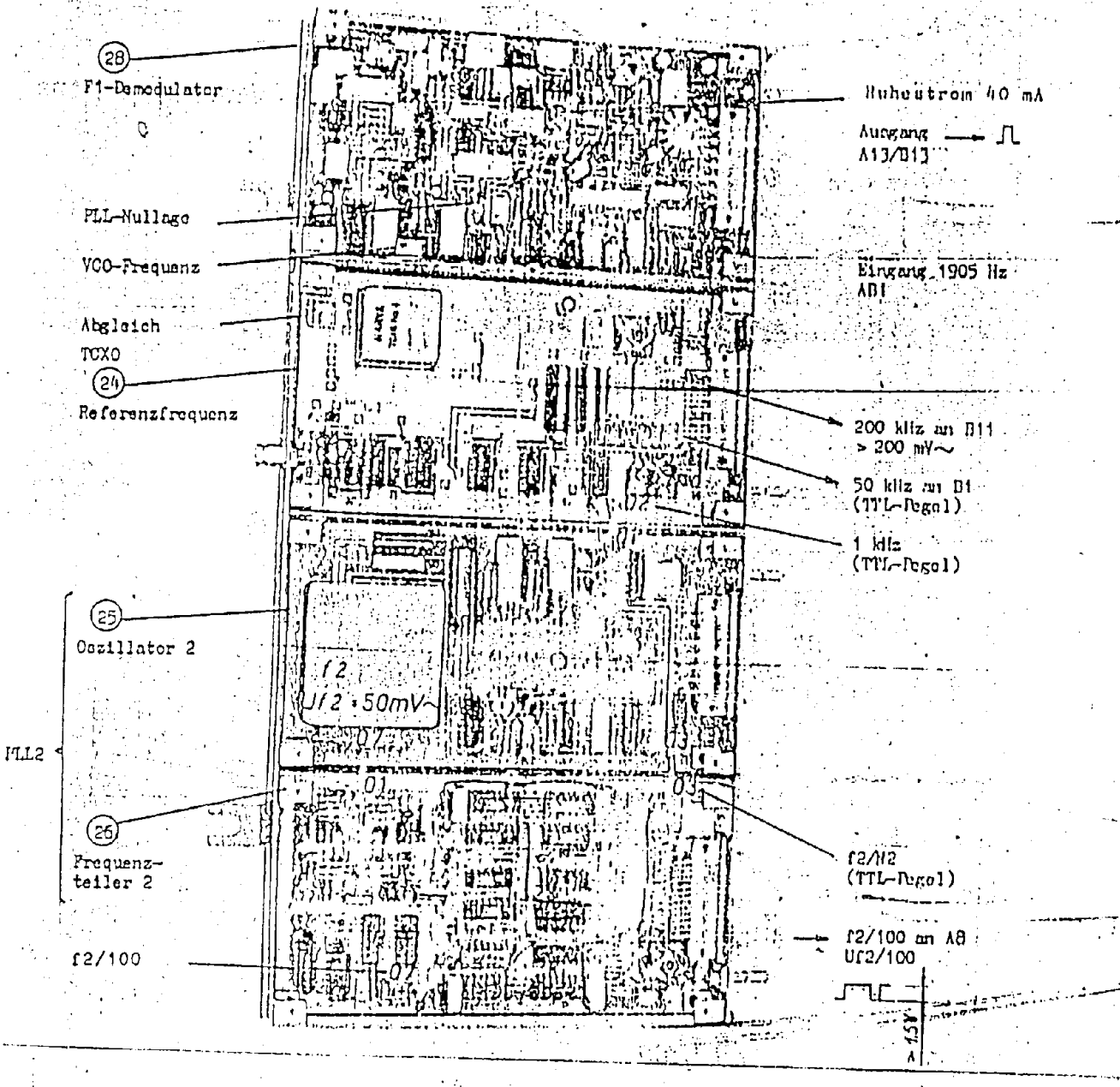


Figure 16 Frequency processing 2 and F1 - Demodulator 1340.041-01221

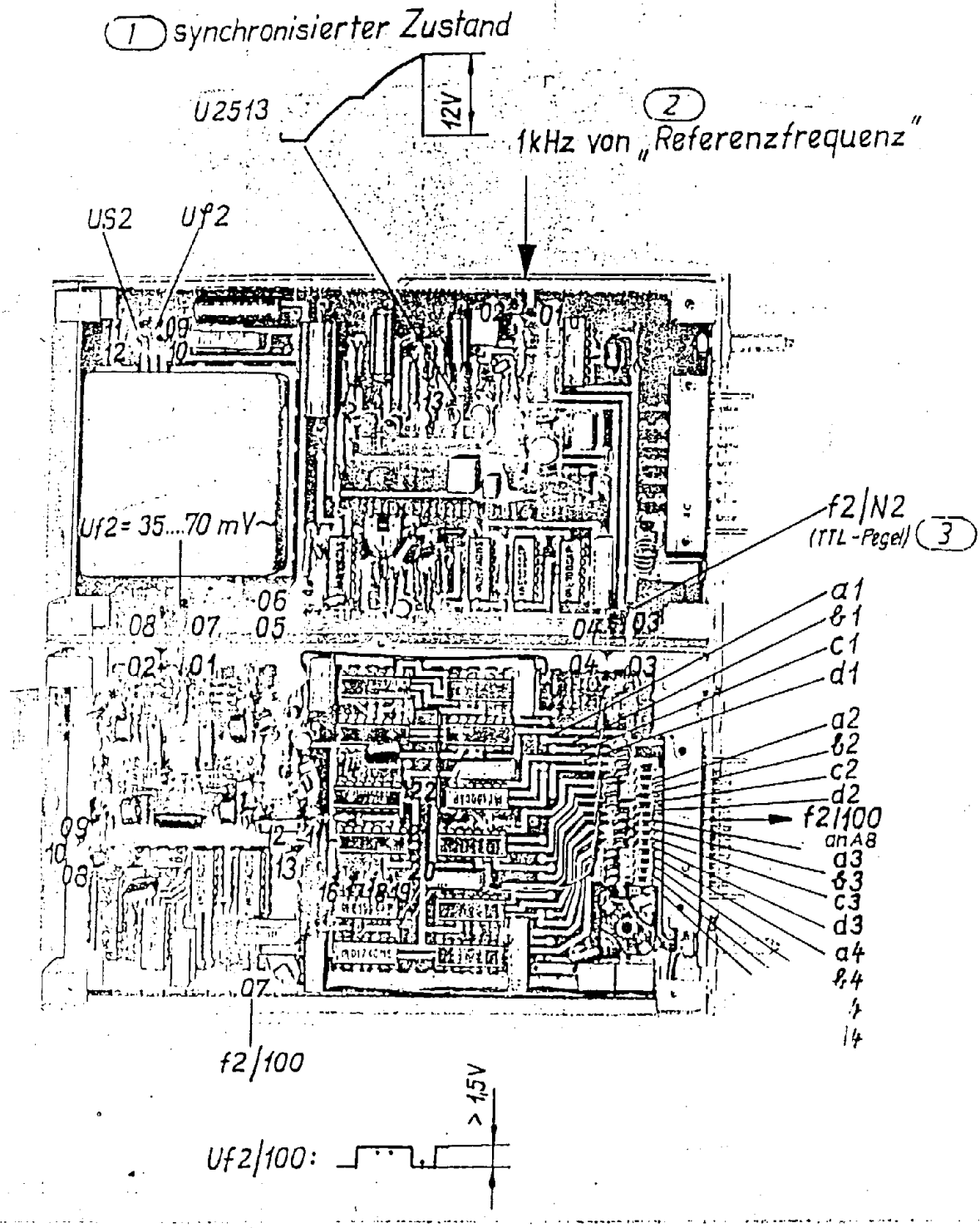
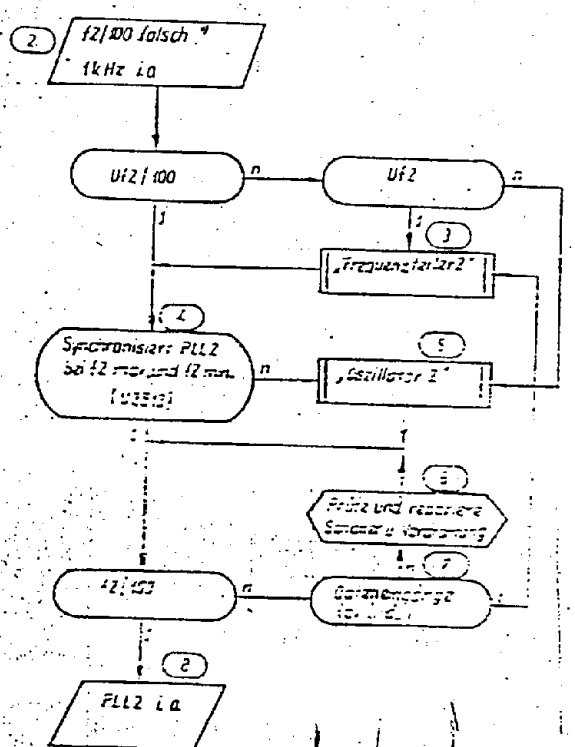


Figure 17

- Position of test points PLL 2

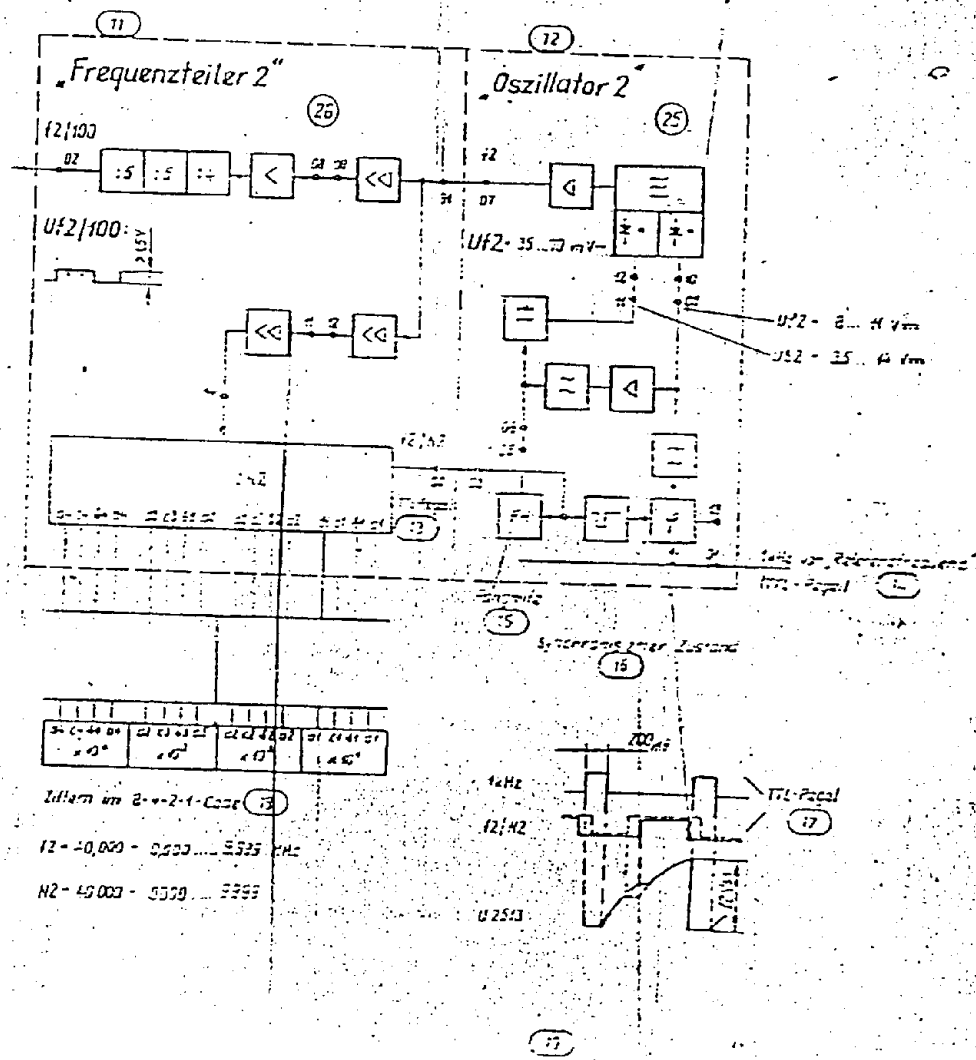
(1) Prüfprogramm PLL2



(9)

* falsch: - kein Ausgangsimpuls f2/100
- PLL2 synchronisiert nicht
- PLL2 synchronisiert über Frequenz falsch

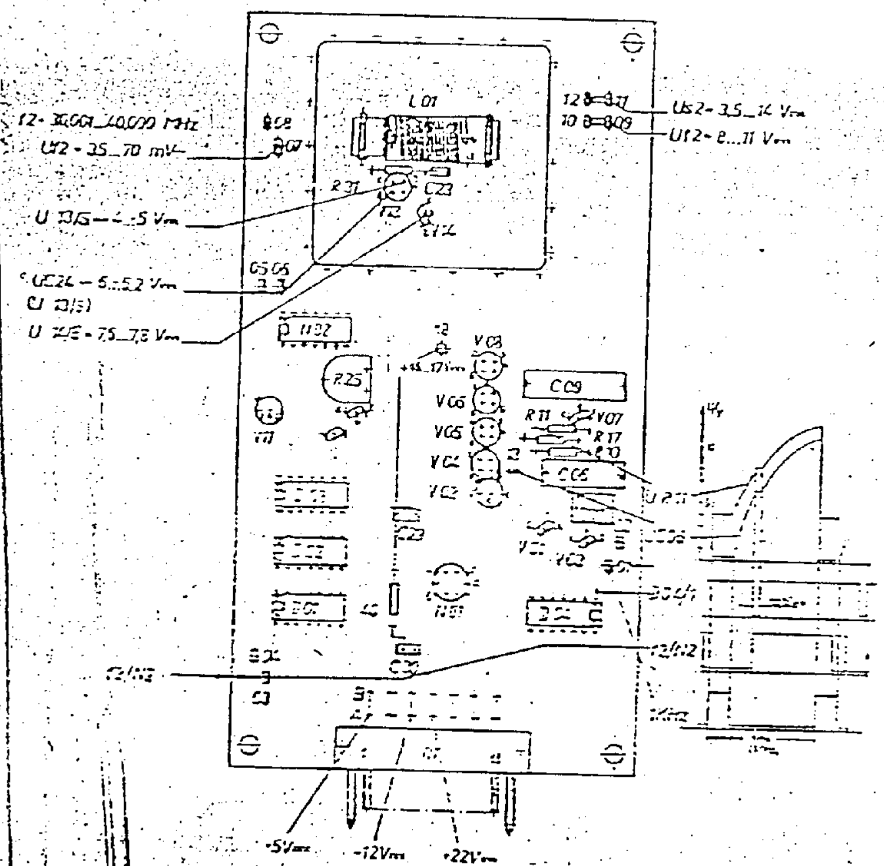
(10) Blockschaltbild PLL2



(27)

Frosenregelkreis 2 (PLL2)

6.3.8. Oscillator 2



P r ü f a b l a u f

Keine Ausgangsspannung f2

1. −12 V (C39)
2. − 9 V (C29)
3. Uf2 (10)
4. US2 (12)

(1) Regelkreis synchronisiert nicht (11)

1. Betriebsspannungen
2. 1 kHz (Ref) (01)
3. f2/N2 (03)
4. Uf2 (10)
5. U_S2 (12)
6. Brücke 11...12 öffnen, an 12 ca. +6 V= anlegen, mit Frequenzschalter "10 kHz" u. "1 kHz" synchronisieren
7. Fanghilfe und AFC überprüfen
8. Abgleich Phasendiskriminator

No output voltage f2

1.	-12 V	C30
2.	-9 V	C29
3.	U 2	(10)
4.	US2	(12)

1

1. Operating voltages
2. 1 kHz (ref) (01)
3. f2/N2 (03)
4. U 2 (10)
5. U_g2 (12)
6. Open bridge 11...12, apply approx. +8 V dc to 12, synchronize with frequency switch '10 kHz' and '1 kHz'
7. Check capture aid and N 02
8. Balance phase discriminator

6.4.1.9. Kontrolle "Regelgleichlauf/Kanal A und B, Automatikregelung"

- EKD: F 4 500.00 kHz, MOD 6, B 6, SEL 0, GC 1, df 2.00 kHz
- auf jeweils 1000 Hz-Ton im Kanal A bzw. B abstimmen
- P4-EMK = 2 µV ... 200 mV in 20 dB-Schritten schalten, Meßwert P3 (A) bzw. (B) = -3,5 dBm ... 3,5 dBm, maximale Pegeldifferenz zwischen (A) und (B) ≤ 2 dB

6.4.1.10. Einstellen "Regeleinsatz Regelglied 1" (Mischer 1)

- HF-Generator P4 an Empfängereingang X 3004 (Y), f = 4501 kHz, EMK = 100 µV.
- ZF2 - Übergabepegel an X 3001 mit Millivoltmeter P3 messen (über BNC-T-Stück — Zubehör),
- EKD: F 4 500.00 kHz, MOD 4, B 7, SEL 0, GC 5, ⊿≈▽ mit P4 auf ca. 1000 Hz-Ton im Kanal A abstimmen.
- ZF2 - Übergabepegel - Sollwert: 5,5 ± 0,5 mV.
- Auf GC 1 umschalten, Mit R 3836 auf - 12 dB unter den bei GC 5 ⊿≈▽ von P3 angezeigten Pegelwert einstellen.

6.4.1.11. Einstellen "Trigger - Regelverstärker"

- HF-Generator P4 an Empfängereingang X 3004 (Y) f_E 4 500.00 kHz, EMK = 1 µV
- EKD: F 4 500.00 kHz, MOD 4, B 7, SEL 0, GC 2, Mit P4 auf ca. 1000 Hz-Ton im Kanal A abstimmen
- mit Digital-Voltmeter P9 Kollektorspannung an V 3826 messen und R 3813 so einstellen, daß U_C = V 3826 auf ca. +18 V springt und diesen Wert beibehält.

Zur Kontrolle: P4-EMK von 30 µV in 10 dB-Schritten schalten. U_C = V 3826 muß kurzzeitig < 1,5 V werden und wieder auf ca. +18 V ansteigen.

Check of the frequency discriminator (capture aid)

D01, D02, D03, V10, V11 and V12

Open bridge 05...06

Open bridge 11...12

Apply approx. +8 V dc to 12 (suitable voltage applied to C14)

fe	f2/N2	D03		
		Pin 9	Pin 5	05
xxx 9999	> 1 kHz	———	⊓⊓	< 1 V
xxx 0000	< 1 kHz	⊓⊓	———	> 14 V

Check of amplifier N 02

Open bridge 05...06

Open bridge 11...12

Adjust with R 2525

$U_{pin4} >> U_{pin 5}$ ⟶ U (11) < 2 V

$U_{pin 4} << U_{pin 5}$ ⟶ U (11) > 13 V

Balancing the oscillator frequency

After replacing V 2516 or V 2517/19 (KB105B) the frequency range o
the oscillator is to be checked. Balancing is performed with
additional winding at L 2501-wire 0.6 mm Ø CuL.

Possibilities: 2 turns in equal direction of winding
1 turn " " "
0 " " "
1 turn in opposite direction of winding

fe	f2	U point 12
xxx 0000	40 0000 kHz	< 14 V type 13 V P 8, R_i > 3 M
xxx 9999	30 0001 kHz	> 3.5 V type 4.5 V

x = optional setting put on shielding cap for meas

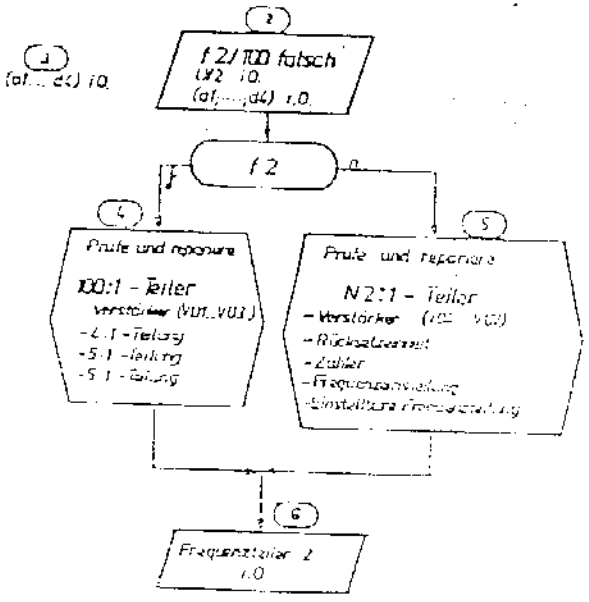
Balancing the phase discriminator

Adjustment with R 2525

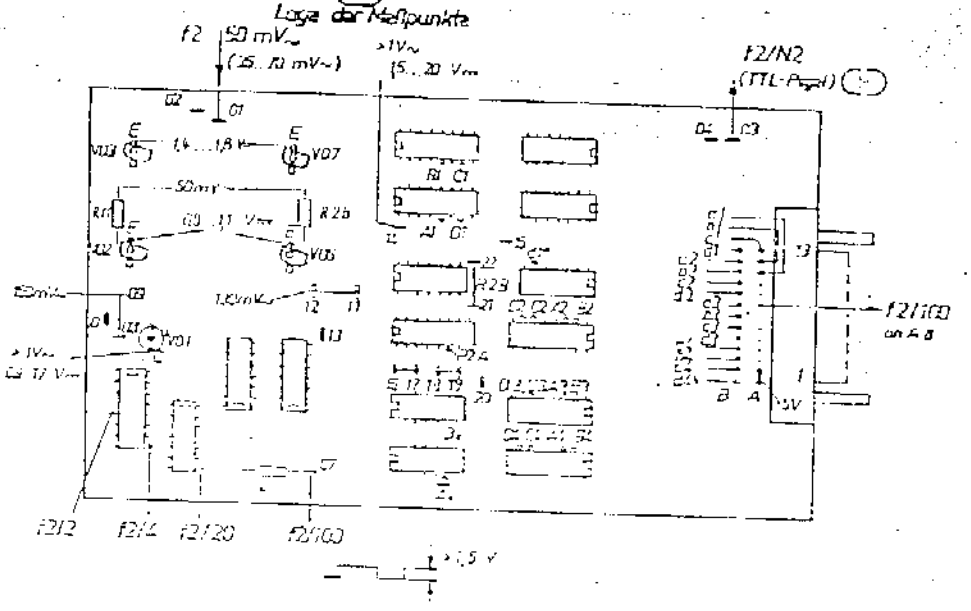
U φ = 8...11 V at point 09 with f_E = xxx 5000

Observe osoillogram at C 2506 and R 2511!

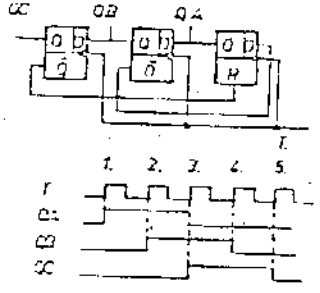
(1) Prüfprogramm Frequenzteiler 2



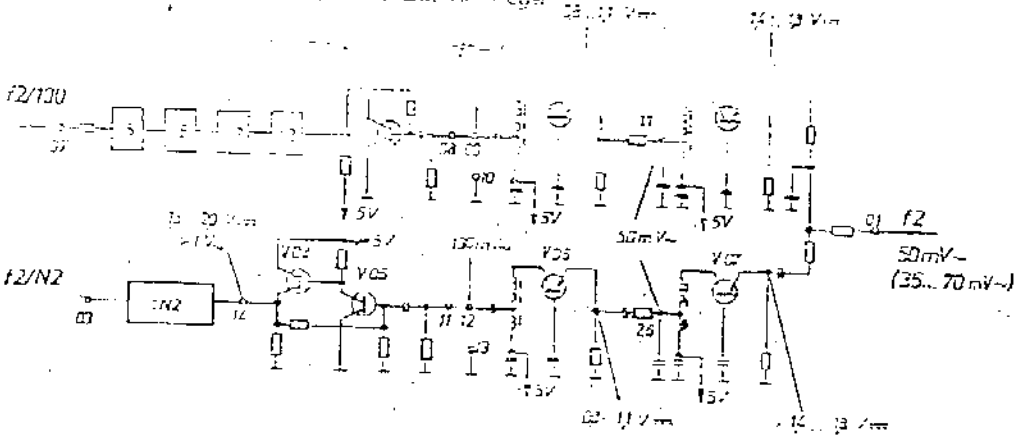
(6) Lage der Meßpunkte



(7) Prinzip des 5:1-Teilers



(8) Verstärker-Arbeitspunkte und HF-Pegel



(1) Prüfung des Einstellbaren Frequenzteilers 2

-Rücksetzeinheit (3:1 - Teilung)

(2)
- Brücken 16 - 17 verbunden
  18 - 19 offen
  21 - 22 verbunden
  18 - 17 verbunden
- 10 Hz - Schalter auf „1"
- Uf2 - 50 mV~

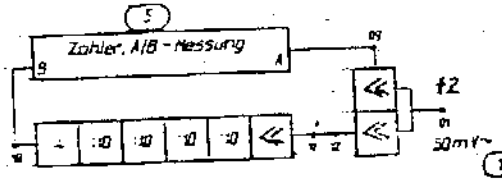
Takt an 14

(3) R2A an 20/6

R2B an 21

-Zähler A/B - 40 000

(5)



(4)
- Brücken 16 - 17 verbunden
  18 - 19 offen
  21 - 22 verbunden
- Uf2 - 50 mV~

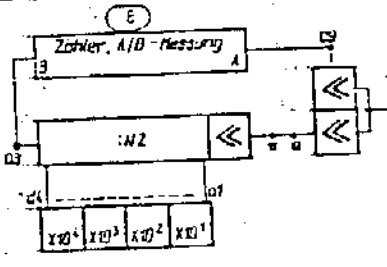
-Frequenzeinstellung

(6)
- Brücken 16 - 17 verbunden
  18 - 19 offen
  21 - 22 verbunden
  16 - 20 verbunden
- Uf2 - 50 mV~

-Einstellbare Frequenzteilung A/B - N2 - 40 000 - (0000...9999)

(7)
- Brücken 16 - 17 verbunden
  18 - 19 verbunden
  21 - 22 verbunden

(8)



- Uf2 - 50 mV~

(9) Für die Fehlersuche kann man an Punkt 11 ein Signal mit einem Pegel von ca. 150 mV~ und einer Frequenz < 30 kHz einspeisen (P 4).

(10) Einstellbarer Frequenzteiler 2

Eingangsfrequenz	f2 - 40 000 - (0 000 ... 9999) kHz
Ausgangsfrequenz	f2/N2 - 1 kHz, im synchronisierten Zustand von PLL 2
Teilerfaktor	N2 - 40 000 - K2
Zählumfang	K2 - 0000 ...9999. Ziffernwahl im 8-4-2-1-Code
Zählende	n2 - 40 000
Zählung	- 10 kHz-, 1 kHz und 100 Hz-Dekade im 8-4-2-1-Code - 10 Hz-Dekade und 2 Bit-Binärzähler siehe Tabellen

(11) 10 Hz-Dekade

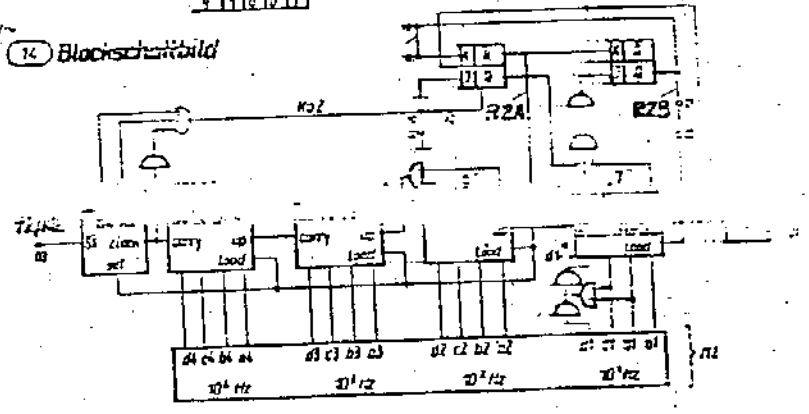
	d03	d2	d01	d1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

(12) d1 wird umkodiert

(13) 2 Bit-Binärzähler

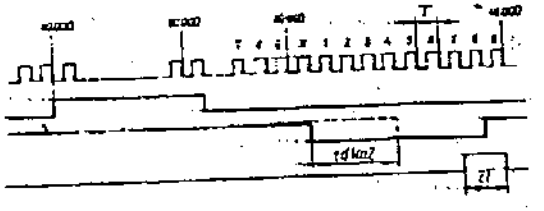
	13	A2
0		
1		
2		
3		

(14) Blockschaltbild



Impulsdiagramm

(15)



6.4. Signal path

6.4.1. Check or correction of levelling

Open cassette lid (complementation side) of cassettes 'signal path 1' and 'signal path 2' and fasten outer cassettes in hinged position with cassette support (contained in the accessories).

6.4.1.1. Basic amplification 'signal path 1'

- RF generator (P4) to receiver input X 3004 (Y)
  f_B = 4 500 kHz, emf = 1 mV
- RF millivoltmeter P2 (150-mV range) via BNC-T-piece (accessories) at X 3002 (IF2 = 200 kHz)
- EKD: [F] 4 500.00 kHz, [MOD] 4, [B] 5, [SEL] 0, [GC] 5
- Tune with P4 to zero beat (required forward centre)
  Test value P2: 50 to 60 mV
- Correction: 'coarse' with R 3434, 'fine' with R 3409 when holding the control volume for 'signal path 1': 60 $^{+2}_{-1}$ dB

6.4.1.2. Control volume 'signal path 1'

- Actual value from point 6.4.1.1. (test value P2) is the reference value
- P4 - emf = 1 V
- Test value P2: Actual value from point 6.4.1.1. $^{+1}_{-2}$ dB
- Correction: with R 3409

6.4.1.3. Mixer - symmetry

- Receiver input X 3004 (Y) not connected
- P2 (500-mV range) to X 3002 (IF2 = 200 kHz) via BNC-T-piece (accessories)
- EKD: [F] 0.00 kHz, [MOD] 4, [B] 5, [SEL] 0, [GC] 5
- Test value P2 ≦ 200 mV
  Correction (minimization): with C 3336 (balancing capacity)

Channel A and B, manual control)

- RF generator P4 to X 0001 (casing) and via connection cable to X 3004 (plug-in).

  f_E = 4 500 kHz, emf = 1 µV

- AF millivoltmeter P3 and load resistance 600 ohm in parallel to line output A (25) and B (26)
- EKD: [F] 4 500.00 kHz, [MOD] 6, [B] 7, [SEL] 0, [GC] 5 ⌀ ≈ Y [df] 2.00 kHz
- Tune with P4 to approx. 1000-Hz tone in channel B, test value P3 (B): +1 dBm, correction with R 3617 *)
- Set 1000-Hz tone with rotary button (2.00-kHz step) in channel A, test value P3 (A): +1 dBm, correction with R 3855 ж) maximum level fault: 0.5 dB.

6.4.1.5. Levelling 'A3E'

- RF generator P4 to receiver input X 3004 (Y)
  f_E = 4 500 kHz, emf = 5 µV, m = 0.5 f_{mod} = 1 kHz
- AF millivoltmeter P3 in parallel to 600-ohm load resistance at AF line output A (25)
- EKD: [F] 4 500.00 kHz, [MOD] 2, [B] 6, [SEL] 0, [GC] 1
- Tune with P4 1000-Hz tone in channel A to minimum noise
- Balance test value P3 (A) = -1 dBm by means of R 3847 ж)

6.4.1.6. Changing AF line levels (max +6 dBm)

A change of the AF line levels (up to max +6 dBm) is to be carried out with
Channel A: for A3E with R 3847
for A1A, J3E, B8E (+SB) with R 3855 (Demod. and AF)
Channel B: for B8E (-SB) with R 3617 (IF 2/B)

Cf. also Sections 6.4.1.4. and 6.4.1.5.

6.4.1.7. Balancing 'control synchronism/channel A and B, man. cor

- RF generator P4, emf = 20 µV
- EKD: [F] 4 500.00 kHz, [MOD] 6, [B] 6, [SEL] 0, [GC] 5
- Tune to 1000-Hz tone in channel A or B
- Adjust test value P3 (B) = 0 dBm with ⌀ ≈
- Adjust test value P 3 (A) = 0 dBm ± 0.5 dB with R 3734
- Switch P4- emf = 2 µV in 20-dB steps and set test value P3 (B) = 0 dBm with ⌀ ≈
- Maximum level difference between (A) and (B): ≦ 1.5 dB

ж) For increased AF output level (e.g. + 6 dBm) balance to a value being 6 dB higher

5.4.1.8. Balancing 'automatic control/channel A and B'

- RF generator P4, emf = 200 mV
- EKD: F 4 500.00 kHz, MOD 6, B 7, SEL 0, GC 1, df 2.00 kHz. Tune with P4 to approx. 1000-Hz tone in channel B, set measuring value P3 (B) = +2 dBm with R 3616
- Set 1000-Hz tone with rotary button ≈ (2.00-kHz step) in channel A
- Set test value P3 (A) = +2 dBm with R 3801, max. level fault: 0.5dB
- P4-emf = 2 µV, test values P3 (A) or (B) = -2 dBm ... 0 dBm

5.4.1.9. Check 'control synchronism/channel A and B, automatic control'

- EKD: F 4 500.00 kHz, MOD 6, B 6, SEL 0, GC 1, df 2.00 kHz
- Tune to 1000-Hz tone in channel A or B
- Switch P4 - emf = 2 µV ... 200 mV in 20-dB steps
  test values P3 (A) or (B) = -3.5 dBm ... 3.5 dBm,
  maximum level difference between (A) and (B): ≦ 2 dB

5.4.1.10. Adjustment 'control start/control element 1' (mixer 1)

- RF generator P4 to receiver input X 3004 (Y), f = 4501 kHz, emf = 100 µV
- IF 2 - interposition level on X 3001 to be measured with millivoltmeter P3 (via BNC-T-element —— accessories).
- EKD: F 4 500.00 kHz, MOD 4, B 7, SEL 0, GC 5,
  Tune ≈ with P4 to approx. 1000 Hz-tone in channel A
- IF 2 - interposition level - rated value : 5.5 ± 0.5 mV
- Switch over to GC 1
- Adjust to a value -12 dB below the one read by P3 for GC 5 ≈ with R 3836.

5.4.1.11. Adjustment 'trigger - control amplifier'

- RF generator P4 at receiver input X 3004 (Y)
  f_E 4 500.00 kHz, emf = 1 µV
- EKD: F 4 500.00 kHz, MOD 4, B 7, SEL 0, GC 2
- Tune with P4 to approx. 1000-Hz tone in channel A
- Measure with digital voltmeter P9 collector voltage at V 3826 and adjust R 3813 such that U_C = V 3826 jumps to approx. +18 V and maintains this value.
  For checking: Switch P4 - emf from 30 µV to 1 µV in 10-dB steps. U_C shall decrease for a short time to < 1.5 V and increase then again to approx. +18 V.

[illegible]

(Channel A and B; manual control)

- RF generator P4 to receiver input X 3004 (Ψ)
  f_E = 4 500 kHz, emf = 30 µV
- EKD: [F] 4 500.00 kHz, [MOD] 4, [B] 7, [SEL] 0, [GC] 1
- Tune with P4 to approx. 1000-Hz tone in channel A
- Measure with digital voltmeter P9 capacitor voltage C 3808 →
- Measure with P9 the voltage at slider of R 3829 and adjust with R 3829 to a value that is 0.5 V below $U_{C\ 3808}$
  (guide value: 4.3 V − 0.5 V = 3.8 V)

6.4.1.13. <u>Balancing 'display $E_Ψ$ '(LED row and decimal digital dis</u>

- RF generator P4 to receiver input X 3004 (Ψ)
  F_E = 4 500 kHz, emf = 1 mV
- EKD: [F] 4 500.00 kHz, [MOD] 4, [B] 2, [SEL] 0, [GC] 1, TEST 3
  Changeover switch 'LED row' (2) → $E_Ψ$
- Tune P4 to zero beat (IF forward centre) .
- Balance the emf pairs in the sequence 30 µV, 30 mV and 3 µV a 1 V with the assigned preset controllers R 45145 ... R 45148 to the values 'decimal digital display' given in the table below.

	P4 - emf			
	30 µV	30 mV	3 µV	1 V
LED row	30 dB (µV)	90 dB (µV)	10 dB (µV)	120 dB (µV)
Decimal digital display	15 ± 1	45 ± 1	5 ± 1	60 ± 1
Preset controller	R 45145	R 45146	R 45148	R 45147

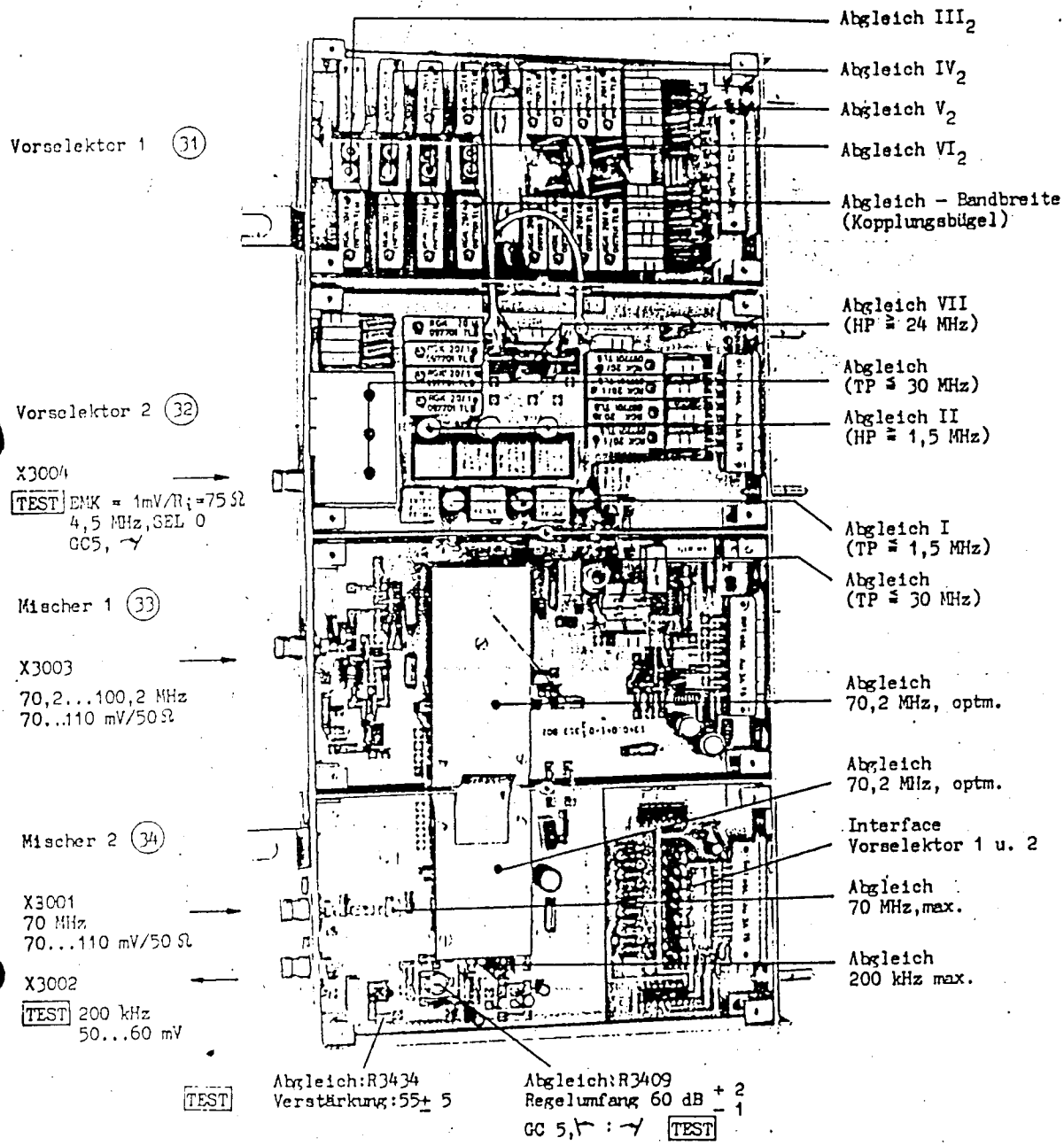
(Position of preset controller cf. Figure 1)

Note: dB (µV) = dB exceeding 1 µV i.e., 0 dB (µV)

If rated balancing cannot be achieved: change shift register R 45122 (150 kohm ... 220 kohm)

dB (µV) = dB over 1 µV , i.e. 0 dB (µV) = 1 µV

The following section provides hints on troubleshooting in the cassette 'signal path 1'.
For this purpose, the plug-in is to be connected outside the casing via adapter cable (30- and 8-core cable, contained in the accessories).
For fault localization: . dismount cassette lid (complementation side)
. perform level check according to the figure



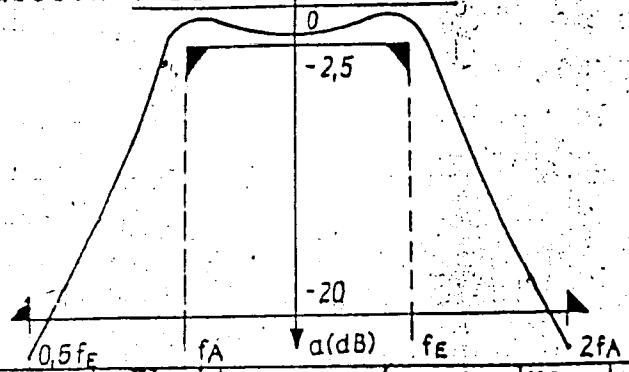
. 86-033 a

Figure 18
Signal path 1 1340.041-01311

Preselector 2, 1340.041-01352

6.4.2.1.1. - Selectivity characteristics 'preselector 1'

(Switchable suboctave filter 1.5 MHz to 24 MHz in 12 subranges)



	Pass range (≦ 2 dB) f_A ... f_E(MHz)	Blocking range (mean value ≧ 20 dB) ≦0.5 . f_E(MHz)	≧ 2 . f_A(MHz)	Balancing frequency	Balancing elements
III 1	1.5 ... 2	≧ 1	≧ 3	–	–
III 2	2 ... 2.5	≦ 1.25	≧ 4	2.25 MHz	L3101, L3102
III 3	2.5 ... 3	≦ 1.5	≧ 5	–	–
IV 1	3 ... 4	≦ 2	≧ 6	–	–
IV 2	4 ... 5	≦ 2.5	≧ 8	4.5 MHz	L3103, L3104
IV 3	5 ... 6	≦ 3	≧ 10	–	–
V 1	6 ... 8	≦ 4	≧ 12	–	–
V 2	8 ... 10	≦ 5	≧ 16	9 MHz	L3105, L3106
V 3	10 ... 12	≦ 6	≧ 20	–	–
VI 1	12 ... 16	≦ 8	≧ 24	–	–
VI 2	16 ... 20	≦ 10	≧ 32	18 MHz	L3107, L3108
VI 3	20 ... 24	≦ 12	≧ 40	–	–

Each subrange ends at f_E – 10 Hz

- For all measurements $Z_E = Z_A$ = 75 ohm
- Balancing with broad-band wobble measuring set-up (P7)*) between cassette input X 3004 and preselector 2 output P 3205.

*) When balancing with RF generator (P4), attenuate the coil that is not to be balanced with a 300-ohm resistance.

- For balancing: Remove connection to mixer 1 (P 3205 → P 3301) at P 3205: 75-ohm resistance → ⊥

- For switching on the subrange to be balanced

EKD: for range III 2: [F] 2250.00, [SEL] 1

range IV 2: " 4500.00, " 1

range V 2: " 9000,00, " 1

range VI 2: " 18000,00, " 1

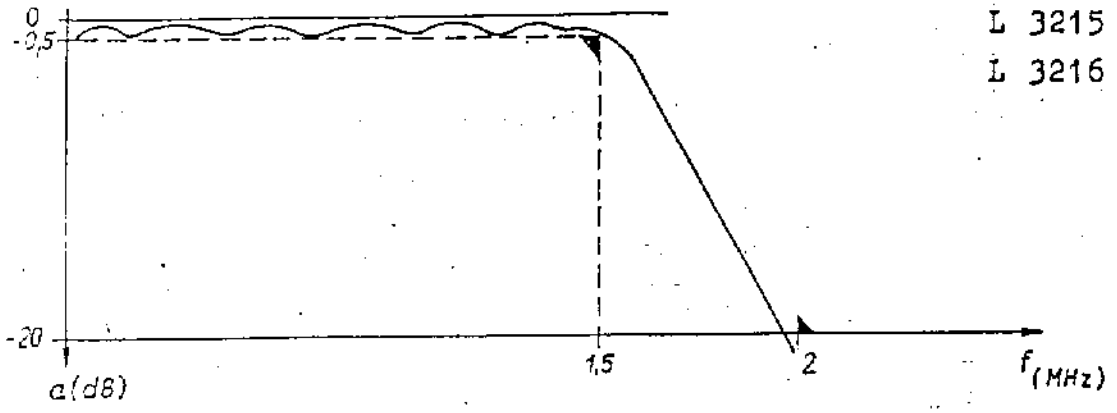
- Coil balancing according to set-point value-selectivity characteristics

Adjust with strap to insertion loss of ≦ 2.5 dB at the pass-range limits f_A and f_E with adherence to the selection ratings at 0.5 . f_E and 2 . f_A.

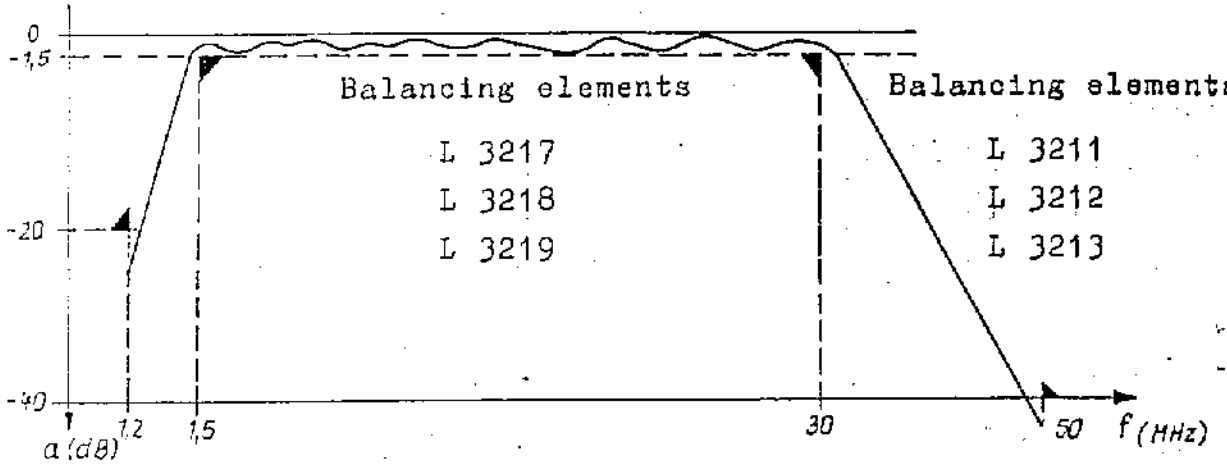
- In the other subranges (III 1 ... VI 1 and III 3 ... VI 3): Check insertion loss ≦ 3 dB and selection ratings according to 6.4.2.1.1.

Range I LP ≙ 1.5 MHz

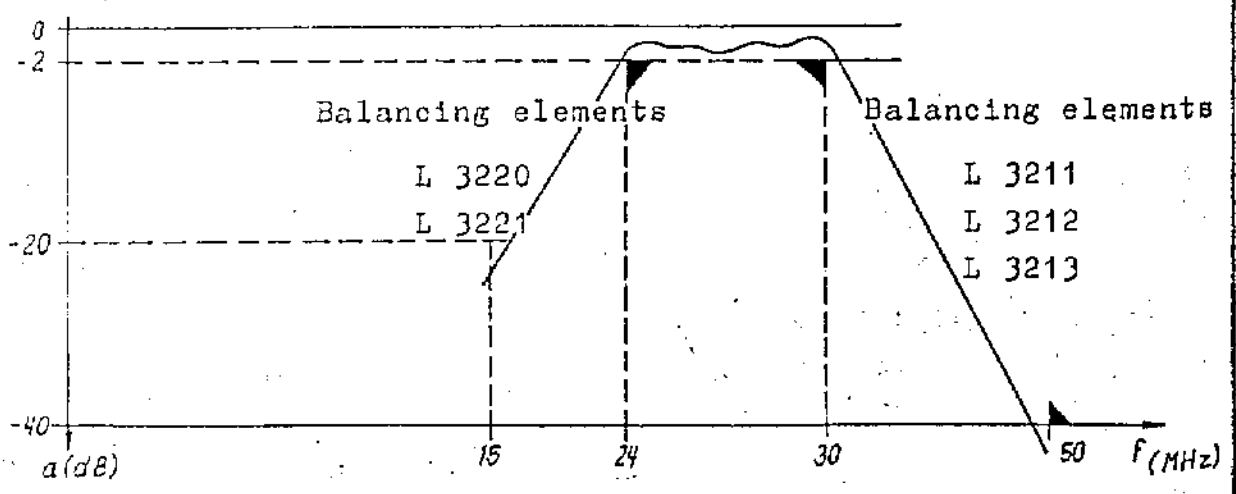
Balancing elements
L 3214
L 3215
L 3216



Range II HP ≙ 1.5 MHz LP ≙ 30 MHz



Range VII HP ≙ 24 MHz LP ≙ 30 MHz



- For all measurements $Z_E = Z_A = 75$ ohm
- Balancing with broad-band wobble measuring set-up (P7) between cassette input X 3004 and preselector 2 - output P 3205
- When balancing: Remove connection to mixer 1 (P 3205 —► P 3301) at P 3205: 75-ohm resistance —► ⊥
- For balancing the respective preselection range the following operation of the receiver is required:

For range I : EKD: [F] 250.00 kHz, [SEL] 1

" II : EKD: " 4500.00 kHz, " 0

" VII : EKD: " 26000.00 kHz, " 1

6.4.3. Signal path 2 1340.041-01321

The following section supplies hints on troubleshooting in the cassette 'signal path 2'.
For this purpose, the plug-in is to be connected outside the casing via adapter cable (30-and 8-core cable, contained in the accessories).

For fault localization:

- Dismount cassette lid (complementation side)
- Apply input signal from RF genprator (P4) to X 3051 (input socket for signal path 2)
- Load line output A (25) and line output B (26) at one end ⏚ and with R = 600 ohm to avoid interferences
- Perform level check acc. to figure 19 or 20.

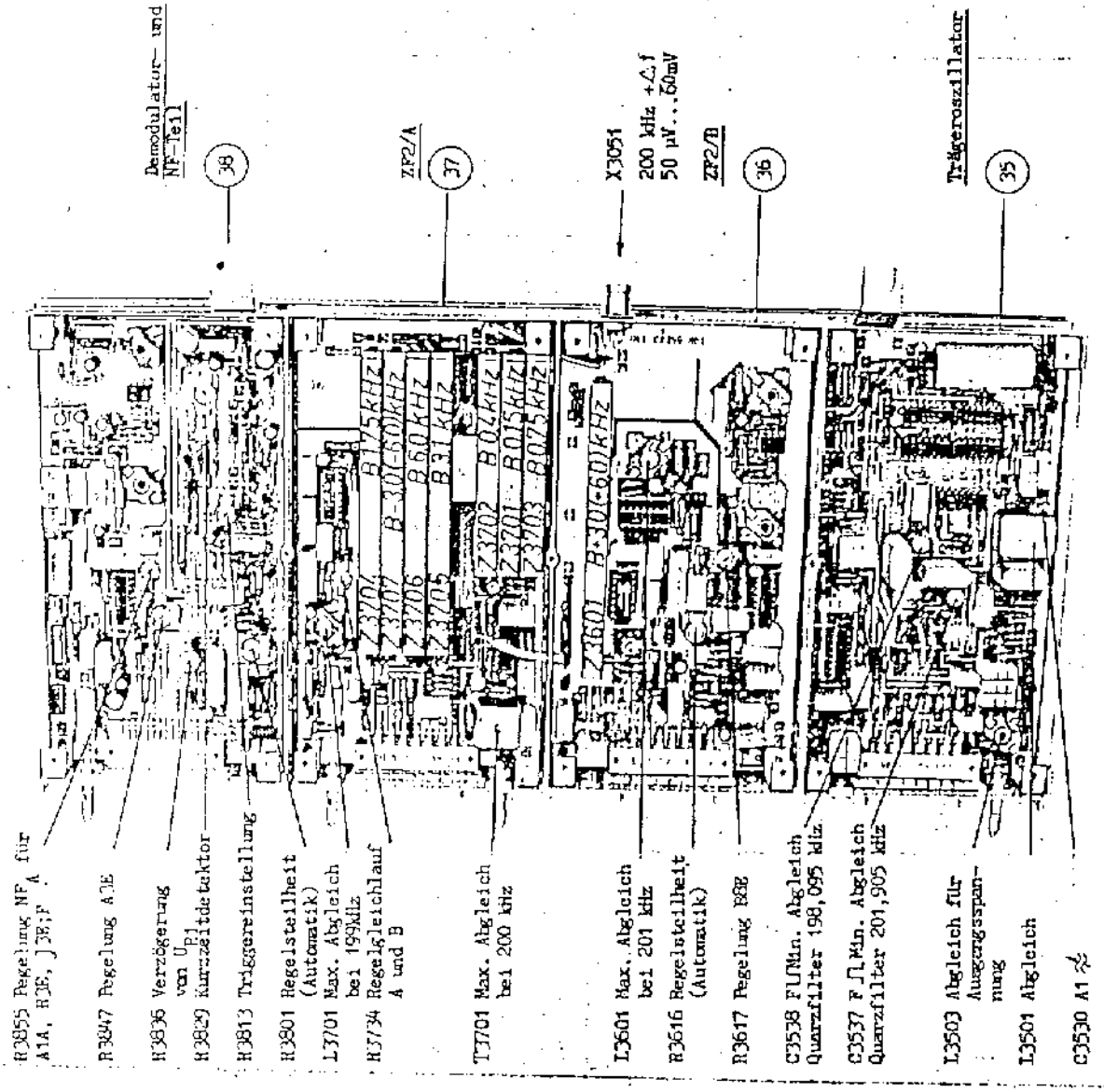


Figure 19

Signal path 2 1340.041-01321

Pegelkontrolle bzw. Pegelkorrektur

	HF-Generator (P4) an X3051 f	HF-Generator (P4) an X3051 $U_{\sim}$	Sendeart	Bandbreite	Verst. Regelung	Prüfung	Prüfpunkt	Meßgröße f	Meßgröße U bzw. $U_{\approx}$
GC 5	–	–	MOD 1	B 6	GC 5	Kontrolle U bzw. $U_{\approx}$	X 3801 /B11	–	≙ 0,75 V – ≙ 0,3 V –
U_{ZF2}-Verst.	199 kHz	55 µV	"	"	GC 5	L 3701 Max.	ZF2 – Ausgang (27)	199 kHz	>100 mV$_{\approx}$
U f_{Tr}-Verst.	200 kHz	10 µV	MOD 3	"	"	T 3701 Max.	ZF2/B P3605 — ⊥	200 kHz	> 30 mV$_{\approx}$
-Kontr.	200 kHz	50 µV	"	"	"	Kontrolle	–	–	LED leuchtet
Trägeroszillator	–	–	MOD 1			A1	X 3801 /B2	≙ 198,8 kHz ≙ 199,5 kHz	110...160 mV$_{\approx}$
	200 kHz	–	MOD 3	beliebig		Kontrolle f und $U_{\approx}$	"	200,00 kHz	120...170 mV$_{\approx}$
(U f_{Tr}, f_{Tr})	–	–	MOD 4	"		"	"	200.00 kHz	"
	–	–	MOD 5						
Regelung/A33 $U_{NF(A)}$	201 kHz	55 µV	MOD 4	B 5	GC 5	R 3855 einstellen	NF-Ltgs.-Ausg.	1 kHz	0 dBm
Regelteilheit	201 kHz	110 µV	"	"	GC 1	R 3801 einstellen	"	1 kHz	-1 dBm
(Automatik)	201 kHz	25 mV	"	"	"	Kontrolle f, $U_{\approx}$	"		≙ +1,2 dBm
Regeleinsatz U_{R1}	201 kHz	1,5 mV	"	"	"	R 3836 einstellen	X 3801 /B10	1 kHz	12,5 V–
Regelung/A33 $U_{NF(A)}$	200 kHz m=0,5/1 kHz	1 mV	MOD 2	"	"	R 3847 einstellen	NF-Ltgs.-Ausg. A	1 kHz	-1 dBm
Abhörverstärker	201 kHz	1,5 mV	MOD 4	"	GC 5	Kontrolle ext.	"	1 kHz	≥ 2 V$_{\approx}$ an 8 Ohm
Regelung/B68 $U_{NF(B)}$	201 kHz	55 µV	MOD 6	B 7	GC 5	L 3601 Max. R 3617 einstellen	NF-Ltgs.-Ausg. B	1 kHz	0 dBm

Figure 20

The measuring criteria are value and frequency response of the output voltage U_A as well as the function of the LED V 4602 ⌐□.

Test and troubleshooting are accomplished in the sequence "Value of the output voltage" - "Frequency of the output voltage".
The tables (figure 21, 22) show, in dependance on the class of emission (MOD) selected, the voltage U of the functional groups or the voltages and frequencies at the inputs U_E, f_E and at the output U_A, f_A ($\hat{=} f_{U3}$) as well as the function of the LED V 4602 ⌐□.

6.4.3.1.1. Output voltage and control voltage generator

The maximum balancing L 3503 is performed at A1A (very flat maximum) or at F ⊔ alternating with F ⊓ to the equal value of U_A. The crystal oscillator is amplitude-controlled via T 3514.

6.4.3.1.2. Crystal oscillator

The crystal-stabilized oscillator is tuned at its frequency by means of the parallel circuit L 3501-C 3521, C 3530 and the capacity diode V 3529.
The frequency range is balanced at A1A with C 3530 (coarse) and L 3501 (fine) to f_A = 198.8 kHz with 0 V at X 3501/B7 and f_A = 199.5 kHz with 9.5 V at X 3501/B7.
Access to the balancing core of L 3501 is provided after dissoldering of the metal tip in the cap centre. After accomplishing balancing work the coil is to be covered again with the metal tip.

6.4.3.1.3. Store and switch

The switch is actuated by the trigger.
Class of emission R3E, U_E = 200 mV, f_E = 200 kHz $\pm\triangle f_E$.
The switch is closed as V 3523 and V 3526 are blocking and V 3508 or V 3509 cause opening - depending on the potential difference - between emitter and collector thus closing the phase control loop
$\triangle f_A = \triangle f_E$.

Class of emission R3E, U_E = 50 mV, f_E = 200 kHz $\pm$ Δf_E.
The switch is open because V 3508 and V 3509 are blocking via V 352
The phase control loop is open, Δf_A is independent of Δf_E, f_A is nearly constant and changes with -3 Hz/min (discharge of store capacitor C 3518).
In case f_A is dependant on f_E: check V 3523, V 3526, V 3508, and V 3509.
When change of f_A too large: replace T 3508, T 3509, T 3510, T 3525, C 3518 in this sequence.
Attention! V 3510 is a MOS transistor. When changing V 3510 or any components which are fed to te transistor terminals these are to be shortened.

In the class of emission J3E, U_E = 200 mV, f_E = 200.000 kHz the operating condition R3E is equal to U_E = 200 mV, f_E = 200.000 kHz. The inverse voltages for V 3523 and V 3526 are firmly switched on via V 3540.

6.4.3.1.4. Phase detector

Direct voltage to N 3501/8 at U_E = 0 : approx. 6 V.
With the control loop closed the voltage at N 3501/8 varies irregularly by approx. $\pm$ 10 % (phase jumps of f_A).

6.4.3.1.5. Voltage path 200.000 kHz

Characteristic of the voltage path: V3501/B3-R3506-V3516-R3503-N3501/14

6.4.3.1.6. Voltage path 200 kHz + Δf_E

Characteristic of the voltage path: V3501-R3508-V3518-C3505-R3503-N3501/14

6.4.3.1.7. Amplifier and trigger

Gate D 3504/9, 10, 11, 8 is included in the amplifier. E 3520 causes slow recharging of C 3517 after having applied the input voltage and with this the delayed response of the trigger (0.5 s) . U_E ≙ 20
V 3504C 15.5 V ⟶ 5 V; V 3503E 3.5 V ⟶ 13.5 V.
V 3521 provokes quick recharging of C 3517 after disconnection of the input voltage and thus immediate response of the trigger.

6.4.3.1.8. Divider 200 kHz/1.905 kHz

Divider ratio 1:105.

For the classes of emission F the divider is put into operation via K input D 3503/10 by applying 2.7 V. The divider consists of the counter components D 3501 and D 3502 as well as of the decoding circuit D 3504 (2 gates) and D 3503 for releasing a reset pulse. Every 103rd pulse at D 3501/14 causes that H potential is applied to the J inputs of D 3503. Thus, the 104th pulse can release a reset pulse at the Q output. This pulse is terminated with the trial edge of the 105th pulse.

6.4.3.1.9. Mixer 200 kHz ± 1.905 kHz

The summation and difference frequencies are available opposite in phase at the outputs N 3502/12 and N 3502/13.
D.C. voltages: N 3502/6.14 approx. 2 V; N 3502/7.9 approx. 3.6 V.
A summation voltage of approx. 400 mV is applied to N 3502/12, 13 (both input- and mixed frequencies).

6.4.3.1.10. Crystal filter 201.905 kHz and 198.095 kHz

Both crystal filters are bridge filters whose branches are activated opposite in phase by N 3502/12 or N 3502/13. After crystal exchange a maximum balance von U_A by minimum tuning of the crystal frequency with C 3535 or C 3536 may be required.
C 3537 and C 3538 provide minimum balancing of the distortion products of U_A (suppression of the undesired frequencies).

Table

DC voltages of the function groups in dependance of the class of emission selected (MOD)

Test value	Function group		Test point	A1A	A3E	R3E, B_R8E	J3E,B8E	F0,F ⎍	F ⎎
DC voltages of the function groups U (V)	Output amplifier and control voltage generator		X3501/B1	18	18	18	18	18	18
	Crystal oscillator		V3548/K	16.5	0	16.0	16.0	0	0
		A1 pitch control	X3501/B7	0...9.5	0	0	0	0	0
	Store and switch		V3542/K	0	0	16.5	16.5	0	0
	Phase detector		V3519/K	0	0	16.5	16.0	0	0
	Voltage path	200.000 kHz	V3516/K	0	0	0	0.7	0.7	0.7
		200 kHz $\pm \Delta$ f	V3517/K	0	0	0.7	0	0	0
	Amplifier and trigger		V3546/K	0	0	16.0	(5)	16	16
	Divider 200/11.905 kHz		X3501/A1 D3503/10	5 0	5 0	5 0	5 0	5 2.7	5 2.7
	Mixer 200 kHz $\pm$ 1.905 kHz		V3534/K	0	0	0	0	16.5	16.5
	Crystal filter	201.905 kHz	X3501/A9	0	0	0	0	17.5	0
		198.095 kHz	X3501/A11	0	0	0	0	0	17.5

Table

Voltages and frequencies at the inputs and at the output as well as the function of the carrier display in dependance on the class of emission selected (MOD)

Test value		Function group	Connection points	A1A	A3E	R3E, B_H8E	J3E, 2B8	F0, F1	F2
Input voltages and frequencies (test)	U_E	Voltage path 200.000 kHz	X3501/B3 —	—	—	—	200 mV	200 mV	200 mV
	f_E		X3501/A3 ⊥				200.00 kHz	200.00 kHz	200.00 kHz
	U_E	Voltage path 200 kHz $\pm \Delta f_E$	P3501 —	—	—	50mV/200mV	—	—	—
	f_E		P3502 ⊥			200kHz+Δf_E $\Delta f_E \leq$ 50Hz			
Output voltages and frequencies	U_A	Output amplifier	X3501/B13 —	110 mV to 160 mV	0	120 to 170 mV	120 to 170 mV	80 to 130 mV W< 5%	80 to 130 mV W< 5 %
R_A = 680 ohm	f_A		X3501/A13	< 198.8 to > 199.5 kHz (A1-pitch control)	—	200kHz+Δf_A U_E=200mV Δf_A=Δf_E U_E=50mV Δf_A const. (<3Hz/min)	200.000 kHz f_A=f_E	201.905 kHz	198.095 kHz
	f_{U3}								
Function Carrier display		Trigger	X3501/B11	dark	dark	U_E=200mV lit U_E=50mV dark	dark	dark	dark

Figure 22

IF2/A, 1340.041-01357
IF2/B, 1340.041-01356

6.4.3.2.1. Amplification in signal path 2 (X3051 —— P3705)

- U_e = 55 µV at X3051 (RF generator P4), GC 5 and ≈
- U_a = 100 mV to 200 mV at P3705 —— ⊥ (millivoltmeter P3)
- U_{R2} = 0.75 V
- Amplification difference with bandwidths B 2... B 4 : ≦ 4 dB
  with B 1 : ≦ 6 dB

Attention Exchange IF2 amplifier circuits N3603 (IF2/B) and N3702 (IF2/A) only in pairs (spare part in B1)

6.4.3.2.2. Carrier amplifier (for R3E and B_R8E)

200 kHz/U_e = 10 µV at X3051 (RF generator P4)
- U_a = 30 mV to 100 mV at P3605 —— ⊥ (millivoltmeter P3)
- 3 dB bandwidth : ≅ ± 50 Hz

6.4.3.2.3. Bandwidth and selection of mechanic filters

B	Rated bandwidth	3 dB bandwidth	60 dB bandwidth
1	0.15 kHz	≅ ± 50 Hz	≅ ± 250 Hz
2	0.4 kHz	≅ ± 150 Hz	≅ ± 500 Hz
3	0.75 kHz	≅ ± 300 Hz	≅ ± 850 Hz
4	1.75 kHz	≅ ± 750 Hz	≅ ± 1250 Hz
5	3.1 kHz	≅ ± 1.5 kHz	≅ ± 2.15 kHz
6	6.0 kHz	≅ ± 3.0 kHz	≅ ± 4.0 kHz
7*)	+3.0 kHz	≅ +(0.25...3.0)kHz	≅ −0.25 kHz; ≅ +3.5 kH
**)	+6.0 kHz	≅ +(0.3...5.9) kHz	≅ −0.3 kHz; ≅ +6.8 kH
8*)	−3.0 kHz	≅ −(0.25...3.0)kHz	≅ +0.25 kHz; ≅ −3.5 k
**)	−6.0 kHz	≅ −(0.3...5.9) kHz	≅ +0.3 kHz; ≅ −6.8 kH
9	⊣	signal path blocked	

*) EKD 511
**) EKD 512

Attention The signs of the built-in sideband channel filters are opposite to that of the input signal (sideband commutation in mixer 1).

6.4.3.3. Demodulator and AF section 1340.039-01358

6.4.3.3.1. Demodulator/A1A; J3E; F1B; F3C

Level outline with input signal applied

At P 3801 → ⊥: IF2 signal = 201 kHz or 200 kHz/100 mV, GC 5

At N 3801/14 : $Uf_{carrier}$ (lim.) = 200 mV to 350 mV_{ss}

At N 3801/9 : U_{IF2} = 7 ... 15 mV≈

At N 3801/8 : U_{AF} = 50 ... 55 mV≈
adjust with R 3855

6.4.3.3.2. Demodulator/A3E

Level outline with input signal applied

At P01 → ⊥: IF2 signal = 200 kHz/m = 0.5; 1 kHz, 100 mV, GO 5

At X01/14 : IF2 signal = 3 ... 5 mV≈

At X01/8 : U_{AF} = 50 ... 55 mV≈ ; adjust with R 3847

Attention At input P 3801 → ⊥ : approx. 1.1 V dc voltage

6.4.3.3.3. AF line amplifier 'channel A'

Level outline with input signal applied

At N 3802/3 : U_{AF} = 50 ... 55 mV≈

At N 3802/6 : U_{AF} = 0.775 V≈ (with 52 mV at N 3801/8)

At X 3801/B4 : U_{AF} = 0.775 V≈

Line output 'A' : at X 3802/5 : 8.8 ... 9.2 V ⎓
at X3802/10 : 8.8 ... 9.2 V ⎓

6.4.3.3.4. Monitoring amplifier

U_{β} at X X 3801: 100 mV (for 0.5 W across 8 ohm X 1021 🔊 external)
(Correcting of amplification possible with R 71.)

Attention Do not generate AF power with the heat radiator disconnected (thermal overload) !

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6.4.3.3.5. Control amplifier

- Manual control: GC 5

  Generation of U manual control by voltage divider R 3845, R 1002 (⊀ ≈) and R 1007

R 1002	→ Mixer 1	→ IF amplification A/B
☝ ⌒	U_{R1} ≙ 14.5 V ⎓	U_{R2} ≙ 0.75 V ⎓
☝ ⌒	U_{R1} ≙ 9.5 V ⎓	U_{R2} ≙ 0.3 V ⎓

- Automatic control: GC 1, GC 2

  At P 3801 → ⊥ : $U_{\approx}$ = 100 mV/200 kHz

  At IF output (27): ≙ 100 mV (without load)

  U at V 3821_B = approx. 45 mV≈ (adjustable with R 3801)

  Control detector/A : U at V 3824_B > +4 V

	Trigger (not driven)	Trigger (driven)
Trigger V 3826_C	≙ 0.55 V ⎓	>17 V ⎓
Holding circuit V 3827_C	approx. 1,25 V ⎓	approx. 0.25 V ⎓
Long-time detector V 3828_B	approx. 0.66 V ⎓	0

$U_{C\ 3808}$ =,3 ... 4 V

Short-time detector $U_{R3829/R3830}$ = 3 ... 4 V ⎓

Amplifier V 3829_B = 13 ... 14 V ⎓

Amplifier V 3830_C = 12 ... 13 V ⎓

Voltage ot slider R 29 = $U_{C\ 3808}$ -0.6 V

6.5. FM demodulator 1340.041-01258

6.5.1. Check 'input signal' (X 2801/A, B1 or X 0002)

Receiver setting: F 0,00 kHz

B 6

MOD 7, 8 or 9

GC 5

Adjust input voltage with control " $\not\approx$ " to 0.8 V.

Measure input frequency at MOD 7, 8 and 9
Setpoint value: 1905 Hz ± 1 Hz

6.5.2. Check 'input band-pass' (N 2801)

(P 12 serves as earth reference for all measurements on this pc board.)

Measure 3-dB decrease at P 01 with dF = 0.10 kHz
Pass range approx. 1.1 kHz to 2.7 kHz
Slope steepness approx. 12 dB/oct.
Operating residual attenuation 1.5 dB to 2 dB

6.5.3. Check 'limiter amplifier' (N 2802, V 2804, V 2805)

U_{P02} : approx. V_{rms} at U_e = 500 mV to 2,5 V
(adjust with control $\not\approx$)

U_{P03} : approx. 0.8 V_{pp}

6.5.4. Check 'PLL' (N 2803, N 2804, D 2801, V 2806 ... V 2816)

Measure PLL zero position and VCO frequency with the signal path blocked (B 9).

Rebalancing: PLL zero position with R 2826 (0 V ± 5 mV at P04)
VCO frequency with R 2842 (1905 Hz ± 2 Hz at P05)

(Forced changeover with IF bandwidth [B])

100-Bd low pass: at [B] 1, 2, 3 (f_g approx. 150 Hz)

600-Bd low pass: at [B] 4, 5, 6 (f_g approx. 900 Hz)

Offset correction : for 100-Bd low pass with R2867 at P 09
for 600-Bd low pass with R2876 and R2883 at P 08 and P 09

6.5.6. Check 'amplifier' (N 2810)

Measure V = approx. 40 with low Δf (e.g. 80 Hz)
Offset correction with R 2891.

6.5.7. Check 'evaluator circuit' (N 2811)

At centre frequency (1905 Hz)	: U_{P11} = 0 V ± 15 mV
At centre frequency $+\Delta f$ = 500 Hz	: U_{P11} = + 1 V ± 50 mV
At centre frequency $-\Delta f$ = 500 Hz	: U_{P11} = − 1 V ± 50 mV
In case of exceeding U_{P11} values	: balance with R 2892
In case of too low U_{P11} values	: balance with R 2897

6.5.8. Check 'Line current for teleprinter'

Connect ammeter with 200 ohm (load resistance) in series to teleprinter terminal (X 0008, 3 and 4).

At [MOD] 1 ... 7 : 40 mA ± 5 mA (correction with R 28106)

6.5.9. Check 'holding and capture range of PLL'

Receiver setting:

[F]	0.00 kHz
[dF]	0.01 kHz
[MOD]	8 and 9
[B]	6
[GC]	1

Changeover switch 'LED row' (2)→'Δfx2'

Holding range: Setpoint value: $\Delta f = \pm 900$ Hz referred to centre frequency

Increase frequency with rotary button " ≋ " until luminous point of the LED row jumps from row end to row centre.

Capture range: Setpoint value: $\Delta f \cong \pm 800$ Hz referred to centre frequency

Detune frequency of Δf values 2.00 kHz towards 0.00 kHz by means of rotary button " ≋ ".

ccomplish this function check at [MOD] 8 and [MOD] 9.

heck simultaneously the synchronization process through
onitoring tone.

100